



# 3.3V CMOS 16-BIT EDGE-TRIGGERED D-TYPE FLIP- FLOP WITH 3-STATE OUTPUTS, 5V TOLERANT I/O AND BUS-HOLD

## IDT74LVCH16374A

### FEATURES:

- Typical  $t_{sk(0)}$  (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to +85°C
- $V_{CC} = 3.3V \pm 0.3V$ , Normal Range
- $V_{CC} = 2.7V$  to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

### Drive Features for LVCH16374A

- High Output Drivers:  $\pm 24mA$
- Reduced system switching noise

### APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

### DESCRIPTION

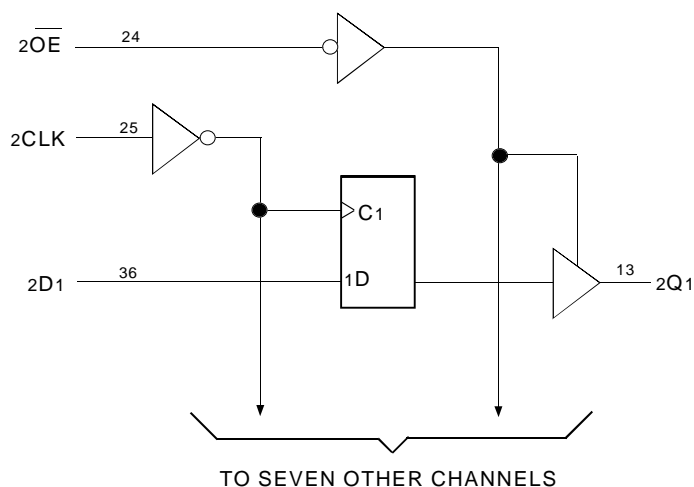
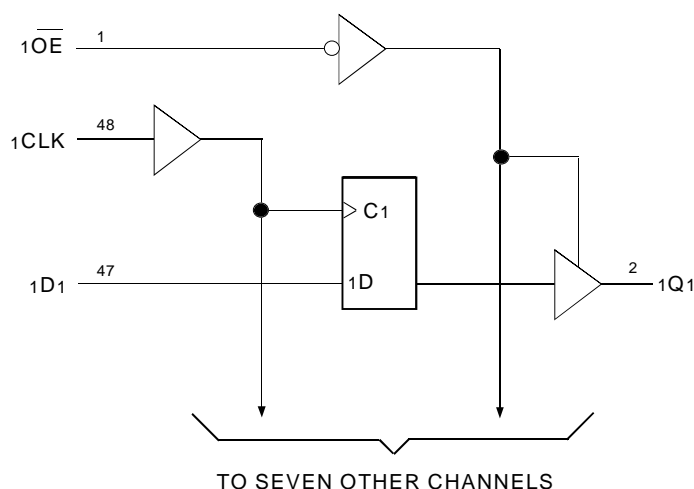
The LVCH16374A 16-bit edge-triggered D-type register is built using advanced dual metal CMOS technology. This high-speed, low-power register is ideal for use as a buffer register for data synchronization and storage. The Output Enable ( $\overline{OE}$ ) and clock (CLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

All pins of the LVCH16374A can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

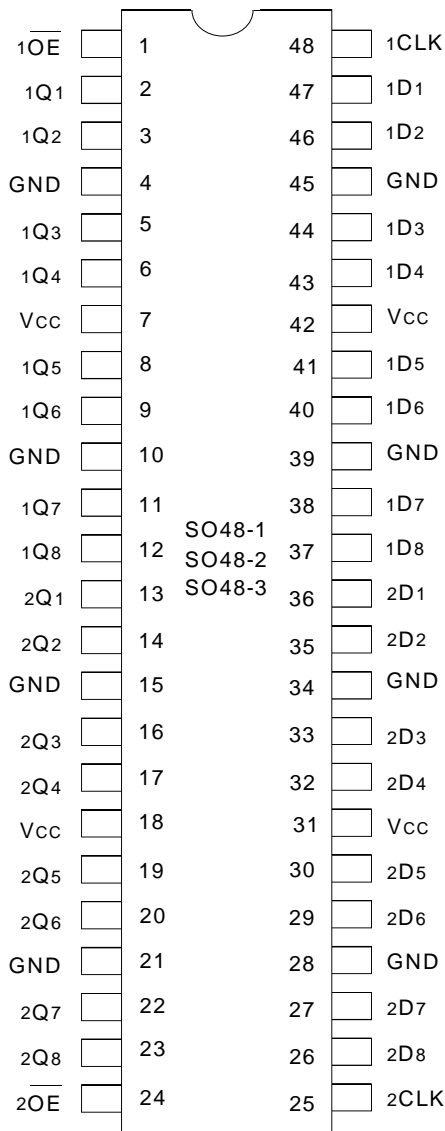
The LVCH16374A has been designed with a  $\pm 24mA$  output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH16374A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

### Functional Block Diagram



## PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP  
TOP VIEW

## PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs <sup>(1)</sup>
xCLK	Clock Inputs
xQx	3-State Outputs
$\overline{xOE}$	3-State Output Enable Input (Active LOW)

### NOTE:

- These pins have "Bus-hold". All other pins are standard inputs, outputs or I/Os.

## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
TSTG	Storage Temperature	- 65 to +150	°C
IOUT	DC Output Current	- 50 to +50	mA
I <sub>IK</sub> I <sub>OK</sub>	Continuous Clamp Current, V <sub>I</sub> < 0 or V <sub>O</sub> < 0	- 50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

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### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	6.5	8	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	6.5	8	pF

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### NOTE:

- As applicable to the device type.

## FUNCTION TABLE (each flip-flop) (1)

Inputs			Outputs
$\overline{xOE}$	xCLK	xDx	xQx
L	↑	H	H
L	↑	L	L
L	H or L	X	Q <sub>0</sub> <sup>(2)</sup>
H	X	X	Z

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW-to-HIGH transition  
Z = High-Impedance
- Q<sub>0</sub> = Output level before the indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IIH IIL	Input Leakage Current	VCC = 3.6V	VI = 0 to 5.5V	—	—	±5	µA
IOZH IOZL	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	VO = 0 to 5.5V	—	—	±10	µA
IOFF	Input/Output Power Off Leakage	VCC = 0V, VIN or VO ≤ 5.5V		—	—	±50	µA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		—	-0.7	-1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	VCC = 3.6V	VIN = GND or VCC	—	—	10	µA
			3.6 ≤ VIN ≤ 5.5V <sup>(2)</sup>	—	—	10	
ΔICC	Quiescent Power Supply Current Variation	One input at VCC - 0.6V other inputs at VCC or GND		—	—	500	µA

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### NOTES:

1. Typical values are at VCC = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## BUS-HOLD CHARACTERISTICS

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 3.0V	VI = 2.0V	-75	—	—	µA
			VI = 0.8V	75	—	—	
IBHH IBHL	Bus-Hold Input Sustain Current	VCC = 2.3V	VI = 1.7V	—	—	—	µA
			VI = 0.7V	—	—	—	
IBHHO IBHLO	Bus-Hold Input Overdrive Current	VCC = 3.6V	VI = 0 to 3.6V	—	—	±500	µA

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### NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at VCC = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OH</sub> = -0.1mA	V <sub>CC</sub> - 0.2	—	V
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -6mA	2	—	
		V <sub>CC</sub> = 2.3V	I <sub>OH</sub> = -12mA	1.7	—	
		V <sub>CC</sub> = 2.7V		2.2	—	
		V <sub>CC</sub> = 3.0V		2.4	—	
		V <sub>CC</sub> = 3.0V	I <sub>OH</sub> = -24mA	2.2	—	
VOL	Output LOW Voltage	V <sub>CC</sub> = 2.3V to 3.6V	I <sub>OL</sub> = 0.1mA	—	0.2	V
		V <sub>CC</sub> = 2.3V	I <sub>OL</sub> = 6mA	—	0.4	
			I <sub>OL</sub> = 12mA	—	0.7	
		V <sub>CC</sub> = 2.7V	I <sub>OL</sub> = 12mA	—	0.4	
		V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 24mA	—	0.55	

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### NOTE:

- V<sub>IH</sub> and V<sub>IL</sub> must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V<sub>CC</sub> range. T<sub>A</sub> = -40°C to +85°C.

## OPERATING CHARACTERISTICS, V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>A</sub> = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per flip-flop Outputs enabled	C <sub>L</sub> = 0pF, f = 10Mhz	58	pF
CPD	Power Dissipation Capacitance per flip-flop Outputs disabled		24	pF

## SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
f <sub>MAX</sub>		150	—	150	—	MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xCLK to xQx	—	4.9	1.5	4.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time x $\overline{OE}$ to xQx	—	5.3	1.5	4.6	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time x $\overline{OE}$ to xQx	—	6.1	1.5	5.5	ns
t <sub>SU</sub>	Set-up Time, data before CLK $\uparrow$	1.9	—	1.9	—	ns
t <sub>H</sub>	Hold Time, data after CLK $\uparrow$	1.1	—	1.1	—	ns
t <sub>w</sub>	Pulse duration, CLK HIGH or LOW	3.3	—	3.3	—	ns
t <sub>sk(o)</sub>	Output Skew <sup>(2)</sup>	—	—	—	500	ps

### NOTES:

- See test circuits and waveforms. T<sub>A</sub> = -40°C to +85°C.
- Skew between any two outputs of the same package and switching in the same direction.

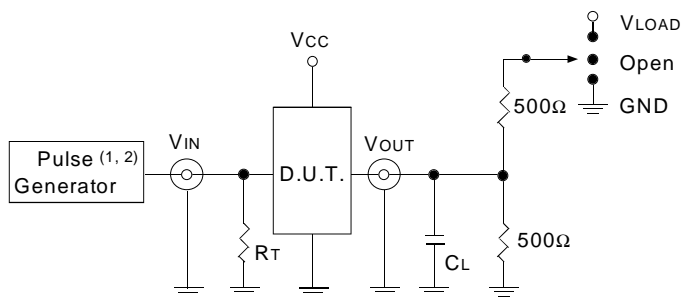
## TEST CIRCUITS AND WAVEFORMS

### TEST CONDITIONS

Symbol	V <sub>CC</sub> (1) = 3.3V ± 0.3V	V <sub>CC</sub> (1) = 2.7V	V <sub>CC</sub> (2) = 2.5V ± 0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF

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### TEST CIRCUITS FOR ALL OUTPUTS



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#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

#### NOTE:

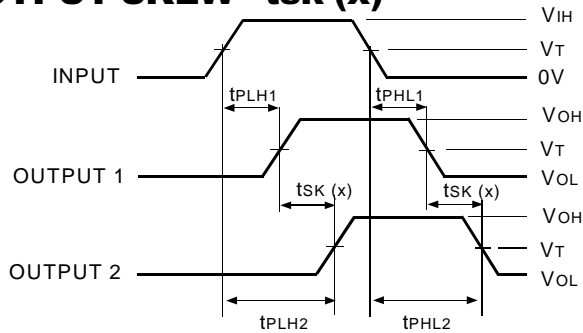
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2.5ns; t<sub>R</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>F</sub> ≤ 2ns; t<sub>R</sub> ≤ 2ns.

### SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other tests	Open

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### OUTPUT SKEW - t<sub>SK</sub>(x)



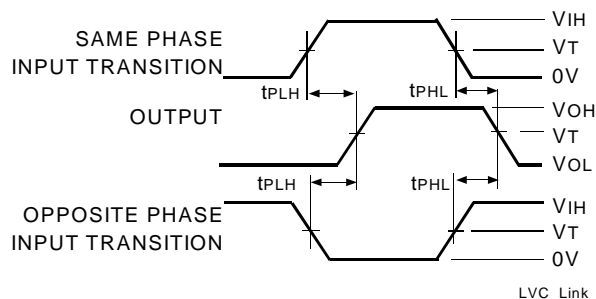
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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#### NOTES:

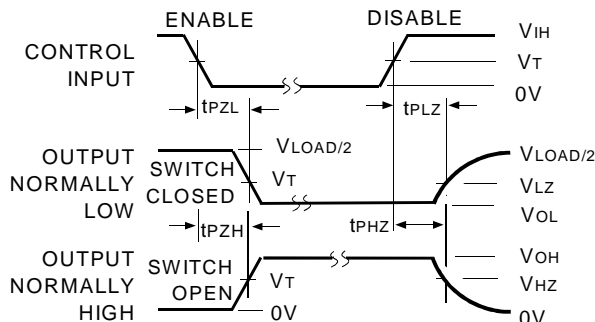
1. For t<sub>SK</sub>(a) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.

### PROPAGATION DELAY



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### ENABLE AND DISABLE TIMES

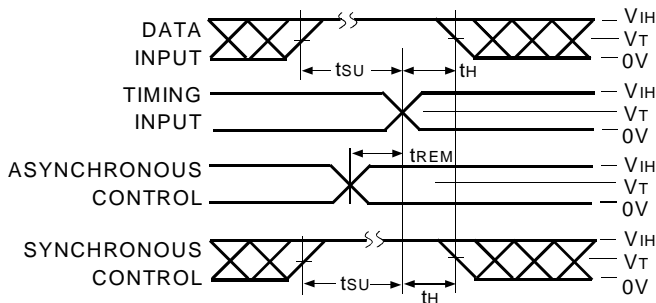


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#### NOTE:

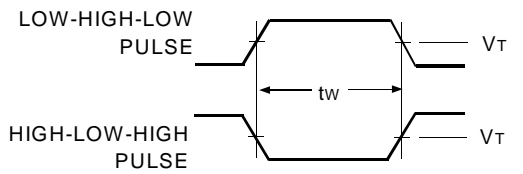
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

### SET-UP, HOLD, AND RELEASE TIMES



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### PULSE WIDTH



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