# 3.3V CMOS 3-LINE TO 8-LINE DECODER/DEMULTIPLEXER, WITH ADDRESS LATCHES

**IDT74LVC137A**

## FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.635mm pitch QSOP, 0.65mm pitch SSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of – 40°C to +85°C
- $V_{CC}$ = 3.3V ±0.3V, Normal Range
- $V_{CC}$ = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

**Drive Features for LVC137A:**

- High Output Drivers: ±24mA
- Reduced system switching noise

## APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

## DESCRIPTION:

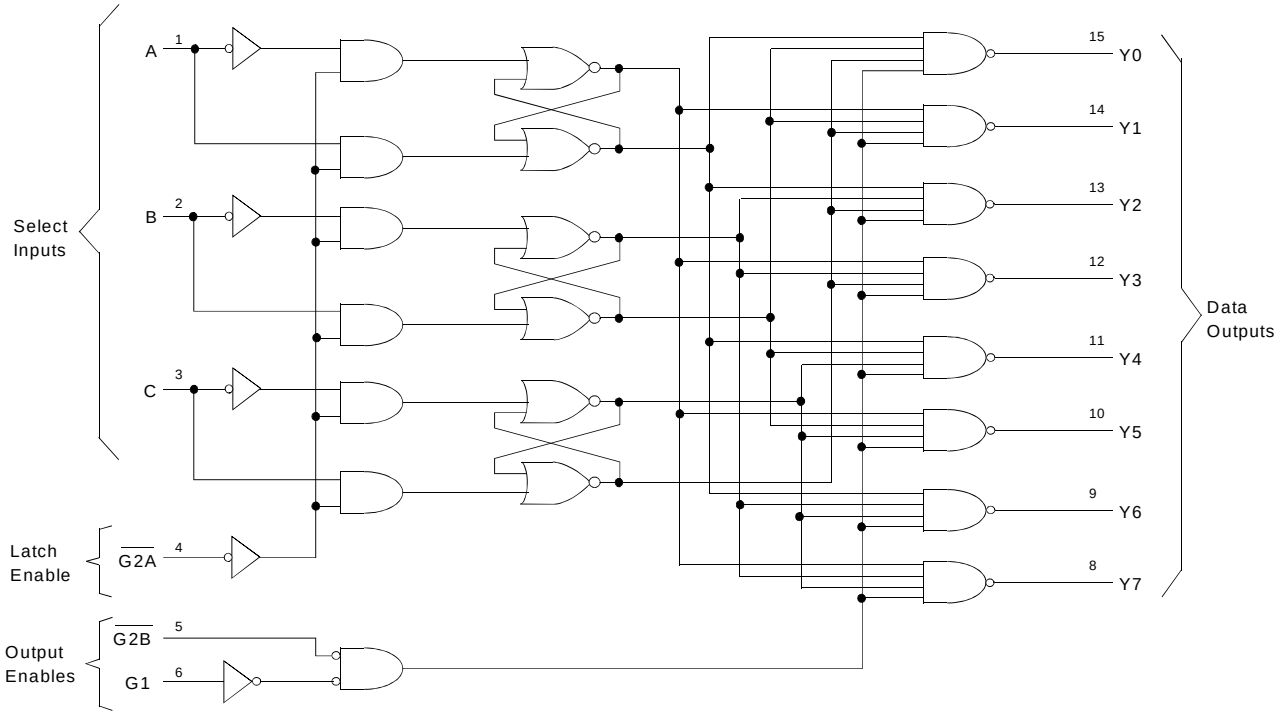
The LVC137A 3-line to 8-line decoder/demultiplexer is built using advanced dual metal CMOS technology. The LVC137A is designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder minimizes the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

When the latch enable ($\overline{G2A}$) input is low, the LVC137A acts as a decoder/demultiplexer. When $\overline{G2A}$ transitions from low to high, the address present at the inputs (A, B, and C) is stored in the latches. Further address changes are ignored, provided $\overline{G2A}$ remains high. The output-enable (G1 and $\overline{G2B}$) inputs control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2B}$ is high.

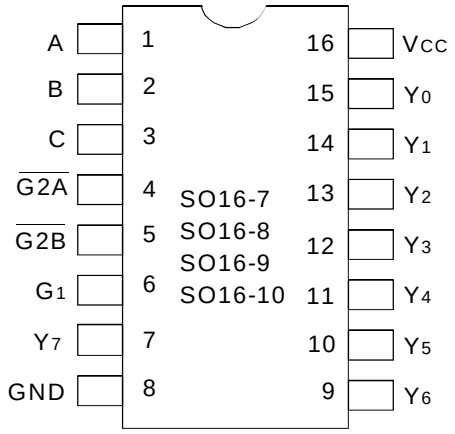
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC137A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

## Functional Block Diagram



## PIN CONFIGURATION




**SOIC/ SSOP/ TSSOP/ QSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | – 0.5 to +6.5 | V |
| $V_{TERM}$(3) | Terminal Voltage with Respect to GND | – 0.5 to +6.5 | V |
| $T_{STG}$ | Storage Temperature | – 65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | – 50 to +50 | mA |
| $I_{IK}$<br>$I_{OK}$ | Continuous Clamp Current,<br>$V_I$ < 0 or $V_O$ < 0 | – 50 | mA |
| $I_{CC}$<br>$I_{SS}$ | Continuous Current through<br>each $V_{CC}$ or GND | ±100 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{CC}$ terminals.
3. All terminals except $V_{CC}$.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| G1 | Output Enable |
| $\overline{G2A}$ | Latch Enable (Active LOW) |
| $\overline{G2B}$ | Output Enable (Active LOW) |
| Yx | Data Outputs |
| A, B, C | Select Data Inputs |

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 5.5 | 8 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 6.5 | 8 | pF |

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**NOTE:**
1. As applicable to the device type.

## FUNCTION TABLE(1)

| Inputs | | | Select Inputs | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Latch Enable | Output Enable | | | | | | | | | | | | |
| $\overline{G2A}$ | G1 | $\overline{G2B}$ | C | B | A | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| L | H | L | L | L | L | L | H | H | H | H | H | H | H |
| L | H | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | L | H | H | L | H | H | H | H | H |
| L | H | L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | L | H | H | H | H | H | H | H | H | H | H | L |
| H | H | L | X | X | X | Outputs corresponding to stored address = L; all other outputs = H | | | | | | | |

**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

**Following Conditions Apply Unless Otherwise Specified:**
**Operating Condition: $T_A$ = – 40°c to +85°c**

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$<br>$I_{IL}$ | Input Leakage Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 5.5V | — | — | ±5 | µA |
| $I_{OZH}$<br>$I_{OZL}$ | High Impedance Output Current<br>(3-State Output pins) | $V_{CC}$ = 3.6V | $V_O$ = 0 to 5.5V | — | — | ±10 | µA |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{CC}$ = 0V, $V_{IN}$ or $V_O \leq$5.5V | | — | — | ±50 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = – 18mA | | — | – 0.7 | – 1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V | $V_{IN}$ = GND or $V_{CC}$ | — | — | 10 | µA |
| $\Delta I_{CC}$ | Quiescent Power Supply<br>Current Variation | One input at $V_{CC}$ – 0.6V<br>other inputs at $V_{CC}$ or GND | | — | — | 500 | µA |

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**NOTE:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

# OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions(1) | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 6mA | 2 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 12mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | | 2.2 | — | |
| | | $V_{CC}$ = 3.0V | | 2.4 | — | |
| | | $V_{CC}$ = 3.0V | $I_{OH}$ = – 24mA | 2.2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 6mA | — | 0.4 | |
| | | | $I_{OL}$ = 12mA | — | 0.7 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 12mA | — | 0.4 | |
| | | $V_{CC}$ = 3.0V | $I_{OL}$ = 24mA | — | 0.55 | |

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**NOTE:**
1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to +85°C.

## OPERATING CHARACTERISTICS, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | Vcc = 2.5V±0.2V | Vcc = 3.3V±0.3V | Unit |
|---|---|---|---|---|---|
| | | | Typical | Typical | |
| $C_{PD}$ | Power Dissipation Capacitance | $C_L$ = 0pF, f = 10Mhz | — | 25 | pF |

## SWITCHING CHARACTERISTICS (1)

| Symbol | Parameter | Vcc = 2.5V±0.2V | | Vcc = 2.7V | | Vcc = 3.3V±0.3V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>A to B, C to Yx | — | — | — | 6.9 | 1 | 6.2 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{G2A}$ to Yx | — | — | — | 8.5 | 1 | 7.8 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>G1 or $\overline{G2B}$ to Yx | — | — | — | 8.2 | 1 | 7.5 | ns |
| $t_W$ | Pulse Duration, $\overline{G2A}$ | 3 | — | 3 | — | 3 | — | ns |
| $t_{SU}$ | Setup Time, at A, B, and C before $\overline{G2A}\downarrow$ | 2 | — | 2.1 | — | 1.9 | — | ns |
| $t_H$ | Hold Time, at A, B, and C after $\overline{G2A}\downarrow$ | 1.2 | — | 1.1 | — | 1.1 | — | ns |
| $t_{SK(0)}$ | Output Skew(2) | — | — | — | — | — | 1 | ns |

**NOTES:**
1. See test circuits and waveforms. $T_A$ = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$= 2.5V ±0.2V | $V_{CC}^{(2)}$= 3.3V ±0.3V & 2.7V | Unit |
|---|---|---|---|
| $V_{LOAD}$ | 2 x Vcc | 6 | V |
| $V_{IH}$ | Vcc | 2.7 | V |
| $V_T$ | Vcc / 2 | 1.5 | V |
| $V_{LZ}$ | 150 | 300 | mV |
| $V_{HZ}$ | 150 | 300 | mV |
| $C_L$ | 30 | 50 | pF |

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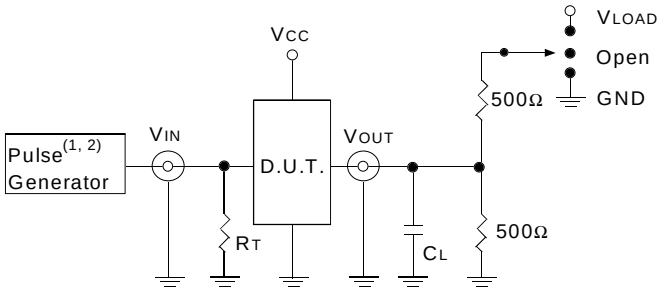
## TEST CIRCUITS FOR ALL OUTPUTS

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**DEFINITIONS:**

$C_L$= Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

**NOTES:**

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other tests | Open |

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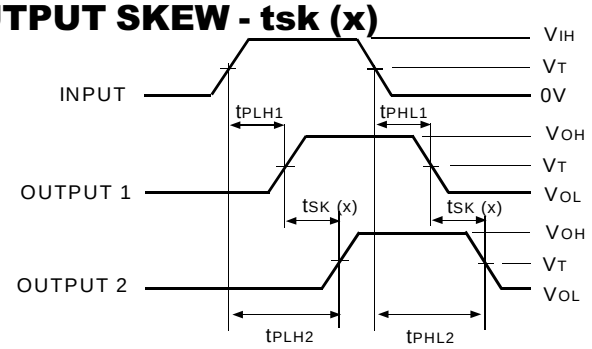
## OUTPUT SKEW - tsk (x)




$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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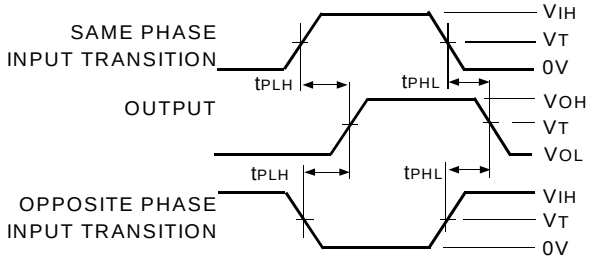
**NOTES:**

1. For $t_{SK}$(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}$(b) OUTPUT1 and OUTPUT2 are in the same bank.

## PROPAGATION DELAY

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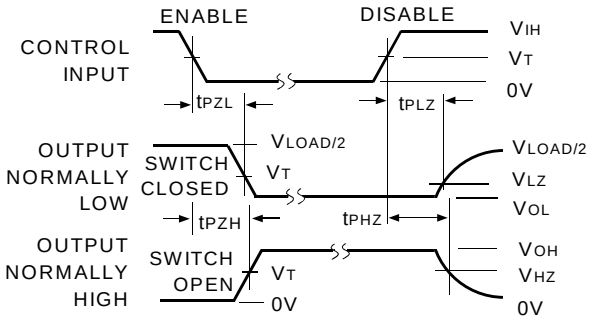
## ENABLE AND DISABLE TIMES

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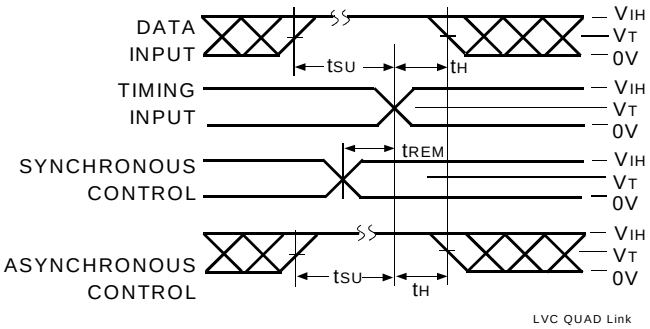
**NOTE:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

## SET-UP, HOLD, AND RELEASE TIMES

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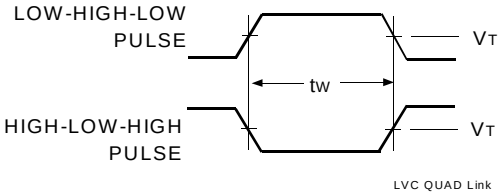
## PULSE WIDTH

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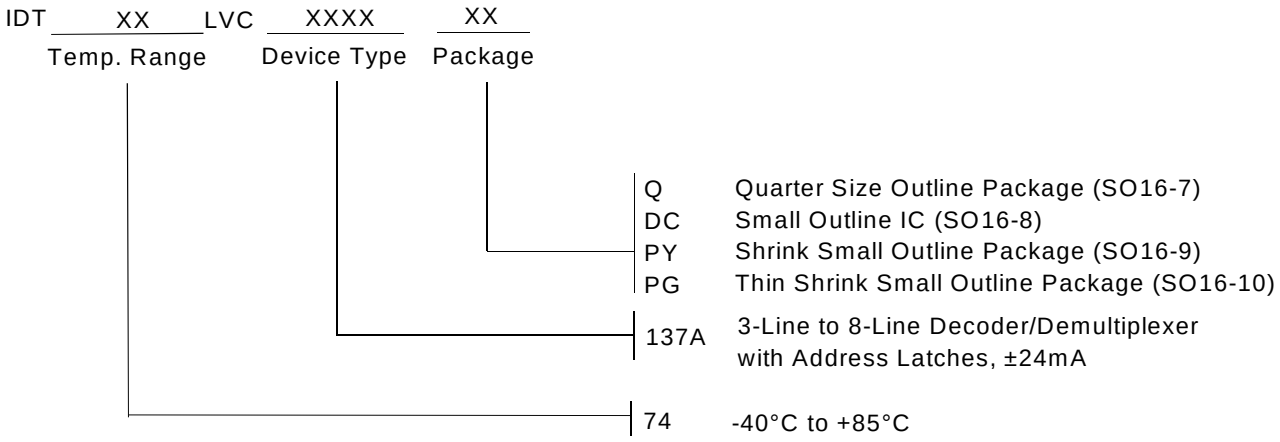
# ORDERING INFORMATION

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