3.3 VOLT MULTIMEDIA FIFO 256 x 8, 512 x 8, 1,024 x 8, 2,048 x 8, and 4,096 x 8

PRELIMINARY

IDT72V10081, IDT72V11081
IDT72V12081, IDT72V13081
IDT72V14081

FEATURES:

- 256 x 8-bit organization array (IDT72V10081)
- 512 x 8-bit organization array (IDT72V11081)
- 1,024 x 8-bit organization array (IDT72V12081)
- 2,048 x 8-bit organization array (IDT72V13081)
- 4,096 x 8-bit organization array (IDT72V14081)
- 15 ns read/write cycle time
- 5V input tolerant
- Independent Read and Write clocks
- Empty and Full Flags signal FIFO status
- Output Enable puts output data bus in high-impedance state
- Available in 32-pin plastic Thin Quad FlatPack (TQFP)
- Industrial temperature range (–40°C to +85°C)

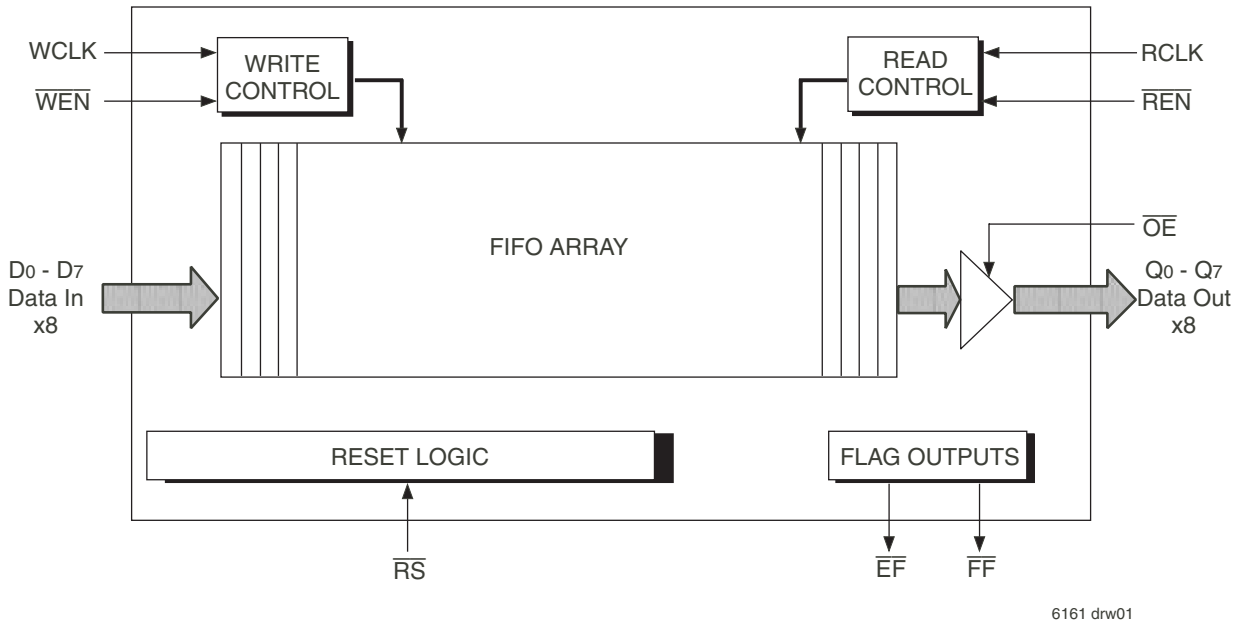
DESCRIPTION:

The IDT72V10081/72V11081/72V12081/72V13081/72V14081 devices are low-power First-In, First-Out (FIFO) memories with clocked read and write controls. These devices have a 256, 512, 1,024, 2,048 and 4,096 x 8-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs such as graphics and interprocessor communication.

These FIFOs have 8-bit input and output ports. The input port is controlled by a free-running clock (WCLK) and Write Enable pin ($\overline{WEN}$). Data is written into the Multimedia FIFO on every rising clock edge when the Write Enable pin is asserted. The output port is controlled by another clock pin (RCLK) and Read Enable pin ($\overline{REN}$). The Read Clock can be tied to the Write Clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An Output Enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Multimedia FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). These FIFOs are fabricated using IDT's submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM



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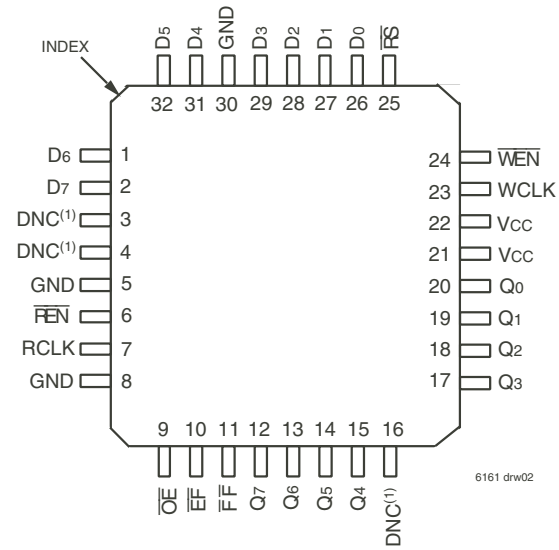
PIN CONFIGURATION



NOTE:
1. DNC = Do Not Connect.

TQFP (PR32-1, order code: PF)
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0-D_7	Data Inputs	I	Data inputs for a 8-bit bus.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
Q_0-Q_7	Data Outputs	O	Data outputs for a 8-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN}$ is asserted.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ goes HIGH, and $\overline{EF}$ goes LOW. A Reset is required before an initial Write after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable is asserted.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition WCLK. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
V_{CC}	Power	I	3.3V volt power supply.
GND	Ground	I	Ground pin.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +5	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminal only.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Industrial	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Industrial	2.0	—	5.5	V
V_{IL}	Input Low Voltage Industrial	-0.5	—	0.8	V
T_A	Operating Temperature Industrial	-40	—	85	°C

DC ELECTRICAL CHARACTERISTICS

(Industrial: V_{CC} = 3.3V ± 0.3V, T_A = -40°C to +85°C)

		IDT72V10081 IDT72V11081 IDT72V12081 IDT72V13081 IDT72V14081 Industrial t_{CLK} = 15 ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	—	—	0.4	V
I_{CC1}(3,4,5)	Active Power Supply Current	—	—	20	mA
I_{CC2}(3,6)	Standby Current	—	—	5	mA

NOTES:
1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs disabled (I_{OUT} = 0).
4. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
5. Typical I_{CC1} = 0.17 + 0.48*fs + 0.02*C_L*fs (in mA) with V_{CC} = 3.3V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
6. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. With output deselected ($\overline{OE}$ ≥ V_{IH}).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS[1]

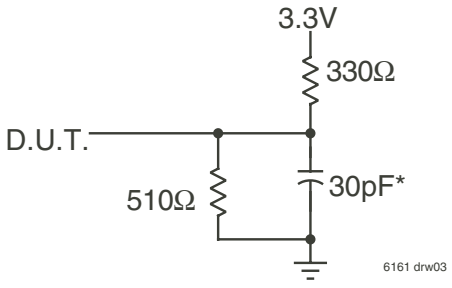
(Industrial: Vcc = 3.3 ±0.3V, TA = -40°C to + 85°C)

		Industrial IDT72V10081L15 IDT72V11081L15 IDT72V12081L15 IDT72V13081L15 IDT72V14081L15		
Symbol	Parameter	Min.	Max.	Unit
f_S	Clock Cycle Frequency	—	66.7	MHz
t_A	Data Access Time	2	10	ns
t_{CLK}	Clock Cycle Time	15	—	ns
t_{CLKH}	Clock High Time	6	—	ns
t_{CLKL}	Clock Low Time	6	—	ns
t_{DS}	Data Setup Time	4	—	ns
t_{DH}	Data Hold Time	1	—	ns
t_{ENS}	Enable Setup Time	4	—	ns
t_{ENH}	Enable Hold Time	1	—	ns
t_{RS}	Reset Pulse Width[1]	15	—	ns
t_{RSS}	Reset Setup Time	10	—	ns
t_{RSR}	Reset Recovery Time	10	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	ns
t_{OLZ}	Output Enable to Output in Low-Z[2]	0	—	ns
t_{OE}	Output Enable to Output Valid	3	8	ns
t_{OHZ}	Output Enable to Output in High-Z[2]	3	8	ns
t_{WFF}	Write Clock to Full Flag	—	10	ns
t_{REF}	Read Clock to Empty Flag	—	10	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Empty Flag &Full Flag	6	—	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D0 - D7)

Data inputs for 8-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EF}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros.

WRITE CLOCK (WCLK)

A write cycle is initiated on the LOW-to-HIGH transition of the Write Clock (WCLK). Data setup and hold times must be met in respect to the LOW-to-HIGH transition of the Write Clock (WCLK). The Full Flag (FF) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock (WCLK).

The Write and Read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)

When Write Enable ($\overline{WEN}$) is low, data can be loaded into the input register and FIFO array on the LOW-to-HIGH transition of every Write Clock (WCLK). Data is stored in the FIFO array sequentially and independently of any on-going read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs on the LOW-to-HIGH transition of the Read Clock (RCLK). The Empty Flag ($\overline{EF}$)is synchronized with respect to the LOW-to-HIGH transition of the Read Clock (RCLK).

The Write and Read clocks can be asynchronous or coincident.

READ ENABLES ($\overline{REN}$)

When both Read Enable ($\overline{REN}$) is LOW, data is read from the FIFO array to the output register on the LOW-to-HIGH transition of the Read Clock (RCLK).

When Read Enable ($\overline{REN}$) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{REF} and a valid read can begin. The Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q output data bus is in a high-impedance state.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 256 writes for the IDT72V10081, 512 writes for the IDT72V11081, 1,024 writes for the IDT72V12081, 2,048 writes for the IDT72V13081 and 4,096 writes for the IDT72V14081.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock (WCLK).

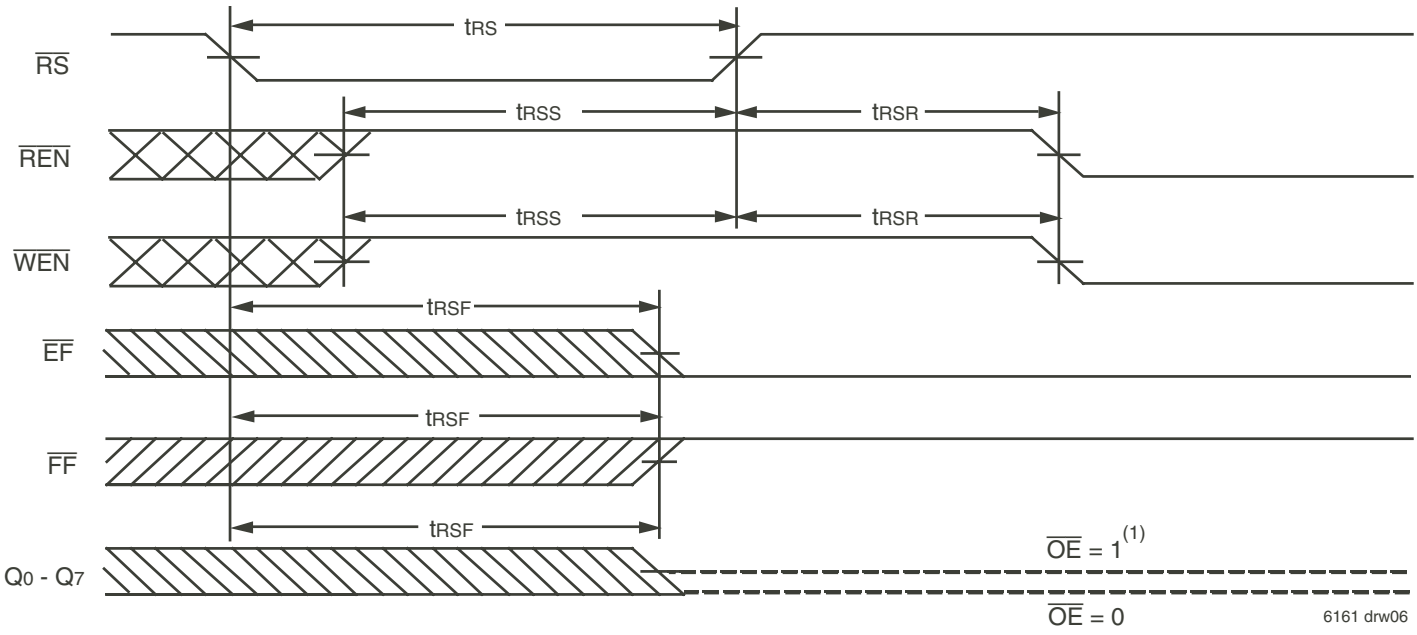
EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the Read Clock (RCLK).

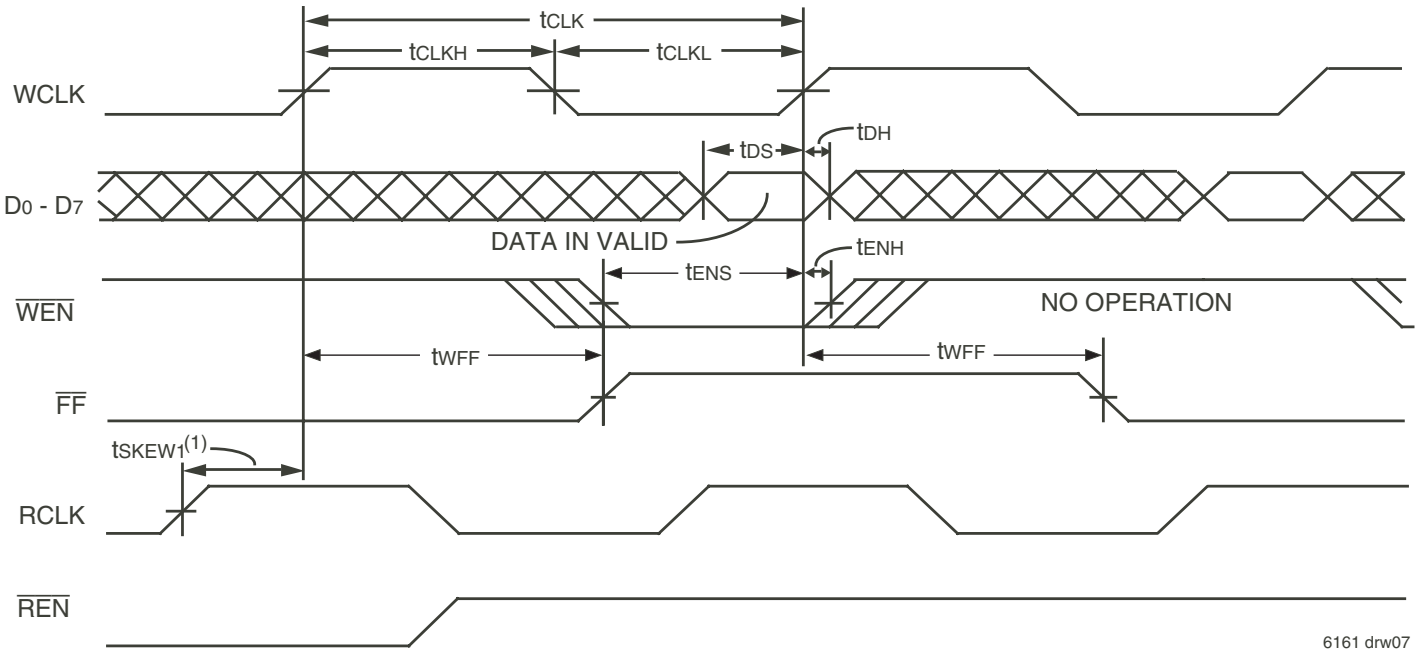
DATA OUTPUTS (Q_0 - Q7)

Data outputs for a 8-bit wide data.



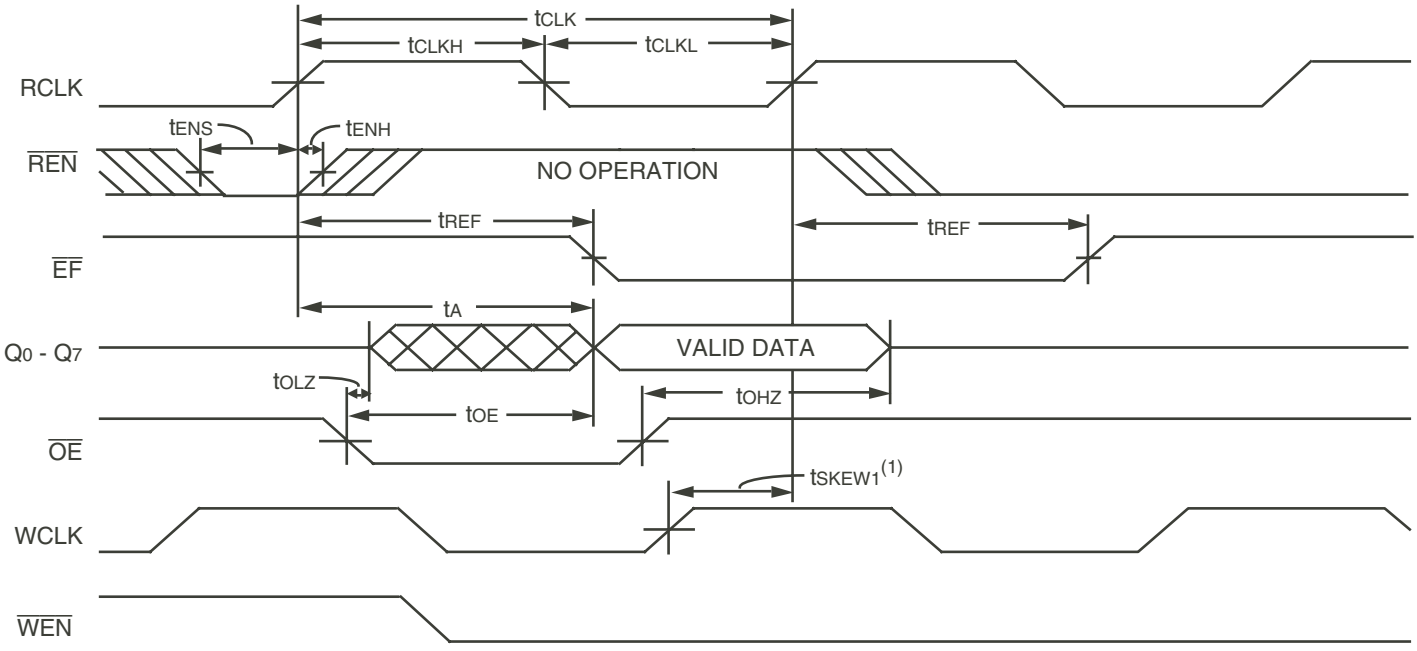
NOTES:
1. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and high-impedance if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 2. Reset Timing



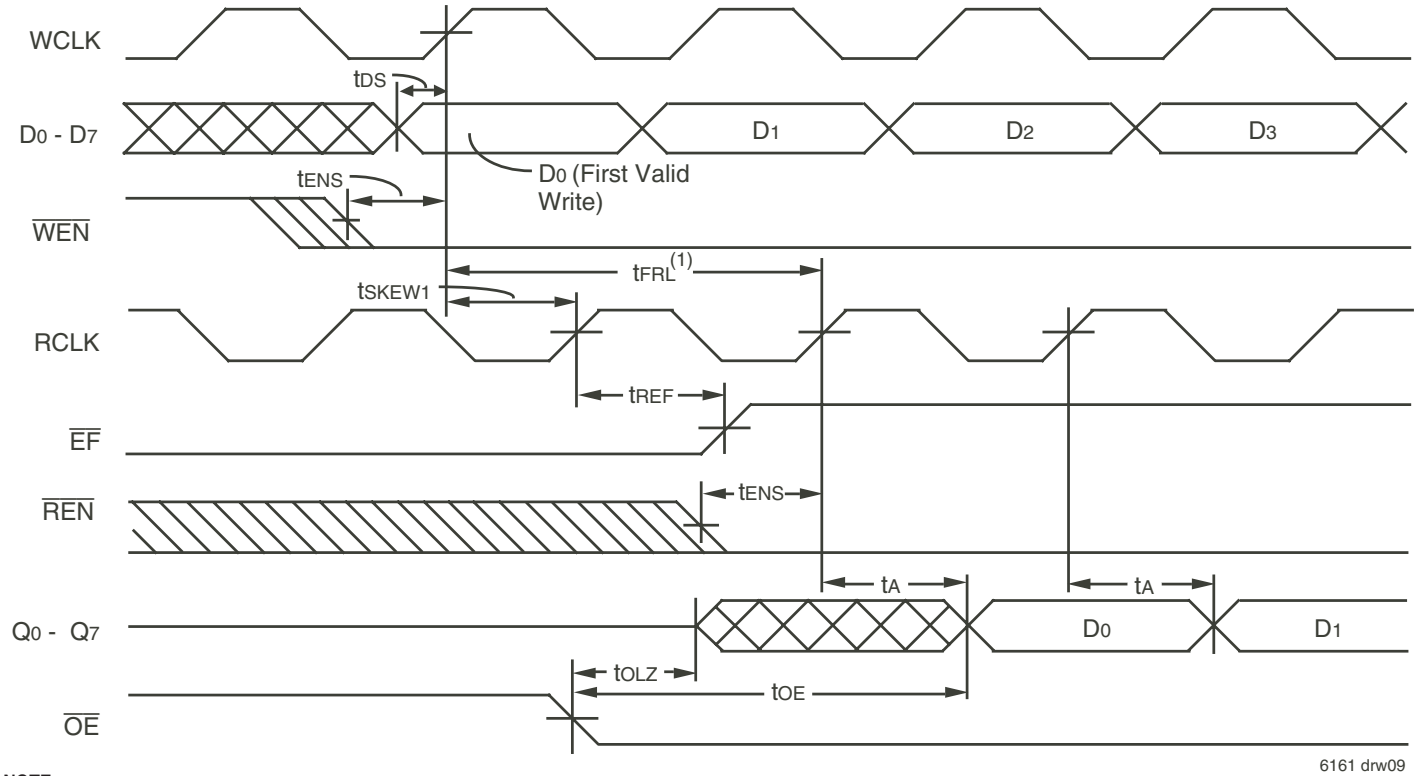
NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 3. Write Cycle Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 4. Read Cycle Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 5. First Data Word Latency Timing

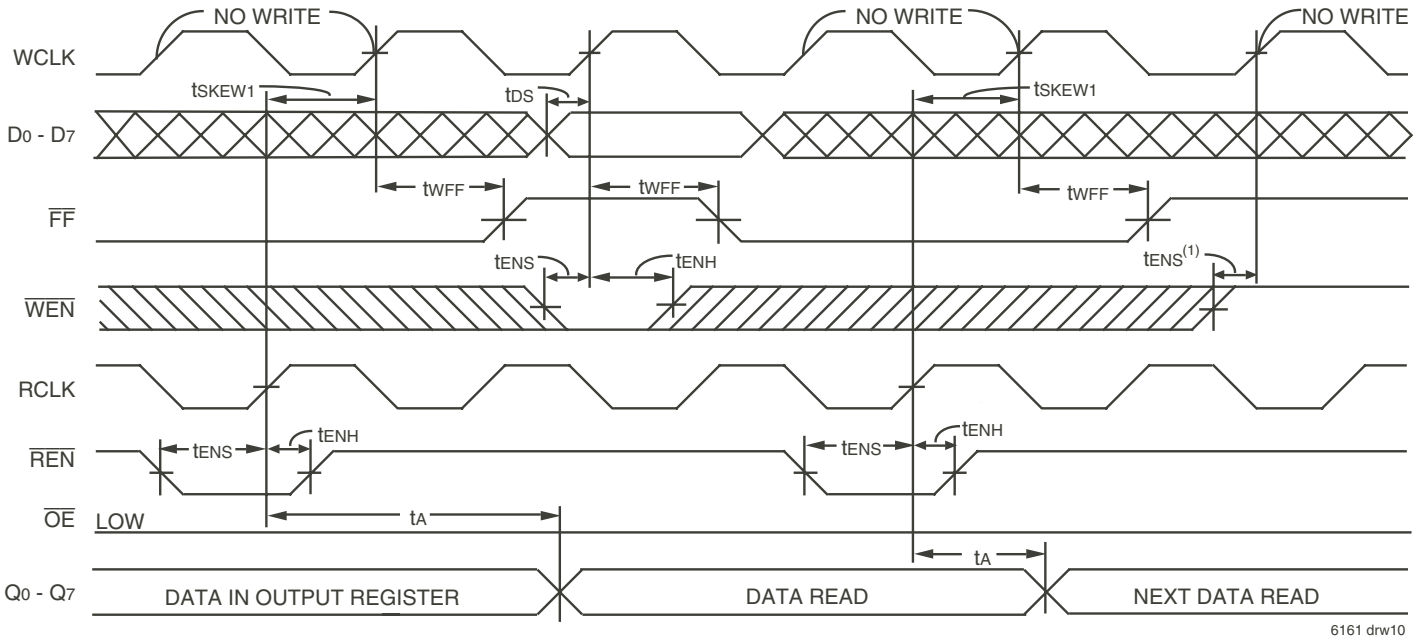
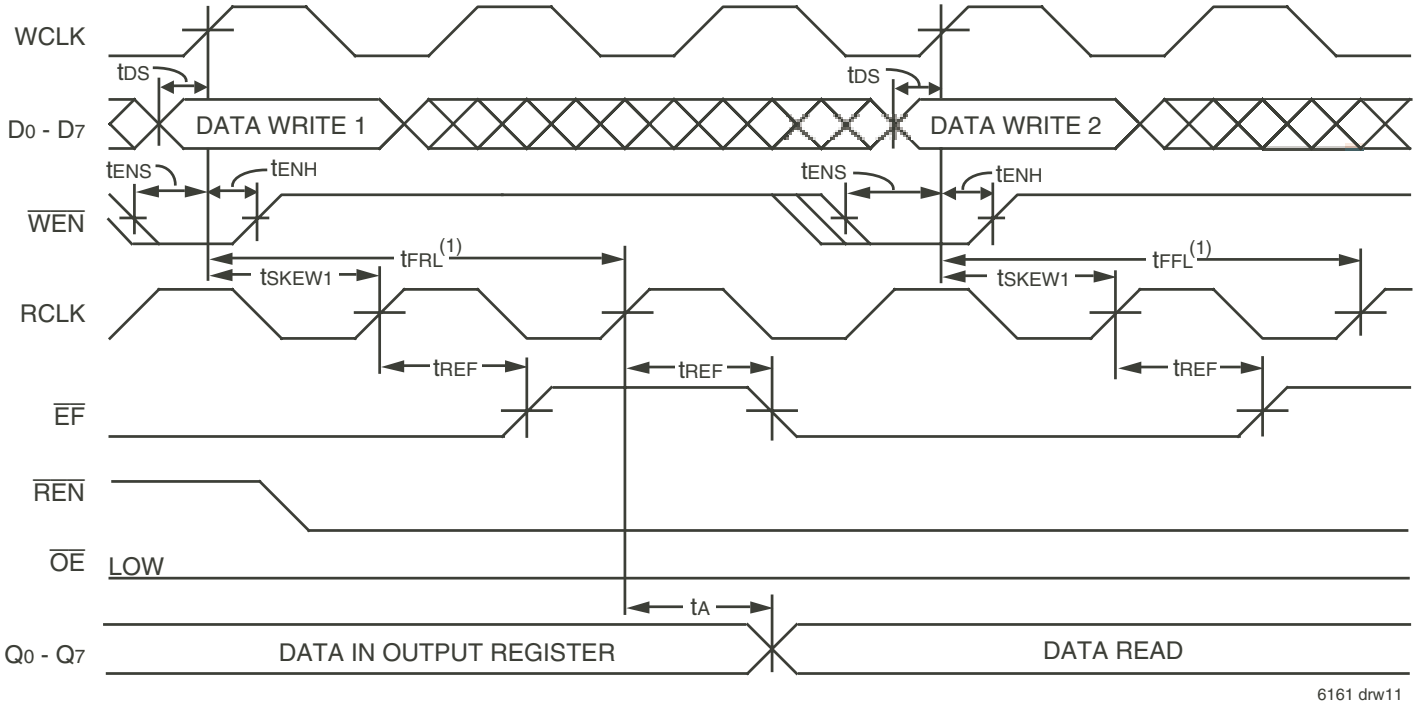


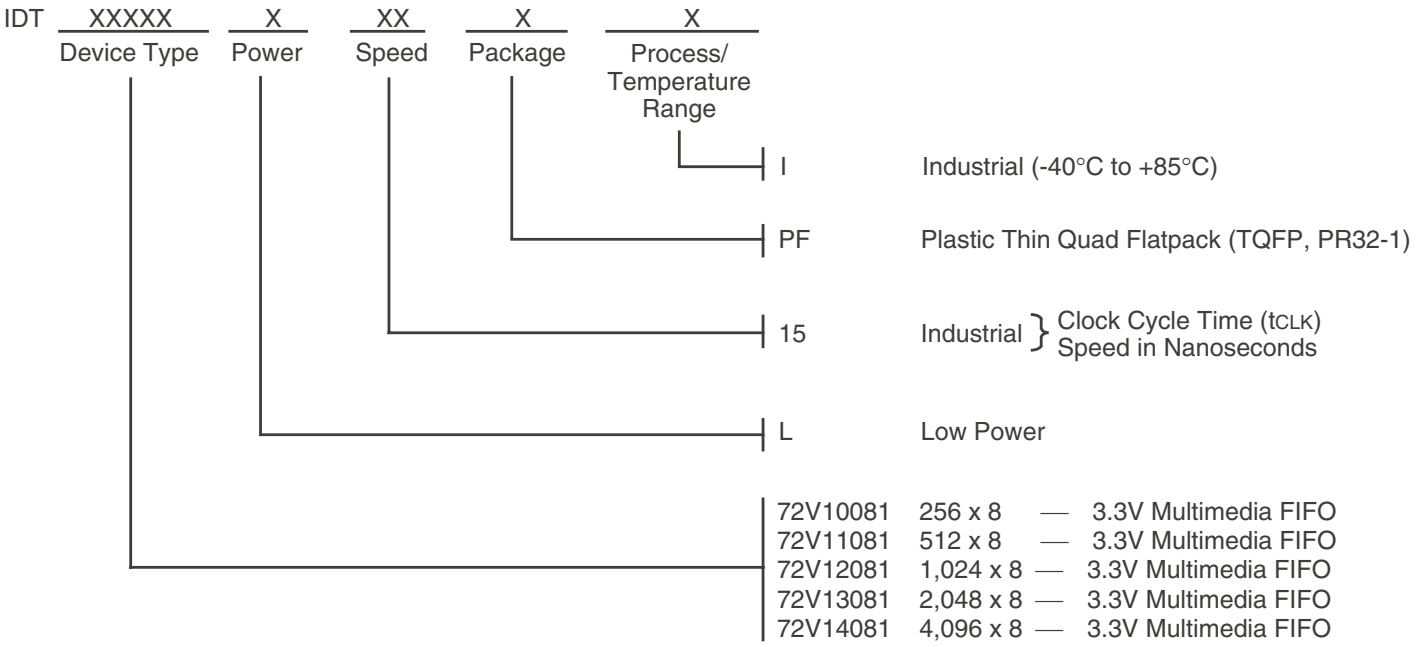
Figure 6. Full Flag Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 7. Empty Flag Timing

ORDERING INFORMATION



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