FPD33584 Low Power, Low EMI, TFT-LCD Column Driver with RSDS Inputs, 64 Grayshades, and 384 Outputs for XGA/SXGA Applications

Check for Samples: FPD33584

FEATURES

- **RSDS (Reduced Swing Differential Signaling) data bus for low power, reduced EMI and small PCB foot print**
- **85MHz maximum operating frequency at V_{DD1}=3.0V (70MHz at V_{DD1} = 2.7V)**
- **Pin compatible with Samsung S6C0666**
- **Ideal for XGA and SXGA applications**
- **Supports notebook and monitor applications**
- **Smart Charge Conservation for low power consumption**
- **64 Gray levels per color (18-bit color)**
- **Supports both Dot and N-Line inversion**
- **Four externally programmable gamma curves**
- **Low offset, High voltage outputs for high contrast in a large range of display panel applications**
- **Optional, high current, repair amplifiers**

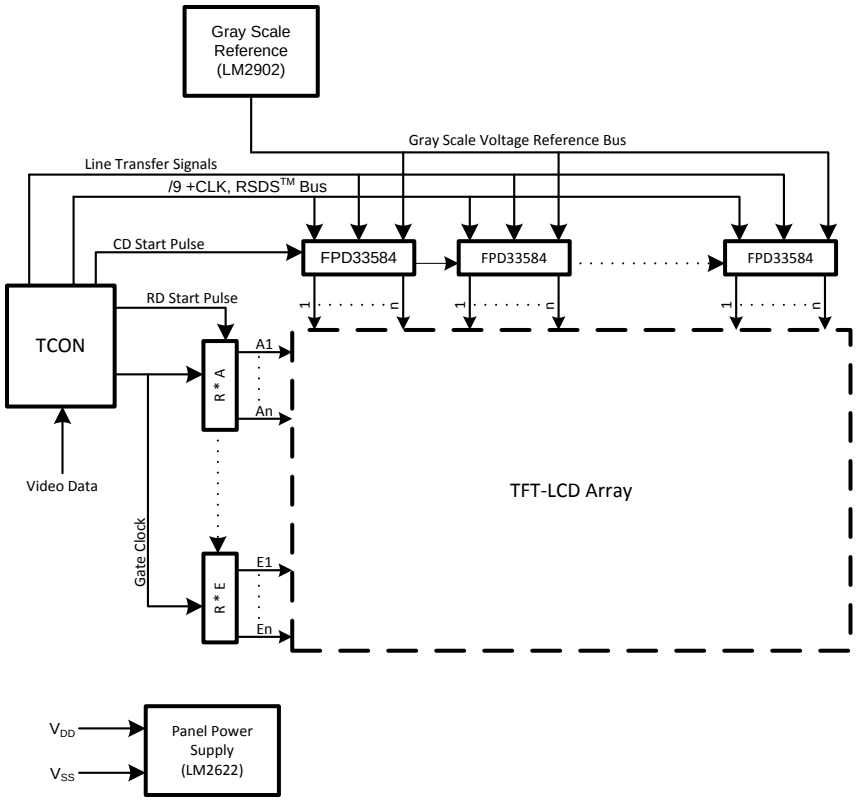
DESCRIPTION

The FPD33584 Column Driver is a direct drive, 64 gray level, 384 output, TFT-LCD column driver with an RSDS™ data interface. It provides the capability to display 262,144 colors (18-bit color) with a large dynamic output range for twisted nematic applications. When used in a bank with other FPD33584 column drivers, the FPD33584 can support XGA (8 drivers) or SXGA (10 drivers) applications. Output voltages are gamma corrected to provide a direct mapping between digital video and LCD panel brightness. The 85MHz operating frequency allows the FPD33584 to meet the requirement of high refresh rate applications (i.e. XGA monitors with a 75Hz refresh rate).

An RSDS™ (Reduced Swing Differential Signaling) interface is used between the timing controller and the column driver to minimize EMI and reduce power.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

System Diagram



Absolute Maximum Ratings (1)

Analog Supply, (V_{DD2}) (2)	−0.3V to +11.5V
Logic Supply, (V_{DD1}) (2)	−0.3V to +5.0V
Low-Polarity RDAC Reference Voltages, (V_{GMA6} to V_{GMA10}) (2)	−0.3V to 0.5V_{DD2}
High-Polarity RDAC Reference Voltages, (V_{GMA1} to V_{GMA5}) (2)	0.5V_{DD2} − 1.0V to V_{DD2} + 0.3V
RDAC Current (All Gamma Voltage Taps), (I_{GMA} to I_{GMA10})	−2.5mA to 2.5mA
Input Voltage (Digital Logic), (V_{IN}) (2)	−0.3V to V_{DD1} + 0.3V
Output Voltage, (V_{OUT}) (2)	−0.3V to V_{DD2} + 0.3V
Output Current (Analog), (I_{OUT})	−7mA to +7mA
Storage Temperature Range, (T_S)	−55°C to +125°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

(2) Absolute voltages referenced to V_{SS1} = V_{SS2} = 0.0V.

Recommended Operating Conditions

	Min	Typ	Max	Units
Logic Supply Voltage (V_{DD1})	2.7	3.3	3.6	V
Supply Voltage (V_{DD2})	7.5		10.5	V
Operating Temperature				
(T_A)	−10	+25	+70	°C

DC Electrical Characteristics

Digital Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic Input High Voltage		0.7 V_{DD1}			V
V_{IL}	Logic Input Low Voltage				0.3 V_{DD1}	V
V_{OH}	Logic Output High Voltage	I_{OH} = −0.5mA	V_{DD1} − 0.5			V
V_{OL}	Logic Output Low Voltage	I_{OL} = 0.5mA			0.5	V
I_{DD1}	Logic Current	(1)		8.0	12.0	mA
I_{IH}	Input Leakage	V_{DD1} = 3.6V, V_{IN} = 3.6V	-1		1	µA
I_{IL}	Input Leakage	V_{DD1} = 3.6V, V_{IN} = 0V	-1		1	µA
C_{IN}	Input Capacitance	All logic pins		2		pF

(1) CLK frequency = 67MHz, V_{DD1} = 3.3V, V_{SS1} = V_{SS2} = 0.0V, line time = 18µs, data = all 1's for 4 lines followed by all 0's for 4 lines.

RSDS™ Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIH_{RSDS}	RSDS High Input Voltage	VCM_{RSDS} = 1.2V (1) see Figure 1	100	200		mV
VIL_{RSDS}	RSDS Low Input Voltage	VCM_{RSDS} = 1.2V (1) see Figure 1		−200	−100	mV
VCM_{RSDS}	RSDS Common Mode Input Voltage Range	VIH_{RSDS} = +100mV, VIL_{RSDS} = −100mV (2) see Figure 1	V_{SS1} + 0.1		V_{DD1} − 1.3	V
IDL	RSDS Input Leakage Current	DxxP, DxxN, CLKP, CLKN	−10		10	µA

(1) VCM_{RSDS} = (VCLKP + VCLKN)/2 or (VDxxP + VDxxN)/2.
(2) VIH_{RSDS} and VIL_{RSDS} are referenced to $VCMR_{RSDS}$

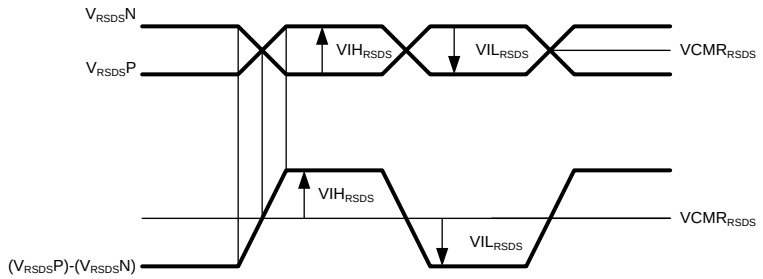


Figure 1. RSDS Signal Definition

Analog Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD2}	Supply Current Consumption	(1)		5.0	12.0	mA
V_{GMA1}	Upper RDAC High Side Input	(2)	$V_{DD2}/2$ + 0.2		V_{DD2} − 0.2	V
V_{GMA5}	Upper RDAC Low Side Input	(2)	$V_{DD2}/2$ + 0.2		V_{DD2} − 0.2	V
V_{GMA6}	Lower RDAC High Side Input	(2)	0.2		$V_{DD2}/2$ − 0.2	V
V_{GMA10}	Lower RDAC Low Side Input	(2)	0.2		$V_{DD2}/2$ − 0.2	V
C_{LOAD}	Output Capacitive Load		30		150	pF
V_{OUT}	Output Voltage Range		V_{SS2} + 0.2		V_{DD2} − 0.2	V
R_{DAC}	RDAC References (V_{GMA1} to V_{GMA5} and V_{GMA6} to V_{GMA10})	each	12.0	15.0	18.0	kΩ
V_{pperr}	Output Peak to Peak Error (gray levels 0 through 58)	$V_{GMA1} = V_{DD2}$ − TBDV $V_{GMA10} = V_{SS2}$ + TBDV (3)		±3	±12	mV
	Output Peak to Peak Error (gray levels 59 through 63)			±5	±25	mV
$V_{parterr}$	Output Part to Part Error	(4)			±5	mV
$I_{OUT\ RP}$	Repair Buffer Output Current	(5)	±2	±3		mA

(1) V_{DD2}= 10V, V_{DD1} = 3.3V, f_{CLK} = 67MHz, line time = 18µsec, data = maximum output swing (GMA1 to GMA10), [TIME1, TIME0] = [0,1] (charge sharing of 32 clock cycles

(2) The following relationship must be maintained between the reference voltages: $V_{DD2} > V_{GMA1} > V_{GMA2} > V_{GMA3} > V_{GMA4} > V_{GMA5} > V_{GMA6} > V_{GMA7} > V_{GMA8} > V_{GMA9} > V_{GMA10} > V_{SS2}$

(3) V_{pperr} is meant to reflect the error in peak-to-peak output voltage for each gray level whent the output swings from the high value VHxx to the low value VLxx. This parameter applies to every output on the die. The typical value represents one standard deviation from ideal based on tester data. The maximum value is a constraint of the test environment, not the performance of the part.

(4) $V_{parterr}$ is meant to guarantee the part-to-part output variation. The average of all outputs at gray level 32 is compared to a nominal gray level 32 value. The difference is $V_{parterr}$

(5) Current into device pins is defined as positive. Current out of device pins is defined as negative. $|V_{OUT} - V_{IN}| > 500mV$.

AC Electrical Characteristics

Digital AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PW_{CLK}	Clock Period	V_{DD1} = 2.7 to 3.0V	14			ns
PW_{CLK}	Clock Period	V_{DD1} = 3.0 to 3.6V	11.7			ns
$PW_{CLK(L)}$	Low Clock Pulse Width		40%		60%	PW_{CLK}
$PW_{CLK(H)}$	High Clock Pulse Width		40%		60%	PW_{CLK}
t_{setup1}	RSDS Data Setup Time		2			ns
t_{hold1}	RSDS Data Hold Time		0			ns
t_{setup2}	ENIOx Setup Time		2			ns
t_{hold2}	ENIOx Hold Time		2			ns
t_{PLH1}	Start Pulse Fall Delay	C_{LINE} = 15 pF			8	ns
PW_{DIO}	ENIOx Pulse Width		1		2	PW_{CLK}
PW_{CLK1}	LOAD Pulse Width		5 T_{CLK}		5µs	
t_{LDT}	Last Clock to LOAD Delay		1			PW_{CLK}
t_{DENSU}	LOAD to First ENIO Setup		2			PW_{CLK}
tPOL–CLK1	POL–CLK1 Time		14			ns

Analog AC Characteristics

Supplies: V_{SS1} = V_{SS2} = 0.0V, V_{DD1} = 3.3V, V_{DD2} = +10.0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{settle\ 90\%}$	Output Settling Time to 90% of Final Value	Figure 2 (1)			6	µs
$t_{6\text{-bit accy}}$	Output Settling Time to 6-bit accuracy	Figure 2 (1)			10	µs
$t_{RP\ 90\%}$	Repair Line Output Settling Time to 90% of Final Value	C_{LOAD} = 150 pF, (1)			6	µs
$t_{RP\ 6\text{-bit accy}}$	Repair Line Output Settling Time to 6-bit accuracy	C_{LOAD} = 150 pF, (1)			10	µs

(1) V_{GMA1} = 9.8V, V_{GMA10} = 0.2V, V_{GMA5} = 5.2V, V_{GMA6} = 4.8V, [TIME0, TIME1] = [0,1].

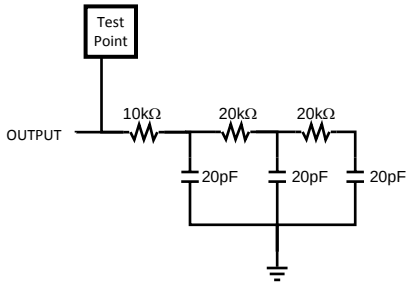
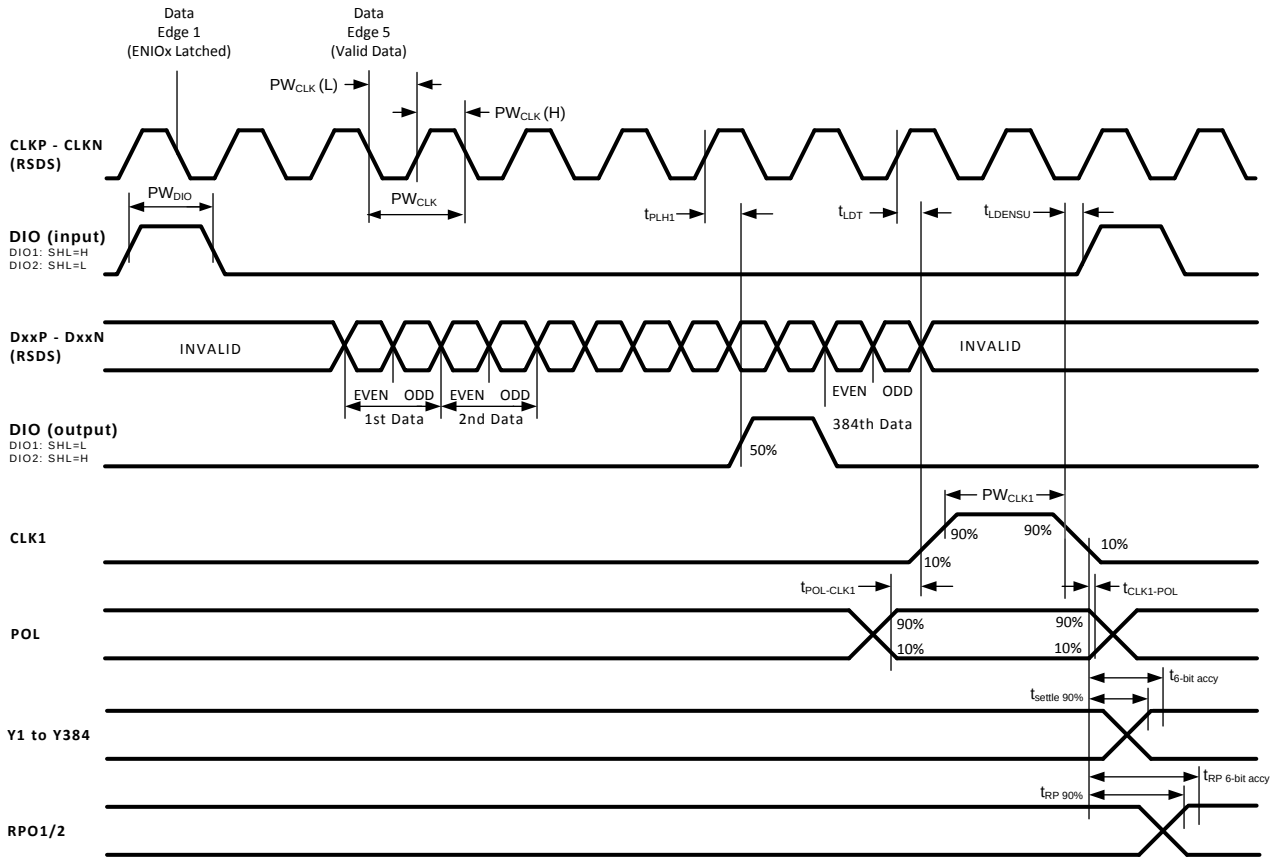
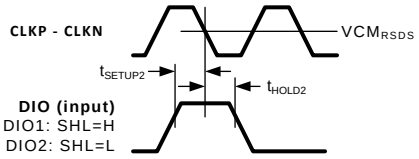
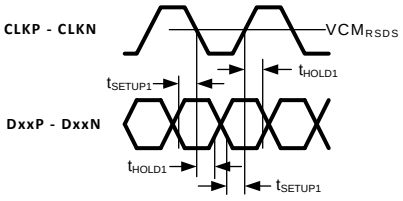


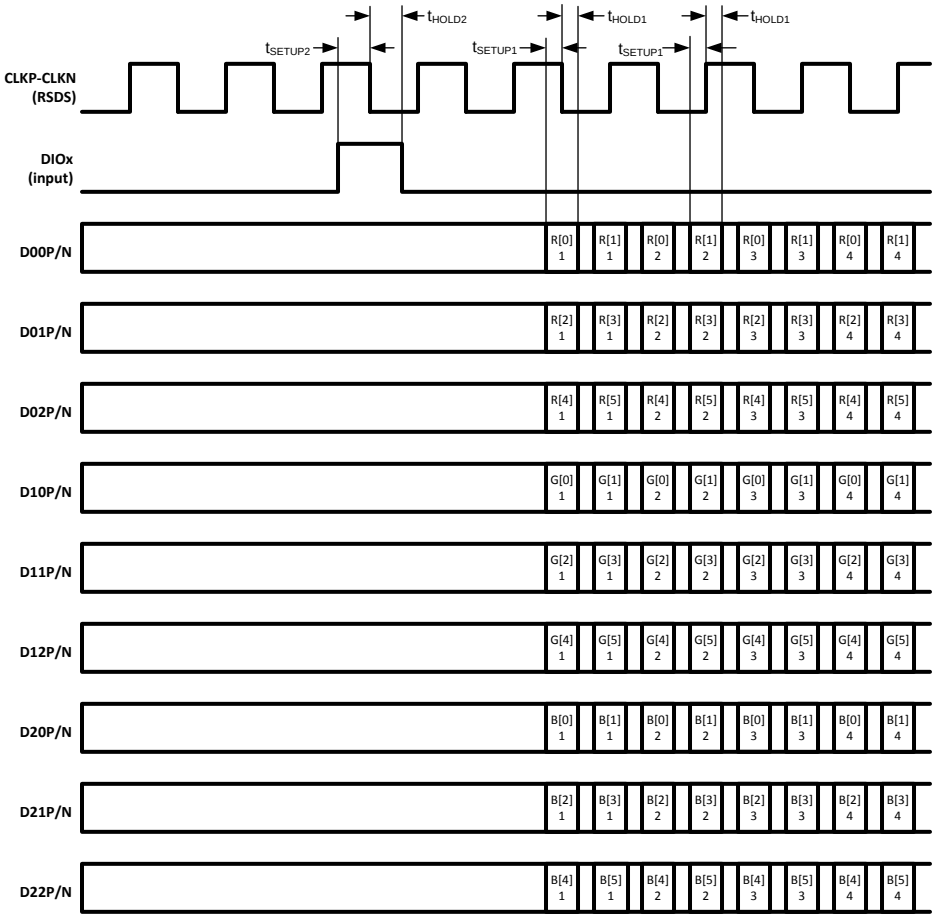
Figure 2. Test Circuit for Output Settling Time Measurements

Timing Diagrams

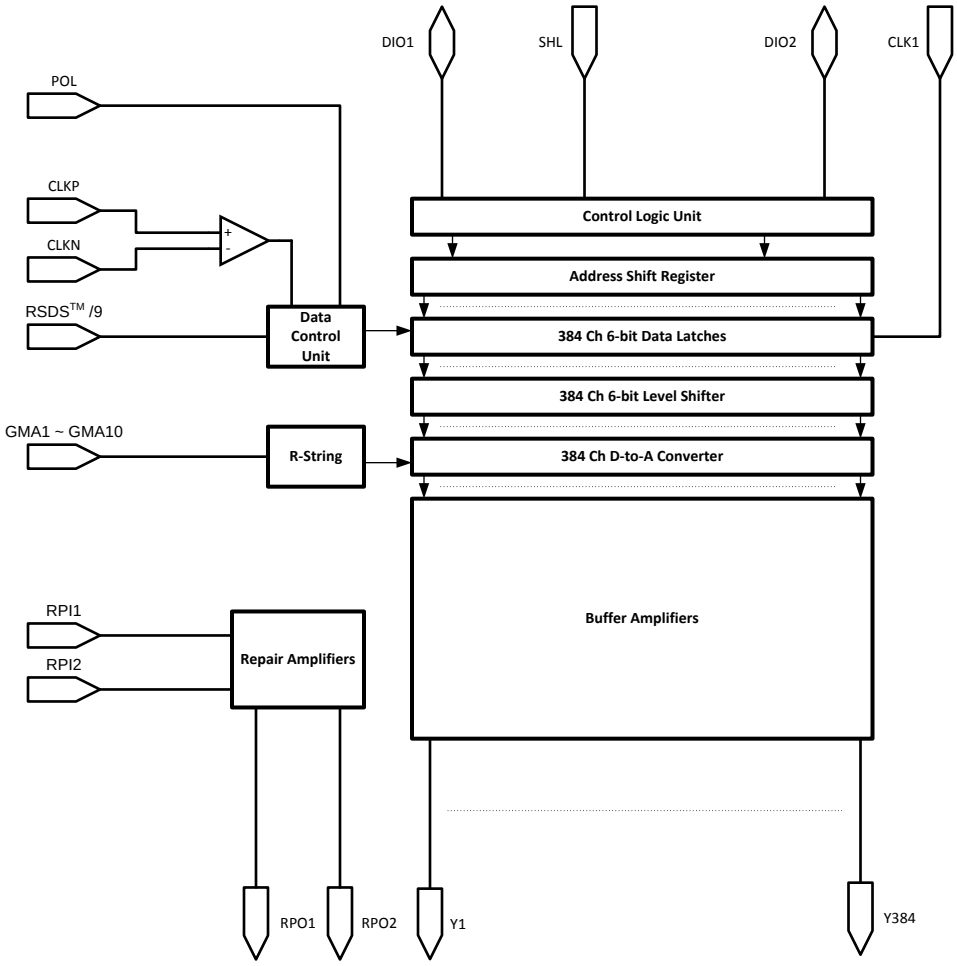








Block Diagram



Functional Description

GENERAL OVERVIEW

The FPD33584 is a low power, low EMI, 384 output column driver with 64 gray level capability (6-bit). It provides direct drive for TFT-LCD displays, eliminating the need for V_{com} modulation. Direct drive significantly reduces system power consumption and also reduces component count while providing superior image quality and cross-talk margin. The FPD33584 utilizes National's *Charge Conservation Technology* that recovers energy stored in the capacitance of the column lines to reduce power consumption further.

The FPD33584 is designed for use in systems using dot inversion as the method of polarity inversion. Column inversion and N-line inversion are also supported. Other modes of polarity inversion including line inversion and frame inversion are not supported.

Digital video data inputs to the FPD33584 are received via a low power, low EMI Reduced Swing Differential Signaling (RSDS) bus. The RSDS digital video commands one of 64 gray level voltages on each output. Output voltages are driven with individual high drive, low offset operational amplifiers. Data loading and line buffering is accomplished by means of an internal, bi-directional shift register.

GAMMA CORRECTION

The FPD33584 is designed to offer compatibility with a wide range of panel gamma characteristics. The output voltage levels corresponding to each of the 64 gray level commands can be externally adjusted to match the desired gamma characteristics of the display by means of two internal resistor-string DACs (RDACs). One RDAC provides the high-polarity output voltages (voltages higher than V_{com}) and the other provides the low-polarity output voltages (voltages lower than V_{com}).

The FPD33584 is available with several R-DAC resistance curve options, all of which have been carefully designed to accurately match the natural, inverse gamma of a twisted nematic (TN) display with a 2.2 gamma transfer characteristic. Additional, custom gamma curves can be requested through your National Semiconductor representative. A typical TN display, when operated with the FPD33584 drivers will produce a luminance with grayscale characteristic typical of CRT monitors. The resistor values for all R-DACs are shown in Table 14. The individual R-DAC characteristics can be found in:

- Gamma A— Figure 4, Table 2, and Table 3
- Gamma B— Figure 5, Table 4, and Table 5
- Gamma C— Figure 6, Table 8, and Table 7
- Gamma D— Figure 7, Table 9, and Table 9
- Gamma F— Figure 8, Table 10, and Table 11
- Gamma G— Figure 9, Table 12, and Table 13

Most applications will only need to provide references for each of the two ends of the two R-DACs (GMA1, GMA5, GMA6, and GMA10). Six additional, intemediate R-DAC tap points are available for further customization.

CHARGE CONSERVATION TECHNOLOGY

National Semiconductor's proprietary charge conservation technology significantly reduces power consumption. Charge conservation works by briefly switching all of the columns to a common node at the start of each line. This has the effect of redistributing the charge stored in the capacitance of the panel columns. Because half the columns are at voltages more positive than V_{com} and half are more negative, this redistribution of charge or “charge-sharing” has the effect of pulling all of the columns to a neutral voltage near the middle of the driver's dynamic range. Thus, the voltages on all the columns are driven approximately halfway toward their next value with no power expended. This dramatically reduces panel power dissipation (up to a theoretical limit of 50%) compared to conventional drivers which must drive each column through the entire voltage swing every time polarity is reversed.

’Smart’ charge sharing is used to further optimize this feature. Data inversion is monitored and charge shared only across data ranges (when output polarity changes between adjacent lines). This is useful during n-line inversion when polarity changes do not occur at every line transition.

Table 1. Charge Sharing Definition

TIME0	TIME1	Charge Share Time
0	0	16 RSDS CLKs (approx. 250ns @ 65MHz)
0	1	32 RSDS CLKs (approx. 500ns @ 65MHz)
1	0	64 RSDS CLKs (approx. 1µs @ 65MHz)
1	1	128 RSDS CLKs (approx. 2µs @ 65MHz)

As shown in Figure 3, charge sharing begins at the falling edge of CLK1 and continues for the number or RSDS clock cycles shown in Table 1. For more information on National’s proprietary Smart Charge Sharing technology, please see application note *AN1235 Using Smart Charge Sharing to Reduce Power and Boost Column Driver Performance*, which is available on the National Semiconductor website or through your National Semiconductor representative.

The amount of charge share time is determined by 2 pins: TIME0 and TIME1. Both TIME0 and TIME1 pins default to a low state, so if both pins are left floating, the charge share time will be 16 RSDS clock cycles. For most applications, one of the charge share times defined by TIME0 and TIME1 will optimize the performance and power savings in the panel. Generally, the average panel should set charge sharing at either 32 RSDS clocks or 64 RSDS clocks, depending on the data rate and the panel load. Panels with much larger RC loads may need to increase the charge share time to get the maximum benefit and panels with a smaller load can realize power savings with a shorter charge share time. Please contact National Semiconductor if you need further assistance in selecting a charge share time.

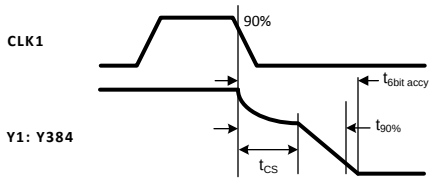


Figure 3. FPD33584 Charge Share Timing

RSDS DATA CHANNEL

The RSDS data bus is comprised of nine channels and a common clock. Each channel consists of a two wire differential pair. The nine channels carry digital video data organized as three busses of three channels. Each three channel bus corresponds on one of the three video colors, red, green and blue. The three video busses are comprised of a most, middle and least significant bit. The six bit video word is carried on the three wires of each video bus in two consecutive half words. The even fields of the word are transmitted-received on a first clock and are followed by the odd fields on the following clock transition. Clocking is dual edge and the clock signal is also carried on a two wire, differential pair.

OPTIONAL REPAIR AMPLIFIERS

The FPD33584 provides two general purpose, unity gain output buffers, one located at each end of the input bank of the die. These buffers may be used to repair an open in a column line. The drive signal from the output of the faulted line can be stitched to the input of the repair buffer during the repair process. The output of the repair buffer is then routed to the other side of the column line making it possible to maintain fast rise and fall times on both ends of the afflicted column line.

PIN DESCRIPTIONS

The pin order configuration for the FPD33584 is shown in Table 15

CLKP and CLKN—*Data Clock (input)*

Differential clock input for RSDS data loading.

D00P–D22N—*RSDS Data Bus (input)*

D0xP–D0xN—Data for OUTPUTS 1,4,7...382 (red)

D1xP–D1xN—Data for OUTPUTS 2,5,8...383 (green)

D2xP–D2xN—Data for OUTPUTS 3,6,9...384 (blue)

Where x = 0 (LSB), 1 or 2 (MSB).

CLK1—*Data Load (input)*

The rising edge of CLK1 copies the digital video buffered by the shift register into a second latch for conversion to analog. The falling edge of CLK1 begins charge sharing.

POL—*Polarity (input)*

When POL is low, odd numbered outputs (1, 3, 5, . . . 383) are controlled by VGMA6 through VGMA10 and even numbered outputs are controlled by VGMA1 through VGMA5. When POL is high, odd numbered outputs are controlled by VGMA1 through VGMA5 and even numbered outputs are controlled by VGMA6 through VGMA10. The POL signal for line #n is sampled at the rising edge of CLK1 on line #n−1.

DIO1/DIO2—*Data Loading Enable 1 and 2 (I/O)*

The DIO1 and DIO2 pins allow several FPD33584 column drivers to be daisy chained together. The start pulse (SP or STH) from the timing controller is connected to the input DIOx pin on the first column driver in the chain. The input DIO for the remaining column drivers in the chain are connected to the output DIO from the preceding column driver. The SHL pin controls whether DIO1 or DIO2 is configured as the input.

If SHL is high, then the DIO1 pin is configured as an input and the DIO2 pin as an output. If SHL is low, the DIO2 pin is configured as an input and the DIO1 pin as an output.

The input DIOx pulse is latched on the falling edge of CLKP

DATPOL—*Digital Data Invert (input)*

When DATPOL is high, RSDS data is inverted. The DATPOL pin can be tied either high or low through connection to a neighboring pin on a custom package eliminating the need to connect the pin to the PCB.

SHL—*Data Shift Direction (input)*

The SHL pin controls the data load direction. When SHL is high, the data is loaded from output 1 to output 384, DIO1 is configured as an input, and DIO2 is configured as an output. When SHL is low, the data is loaded from output 384 to output 1, DIO2 is configured as an input, and DIO1 is configured as an output. The SHL pin can be tied off in the custom package, eliminating the need to connect it to the PCB.

RPI1/ RPI2—*Repair Amp Input 1 and 2 (input)*

The input signal for the repair line buffers. These buffers are optional and when not used, the input should be tied to ground. RPI1 and RPI2 can be tied to ground with a connection in the package, eliminating the need to connect them to the PCB.

RPO1/ RPO2—*Repair Amp Output 1 and 2 (output)*

The output of the repair line buffers. These outputs are current buffered copies of their respective inputs. When not in use, RPO1 and RPO2 can be left unconnected.

TIME0/ TIME1—*Charge Share Time Select Pins (input)*

The TIME0 and TIME1 pins define the length of charge share time. Table 1 lists the charge share time options defined by TIME0 and TIME1. Both of these pins have internal pull-down resistors and default to a logic low state. They can also be tied high in the package, eliminating the need to connect them to the PCB.

V_{GMA1}–V_{GMA10}—*RDAC References (input)*

The reference voltages to the upper and lower RDACs used to control the inverse gamma transfer function of the driver.

Option - Any or all of the inputs V_{GMA2} through V_{GMA4} and V_{GMA7} through V_{GMA9} can be left undriven (floating).

V_{DD1}—*Digital Voltage Supply (power)*

Positive supply voltage for the digital logic functions of the driver. Nominally 3.3V.

V_{DD2}—*Analog Voltage Supply (power)*

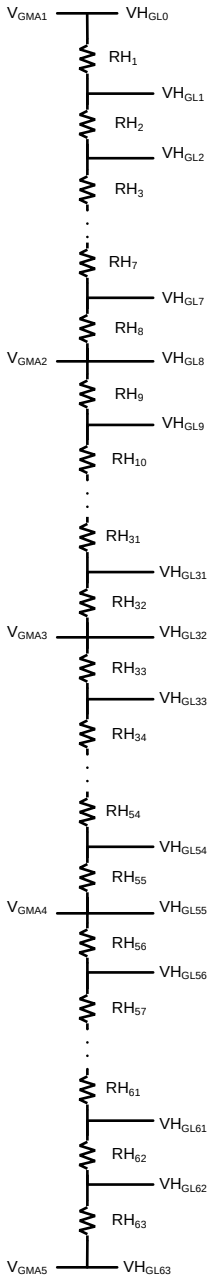
Positive supply voltage for the analog functions of the driver. Nominally between 8.0 and 10.0V

V_{SS1}—*Digital Ground (power)*

Digital ground reference voltage. Typically tied to V_{SS2} on the PCB.

V_{SS2}—*Analog Ground (power)*

Analog ground reference voltage. Typically tied to V_{SS1} on the PCB



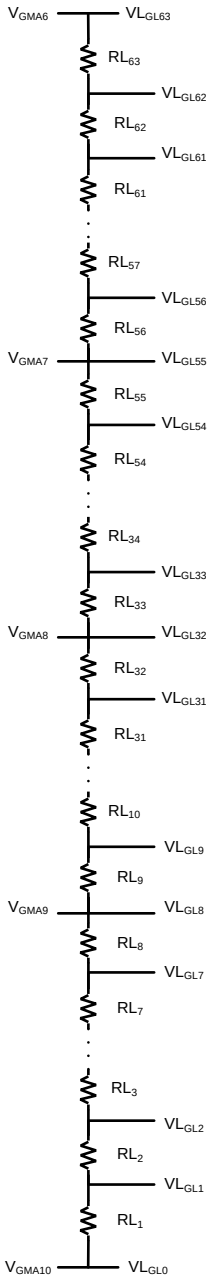


Figure 4. FPD33584A R-DAC Configuration

Table 2. FPD33584A Lower Gamma Voltages

Data	Output Voltage (gamma A)			Data	Output Voltage (gamma A)		
00_H	VL0	VGMA10		**20_H**	VL32	VGMA8	
01_H	VL1	VGMA9−(VGMA9−VGMA10)×	4049/5879	**21_H**	VL33	VGMA7−(VGMA7−VGMA8)×	2588/2692
02_H	VL2	VGMA9−(VGMA9−VGMA10)×	3022/5879	**22_H**	VL34	VGMA7−(VGMA7−VGMA8)×	2484/2692
03_H	VL3	VGMA9−(VGMA9−VGMA10)×	2293/5879	**23_H**	VL35	VGMA7−(VGMA7−VGMA8)×	2380/2692

Table 2. FPD33584A Lower Gamma Voltages (continued)

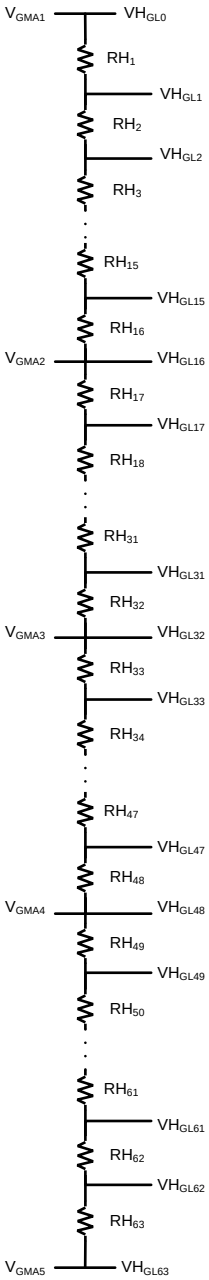
Data	Output Voltage (gamma A)			Data	Output Voltage (gamma A)		
04_H	VL4	VGMA9−(VGMA9−VGMA10)×	1668/5879	**24_H**	VL36	VGMA7−(VGMA7−VGMA8)×	2276/2692
05_H	VL5	VGMA9−(VGMA9−VGMA10)×	1147/5879	**25_H**	VL37	VGMA7−(VGMA7−VGMA8)×	2172/2692
06_H	VL6	VGMA9−(VGMA9−VGMA10)×	730/5879	**26_H**	VL38	VGMA7−(VGMA7−VGMA8)×	2068/2692
07_H	VL7	VGMA9−(VGMA9−VGMA10)×	313/5879	**27_H**	VL39	VGMA7−(VGMA7−VGMA8)×	1964/2692
08_H	VL8	GMA9		**28_H**	VL40	VGMA7−(VGMA7−VGMA8)×	1860/2692
09_H	VL9	VGMA8−(VGMA8−VGMA9)×	2825/3138	**29_H**	VL41	VGMA7−(VGMA7−VGMA8)×	1756/2692
$0A_H$	VL10	VGMA8−(VGMA8−VGMA9)×	2617/3138	**$2A_H$**	VL42	VGMA7−(VGMA7−VGMA8)×	1652/2692
$0B_H$	VL11	VGMA8−(VGMA8−VGMA9)×	2409/3138	**$2B_H$**	VL43	VGMA7−(VGMA7−VGMA8)×	1548/2692
$0C_H$	VL12	VGMA8−(VGMA8−VGMA9)×	2260/3138	**$2C_H$**	VL44	VGMA7−(VGMA7−VGMA8)×	1429/2692
$0D_H$	VL13	VGMA8−(VGMA8−VGMA9)×	2111/3138	**$2D_H$**	VL45	VGMA7−(VGMA7−VGMA8)×	1310/2692
$0E_H$	VL14	VGMA8−(VGMA8−VGMA9)×	1977/3138	**$2E_H$**	VL46	VGMA7−(VGMA7−VGMA8)×	1191/2692
$0F_H$	VL15	VGMA8−(VGMA8−VGMA9)×	1843/3138	**$2F_H$**	VL47	VGMA7−(VGMA7−VGMA8)×	1072/2692
10_H	VL16	VGMA8−(VGMA8−VGMA9)×	1724/3138	**30_H**	VL48	VGMA7−(VGMA7−VGMA8)×	953/2692
11_H	VL17	VGMA8−(VGMA8−VGMA9)×	1605/3138	**31_H**	VL49	VGMA7−(VGMA7−VGMA8)×	834/2692
12_H	VL18	VGMA8−(VGMA8−VGMA9)×	1486/3138	**32_H**	VL50	VGMA7−(VGMA7−VGMA8)×	715/2692
13_H	VL19	VGMA8−(VGMA8−VGMA9)×	1367/3138	**33_H**	VL51	VGMA7−(VGMA7−VGMA8)×	581/2692
14_H	VL20	VGMA8−(VGMA8−VGMA9)×	1248/3138	**34_H**	VL52	VGMA7−(VGMA7−VGMA8)×	447/2692
15_H	VL21	VGMA8−(VGMA8−VGMA9)×	1144/3138	**35_H**	VL53	VGMA7−(VGMA7−VGMA8)×	298/2692
16_H	VL22	VGMA8−(VGMA8−VGMA9)×	1040/3138	**36_H**	VL54	VGMA7−(VGMA7−VGMA8)×	149/2692
17_H	VL23	VGMA8−(VGMA8−VGMA9)×	936/3138	**37_H**	VL55	VGMA7	
18_H	VL24	VGMA8−(VGMA8−VGMA9)×	832/3138	**38_H**	VL56	VGMA6−(VGMA6−VGMA7)×	3140/3289
19_H	VL25	VGMA8−(VGMA8−VGMA9)×	728/3138	**39_H**	VL57	VGMA6−(VGMA6−VGMA7)×	2947/3289
$1A_H$	VL26	VGMA8−(VGMA8−VGMA9)×	624/3138	**$3A_H$**	VL58	VGMA6−(VGMA6−VGMA7)×	2724/3289
$1B_H$	VL27	VGMA8−(VGMA8−VGMA9)×	520/3138	**$3B_H$**	VL59	VGMA6−(VGMA6−VGMA7)×	2471/3289
$1C_H$	VL28	VGMA8−(VGMA8−VGMA9)×	416/3138	**$3C_H$**	VL60	VGMA6−(VGMA6−VGMA7)×	2158/3289
$1D_H$	VL29	VGMA8−(VGMA8−VGMA9)×	312/3138	**$3D_H$**	VL61	VGMA6−(VGMA6−VGMA7)×	1637/3289
$1E_H$	VL30	VGMA8−(VGMA8−VGMA9)×	208/3138	**$3E_H$**	VL62	VGMA6−(VGMA6−VGMA7)×	923/3289
$1F_H$	VL31	VGMA8−(VGMA8−VGMA9)×	104/3138	**$3F_H$**	VL63	VGMA6	

Table 3. FPD33584A Upper Gamma Voltages

Data	Output Voltage (gamma A)			Data	Output Voltage (gamma A)		
00_H	VH0	VGMA1		20_H	VH32	VGMA3	
01_H	VH1	VGMA2+(VGMA1−VGMA2)×	4049/5879	21_H	VH33	VGMA4+(VGMA3−VGMA4)×	2588/2692
02_H	VH2	VGMA2+(VGMA1−VGMA2)×	3022/5879	22_H	VH34	VGMA4+(VGMA3−VGMA4)×	2484/2692
03_H	VH3	VGMA2+(VGMA1−VGMA2)×	2293/5879	23_H	VH35	VGMA4+(VGMA3−VGMA4)×	2380/2692
04_H	VH4	VGMA2+(VGMA1−VGMA2)×	1668/5879	24_H	VH36	VGMA4+(VGMA3−VGMA4)×	2276/2692
05_H	VH5	VGMA2+(VGMA1−VGMA2)×	1147/5879	25_H	VH37	VGMA4+(VGMA3−VGMA4)×	2172/2692
06_H	VH6	VGMA2+(VGMA1−VGMA2)×	730/5879	26_H	VH38	VGMA4+(VGMA3−VGMA4)×	2068/2692
07_H	VH7	VGMA2+(VGMA1−VGMA2)×	313/5879	27_H	VH39	VGMA4+(VGMA3−VGMA4)×	1964/2692
08_H	VH8	GMA2		28_H	VH40	VGMA4+(VGMA3−VGMA4)×	1860/2692
09_H	VH9	VGMA3+(VGMA2−VGMA3)×	2825/3138	29_H	VH41	VGMA4+(VGMA3−VGMA4)×	1756/2692
$0A_H$	VH10	VGMA3+(VGMA2−VGMA3)×	2617/3138	$2A_H$	VH42	VGMA4+(VGMA3−VGMA4)×	1652/2692
$0B_H$	VH11	VGMA3+(VGMA2−VGMA3)×	2409/3138	$2B_H$	VH43	VGMA4+(VGMA3−VGMA4)×	1548/2692
$0C_H$	VH12	VGMA3+(VGMA2−VGMA3)×	2260/3138	$2C_H$	VH44	VGMA4+(VGMA3−VGMA4)×	1429/2692
$0D_H$	VH13	VGMA3+(VGMA2−VGMA3)×	2111/3138	$2D_H$	VH45	VGMA4+(VGMA3−VGMA4)×	1310/2692
$0E_H$	VH14	VGMA3+(VGMA2−VGMA3)×	1977/3138	$2E_H$	VH46	VGMA4+(VGMA3−VGMA4)×	1191/2692
$0F_H$	VH15	VGMA3+(VGMA2−VGMA3)×	1843/3138	$2F_H$	VH47	VGMA4+(VGMA3−VGMA4)×	1072/2692
10_H	VH16	VGMA3+(VGMA2−VGMA3)×	1724/3138	30_H	VH48	VGMA4+(VGMA3−VGMA4)×	953/2692
11_H	VH17	VGMA3+(VGMA2−VGMA3)×	1605/3138	31_H	VH49	VGMA4+(VGMA3−VGMA4)×	834/2692
12_H	VH18	VGMA3+(VGMA2−VGMA3)×	1486/3138	32_H	VH50	VGMA4+(VGMA3−VGMA4)×	715/2692
13_H	VH19	VGMA3+(VGMA2−VGMA3)×	1367/3138	33_H	VH51	VGMA4+(VGMA3−VGMA4)×	581/2692
14_H	VH20	VGMA3+(VGMA2−VGMA3)×	1248/3138	34_H	VH52	VGMA4+(VGMA3−VGMA4)×	447/2692
15_H	VH21	VGMA3+(VGMA2−VGMA3)×	1144/3138	35_H	VH53	VGMA4+(VGMA3−VGMA4)×	298/2692
16_H	VH22	VGMA3+(VGMA2−VGMA3)×	1040/3138	36_H	VH54	VGMA4+(VGMA3−VGMA4)×	149/2692
17_H	VH23	VGMA3+(VGMA2−VGMA3)×	936/3138	37_H	VH55	VGMA4	
18_H	VH24	VGMA3+(VGMA2−VGMA3)×	832/3138	38_H	VH56	VGMA5+(VGMA4−VGMA5)×	3140/3289
19_H	VH25	VGMA3+(VGMA2−VGMA3)×	728/3138	39_H	VH57	VGMA5+(VGMA4−VGMA5)×	2947/3289
$1A_H$	VH26	VGMA3+(VGMA2−VGMA3)×	624/3138	$3A_H$	VH58	VGMA5+(VGMA4−VGMA5)×	2724/3289
$1B_H$	VH27	VGMA3+(VGMA2−VGMA3)×	520/3138	$3B_H$	VH59	VGMA5+(VGMA4−VGMA5)×	2471/3289

Table 3. FPD33584A Upper Gamma Voltages (continued)

Data	Output Voltage (gamma A)			Data	Output Voltage (gamma A)		
$1C_H$	VH28	VGMA3+(VGMA2−VGMA3)×	416/3138	**$3C_H$**	VH60	VGMA5+(VGMA4−VGMA5)×	2158/3289
$1D_H$	VH29	VGMA3+(VGMA2−VGMA3)×	312/3138	**$3D_H$**	VH61	VGMA5+(VGMA4−VGMA5)×	1637/3289
$1E_H$	VH30	VGMA3+(VGMA2−VGMA3)×	208/3138	**$3E_H$**	VH62	VGMA5+(VGMA4−VGMA5)×	923/3289
$1F_H$	VH31	VGMA3+(VGMA2−VGMA3)×	104/3138	**$3F_H$**	VH63	VGMA5	



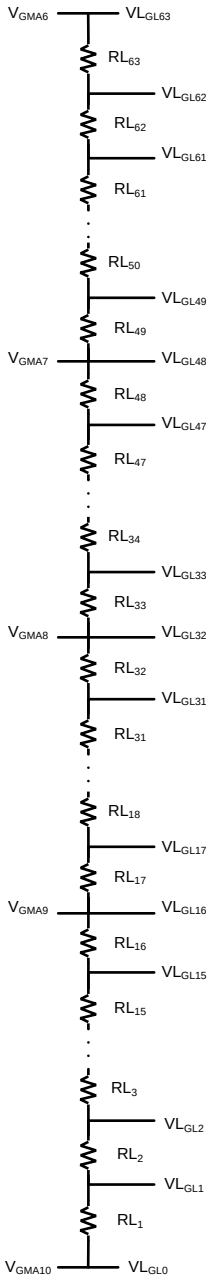


Figure 5. FPD33584B R-DAC Configuration

Table 4. FPD33584B Lower Gamma Voltages (compatible with Samsung S6C0666)

Data	Output Voltage (gamma B)			Data	Output Voltage (gamma B)		
00_H	VL0	VGMA10		**20_H**	VL32	VGMA8	
01_H	VL1	VGMA9−(VGMA9−VGMA10)×	5747/6149	**21_H**	VL33	VGMA7−(VGMA7−VGMA8)×	2040/2174
02_H	VL2	VGMA9−(VGMA9−VGMA10)×	5345/6149	**22_H**	VL34	VGMA7−(VGMA7−VGMA8)×	1906/2174
03_H	VL3	VGMA9−(VGMA9−VGMA10)×	4943/6149	**23_H**	VL35	VGMA7−(VGMA7−VGMA8)×	1772/2174

Table 4. FPD33584B Lower Gamma Voltages (compatible with Samsung S6C0666) (continued)

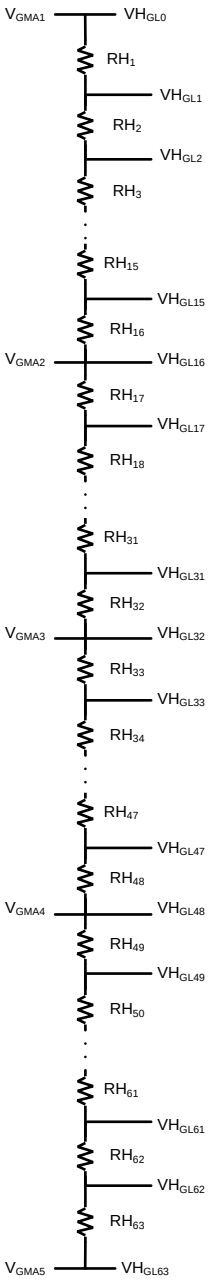
Data	Output Voltage (gamma B)			Data	Output Voltage (gamma B)		
04_H	VL4	VGMA9−(VGMA9−VGMA10)×	4541/6149	**24_H**	VL36	VGMA7−(VGMA7−VGMA8)×	1638/2174
05_H	VL5	VGMA9−(VGMA9−VGMA10)×	4139/6149	**25_H**	VL37	VGMA7−(VGMA7−VGMA8)×	1504/2174
06_H	VL6	VGMA9−(VGMA9−VGMA10)×	3737/6149	**26_H**	VL38	VGMA7−(VGMA7−VGMA8)×	1370/2174
07_H	VL7	VGMA9−(VGMA9−VGMA10)×	3335/6149	**27_H**	VL39	VGMA7−(VGMA7−VGMA8)×	1236/2174
08_H	VL8	VGMA9−(VGMA9−VGMA10)×	2933/6149	**28_H**	VL40	VGMA7−(VGMA7−VGMA8)×	1102/2174
09_H	VL9	VGMA9−(VGMA9−VGMA10)×	2531/6149	**29_H**	VL41	VGMA7−(VGMA7−VGMA8)×	968/2174
$0A_H$	VL10	VGMA9−(VGMA9−VGMA10)×	2129/6149	**$2A_H$**	VL42	VGMA7−(VGMA7−VGMA8)×	834/2174
$0B_H$	VL11	VGMA9−(VGMA9−VGMA10)×	1727/6149	**$2B_H$**	VL43	VGMA7−(VGMA7−VGMA8)×	700/2174
$0C_H$	VL12	VGMA9−(VGMA9−VGMA10)×	1325/6149	**$2C_H$**	VL44	VGMA7−(VGMA7−VGMA8)×	566/2174
$0D_H$	VL13	VGMA9−(VGMA9−VGMA10)×	968/6149	**$2D_H$**	VL45	VGMA7−(VGMA7−VGMA8)×	432/2174
$0E_H$	VL14	VGMA9−(VGMA9−VGMA10)×	611/6149	**$2E_H$**	VL46	VGMA7−(VGMA7−VGMA8)×	298/2174
$0F_H$	VL15	VGMA9−(VGMA9−VGMA10)×	298/6149	**$2F_H$**	VL47	VGMA7−(VGMA7−VGMA8)×	149/2174
10_H	VL16	VGMA9		**30_H**	VL48	VGMA7	
11_H	VL17	VGMA8−(VGMA8−VGMA9)×	3036/3304	**31_H**	VL49	VGMA6−(VGMA6−VGMA7)×	3214/3378
12_H	VL18	VGMA8−(VGMA8−VGMA9)×	2768/3304	**32_H**	VL50	VGMA6−(VGMA6−VGMA7)×	3035/3378
13_H	VL19	VGMA8−(VGMA8−VGMA9)×	2500/3304	**33_H**	VL51	VGMA6−(VGMA6−VGMA7)×	2856/3378
14_H	VL20	VGMA8−(VGMA8−VGMA9)×	2247/3304	**34_H**	VL52	VGMA6−(VGMA6−VGMA7)×	2663/3378
15_H	VL21	VGMA8−(VGMA8−VGMA9)×	2009/3304	**35_H**	VL53	VGMA6−(VGMA6−VGMA7)×	2470/3378
16_H	VL22	VGMA8−(VGMA8−VGMA9)×	1786/3304	**36_H**	VL54	VGMA6−(VGMA6−VGMA7)×	2262/3378
17_H	VL23	VGMA8−(VGMA8−VGMA9)×	1578/3304	**37_H**	VL55	VGMA6−(VGMA6−VGMA7)×	2054/3378
18_H	VL24	VGMA8−(VGMA8−VGMA9)×	1177/3304	**38_H**	VL56	VGMA6−(VGMA6−VGMA7)×	1816/3378
19_H	VL25	VGMA8−(VGMA8−VGMA9)×	984/3304	**39_H**	VL57	VGMA6−(VGMA6−VGMA7)×	1578/3378
$1A_H$	VL26	VGMA8−(VGMA8−VGMA9)×	805/3304	**$3A_H$**	VL58	VGMA6−(VGMA6−VGMA7)×	1325/3378
$1B_H$	VL27	VGMA8−(VGMA8−VGMA9)×	626/3304	**$3B_H$**	VL59	VGMA6−(VGMA6−VGMA7)×	1072/3378
$1C_H$	VL28	VGMA8−(VGMA8−VGMA9)×	462/3304	**$3C_H$**	VL60	VGMA6−(VGMA6−VGMA7)×	804/3378
$1D_H$ $1D_H$	VL29	VGMA8−(VGMA8−VGMA9)×	462/3304	**$3D_H$**	VL61	VGMA6−(VGMA6−VGMA7)×	536/3378
$1E_H$	VL30	VGMA8−(VGMA8−VGMA9)×	298/3304	**$3E_H$**$3E_H$	VL62	VGMA6−(VGMA6−VGMA7)×	268/3378
$1F_H$	VL31	VGMA8−(VGMA8−VGMA9)×	149/3304	**$3F_H$**	VL63	VGMA6	

Table 5. FPD33584B Upper Gamma Voltages (compatible with Samsung S6C0666)

Data	Output Voltage (gamma B)			Data	Output Voltage (gamma B)		
00_H	VH0	VGMA1		20_H	VH32	VGMA3	
01_H	VH1	VGMA2+(VGMA1−VGMA2)×	5747/6149	21_H	VH33	VGMA4+(VGMA3−VGMA4)×	2040/2174
02_H	VH2	VGMA2+(VGMA1−VGMA2)×	5345/6149	22_H	VH34	VGMA4+(VGMA3−VGMA4)×	1906/2174
03_H	VH3	VGMA2+(VGMA1−VGMA2)×	4943/6149	23_H	VH35	VGMA4+(VGMA3−VGMA4)×	1772/2174
04_H	VH4	VGMA2+(VGMA1−VGMA2)×	4541/6149	24_H	VH36	VGMA4+(VGMA3−VGMA4)×	1638/2174
05_H	VH5	VGMA2+(VGMA1−VGMA2)×	4139/6149	25_H	VH37	VGMA4+(VGMA3−VGMA4)×	1504/2174
06_H	VH6	VGMA2+(VGMA1−VGMA2)×	3737/6149	26_H	VH38	VGMA4+(VGMA3−VGMA4)×	1370/2174
07_H	VH7	VGMA2+(VGMA1−VGMA2)×	3335/6149	27_H	VH39	VGMA4+(VGMA3−VGMA4)×	1236/2174
08_H	VH8	VGMA2+(VGMA1−VGMA2)×	2933/6149	28_H	VH40	VGMA4+(VGMA3−VGMA4)×	1102/2174
09_H	VH9	VGMA2+(VGMA1−VGMA2)×	2531/6149	29_H	VH41	VGMA4+(VGMA3−VGMA4)×	968/2174
$0A_H$	VH10	VGMA2+(VGMA1−VGMA2)×	2129/6149	$2A_H$	VH42	VGMA4+(VGMA3−VGMA4)×	834/2174
$0B_H$	VH11	VGMA2+(VGMA1−VGMA2)×	1727/6149	$2B_H$	VH43	VGMA4+(VGMA3−VGMA4)×	700/2174
$0C_H$	VH12	VGMA2+(VGMA1−VGMA2)×	1325/6149	$2C_H$	VH44	VGMA4+(VGMA3−VGMA4)×	566/2174
$0D_H$	VH13	VGMA2+(VGMA1−VGMA2)×	968/6149	$2D_H$	VH45	VGMA4+(VGMA3−VGMA4)×	432/2174
$0E_H$	VH14	VGMA2+(VGMA1−VGMA2)×	611/6149	$2E_H$	VH46	VGMA4+(VGMA3−VGMA4)×	298/2174
$0F_H$	VH15	VGMA2+(VGMA1−VGMA2)×	298/6149	$2F_H$	VH47	VGMA4+(VGMA3−VGMA4)×	149/2174
10_H	VH16	VGMA2		30_H	VH48	VGMA4	
11_H	VH17	VGMA3+(VGMA2−VGMA3)×	3036/3304	31_H	VH49	VGMA5+(VGMA4−VGMA5)×	3214/3378
12_H	VH18	VGMA3+(VGMA2−VGMA3)×	2768/3304	32_H	VH50	VGMA5+(VGMA4−VGMA5)×	3035/3378
13_H	VH19	VGMA3+(VGMA2−VGMA3)×	2500/3304	33_H	VH51	VGMA5+(VGMA4−VGMA5)×	2856/3378
14_H	VH20	VGMA3+(VGMA2−VGMA3)×	2247/3304	34_H	VH52	VGMA5+(VGMA4−VGMA5)×	2663/3378
15_H	VH21	VGMA3+(VGMA2−VGMA3)×	2009/3304	35_H	VH53	VGMA5+(VGMA4−VGMA5)×	2470/3378
16_H	VH22	VGMA3+(VGMA2−VGMA3)×	1786/3304	36_H	VH54	VGMA5+(VGMA4−VGMA5)×	2262/3378
17_H	VH23	VGMA3+(VGMA2−VGMA3)×	1578/3304	37_H	VH55	VGMA5+(VGMA4−VGMA5)×	2054/3378
18_H	VH24	VGMA3+(VGMA2−VGMA3)×	1177/3304	38_H	VH56	VGMA5+(VGMA4−VGMA5)×	1816/3378
19_H	VH25	VGMA3+(VGMA2−VGMA3)×	984/3304	39_H	VH57	VGMA5+(VGMA4−VGMA5)×	1578/3378
$1A_H$	VH26	VGMA3+(VGMA2−VGMA3)×	805/3304	$3A_H$	VH58	VGMA5+(VGMA4−VGMA5)×	1325/3378
$1B_H$	VH27	VGMA3+(VGMA2−VGMA3)×	626/3304	$3B_H$	VH59	VGMA5+(VGMA4−VGMA5)×	1072/3378
$1C_H$	VH28	VGMA3+(VGMA2−VGMA3)×	462/3304	$3C_H$	VH60	VGMA5+(VGMA4−VGMA5)×	804/3378

Table 5. FPD33584B Upper Gamma Voltages (compatible with Samsung S6C0666) (continued)

Data	Output Voltage (gamma B)			Data	Output Voltage (gamma B)		
1D$_H$	VH29	VGMA3+(VGMA2−VGMA3)×	462/3304	**3D$_H$**	VH61	VGMA5+(VGMA4−VGMA5)×	536/3378
1E$_H$	VH30	VGMA3+(VGMA2−VGMA3)×	298/3304	**3E$_H$**	VH62	VGMA5+(VGMA4−VGMA5)×	268/3378
1F$_H$	VH31	VGMA3+(VGMA2−VGMA3)×	149/3304	**3F$_H$**	VH63	VGMA5	



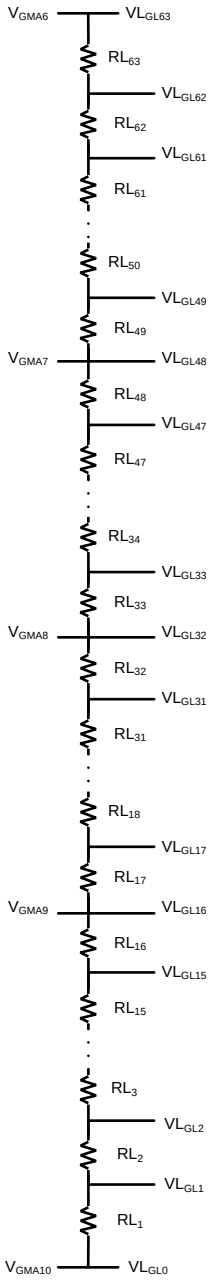


Figure 6. FPD33584C R-DAC Configuration

Table 6. FPD33584C Lower Gamma Voltages (compatible with NEC µPD17632A)

Data	Output Voltage (gamma C)			Data	Output Voltage (gamma C)		
00_H	VL0	VGMA10		**20_H**	VL32	VGMA8	
01_H	VL1	VGMA9−(VGMA9−VGMA10)×	7250/8050	**21_H**	VL33	VGMA7−(VGMA7−VGMA8)×	1500/1600
02_H	VL2	VGMA9−(VGMA9−VGMA10)×	6500/8050	**22_H**	VL34	VGMA7−(VGMA7−VGMA8)×	1400/1600
03_H	VL3	VGMA9−(VGMA9−VGMA10)×	5800/8050	**23_H**	VL35	VGMA7−(VGMA7−VGMA8)×	1300/1600

Table 6. FPD33584C Lower Gamma Voltages (compatible with NEC μPD17632A) (continued)

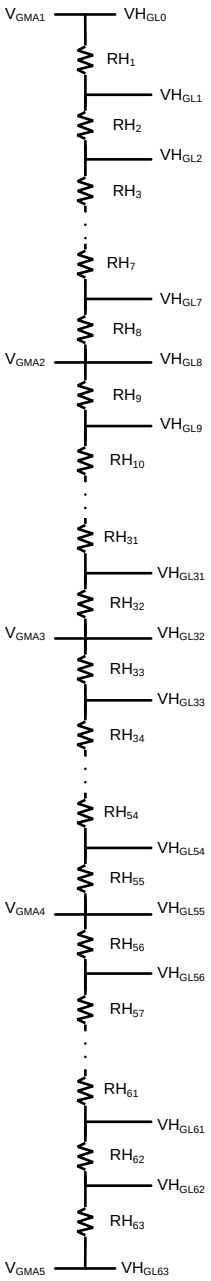
Data	Output Voltage (gamma C)			Data	Output Voltage (gamma C)		
04_H	VL4	VGMA9−(VGMA9−VGMA10)×	5150/8050	**24_H**	VL36	VGMA7−(VGMA7−VGMA8)×	1200/1600
05_H	VL5	VGMA9−(VGMA9−VGMA10)×	4550/8050	**25_H**	VL37	VGMA7−(VGMA7−VGMA8)×	1100/1600
06_H	VL6	VGMA9−(VGMA9−VGMA10)×	4000/8050	**26_H**	VL38	VGMA7−(VGMA7−VGMA8)×	1000/1600
07_H	VL7	VGMA9−(VGMA9−VGMA10)×	3450/8050	**27_H**	VL39	VGMA7−(VGMA7−VGMA8)×	900/1600
08_H	VL8	VGMA9−(VGMA9−VGMA10)×	2950/8050	**28_H**	VL40	VGMA7−(VGMA7−VGMA8)×	800/1600
09_H	VL9	VGMA9−(VGMA9−VGMA10)×	2450/8050	**29_H**	VL41	VGMA7−(VGMA7−VGMA8)×	700/1600
$0A_H$	VL10	VGMA9−(VGMA9−VGMA10)×	2050/8050	**$2A_H$**	VL42	VGMA7−(VGMA7−VGMA8)×	600/1600
$0B_H$	VL11	VGMA9−(VGMA9−VGMA10)×	1650/8050	**$2B_H$**	VL43	VGMA7−(VGMA7−VGMA8)×	500/1600
$0C_H$	VL12	VGMA9−(VGMA9−VGMA10)×	1300/8050	**$2C_H$**	VL44	VGMA7−(VGMA7−VGMA8)×	400/1600
$0D_H$	VL13	VGMA9−(VGMA9−VGMA10)×	950/8050	**$2D_H$**	VL45	VGMA7−(VGMA7−VGMA8)×	300/1600
$0E_H$	VL14	VGMA9−(VGMA9−VGMA10)×	600/8050	**$2E_H$**	VL46	VGMA7−(VGMA7−VGMA8)×	200/1600
$0F_H$	VL15	VGMA9−(VGMA9−VGMA10)×	300/8050	**$2F_H$**	VL47	VGMA7−(VGMA7−VGMA8)×	100/1600
10_H	VL16	VGMA9		**30_H**	VL48	VGMA7	
11_H	VL17	VGMA8−(VGMA8−VGMA9)×	2450/2750	**31_H**	VL49	VGMA6−(VGMA6−VGMA7)×	3350/3450
12_H	VL18	VGMA8−(VGMA8−VGMA9)×	2200/2750	**32_H**	VL50	VGMA6−(VGMA6−VGMA7)×	3250/3450
13_H	VL19	VGMA8−(VGMA8−VGMA9)×	1950/2750	**33_H**	VL51	VGMA6−(VGMA6−VGMA7)×	3150/3450
14_H	VL20	VGMA8−(VGMA8−VGMA9)×	1700/2750	**34_H**	VL52	VGMA6−(VGMA6−VGMA7)×	3050/3450
15_H	VL21	VGMA8−(VGMA8−VGMA9)×	1500/2750	**35_H**	VL53	VGMA6−(VGMA6−VGMA7)×	2950/3450
16_H	VL22	VGMA8−(VGMA8−VGMA9)×	1300/2750	**36_H**	VL54	VGMA6−(VGMA6−VGMA7)×	2800/3450
17_H	VL23	VGMA8−(VGMA8−VGMA9)×	1100/2750	**37_H**	VL55	VGMA6−(VGMA6−VGMA7)×	2650/3450
18_H	VL24	VGMA8−(VGMA8−VGMA9)×	950/2750	**38_H**38_H	VL56	VGMA6−(VGMA6−VGMA7)×	2500/3450
19_H 19_H	VL25	VGMA8−(VGMA8−VGMA9)×	800/2750	**39_H**	VL57	VGMA6−(VGMA6−VGMA7)×	2300/3450
$1A_H$	VL26	VGMA8−(VGMA8−VGMA9)×	650/2750	**$3A_H$**	VL58	VGMA6−(VGMA6−VGMA7)×	2100/3450
$1B_H$	VL27	VGMA8−(VGMA8−VGMA9)×	500/2750	**$3B_H$**	VL59	VGMA6−(VGMA6−VGMA7)×	1850/3450
$1C_H$	VL28	VGMA8−(VGMA8−VGMA9)×	400/2750	**$3C_H$**	VL60	VGMA6−(VGMA6−VGMA7)×	1600/3450
$1D_H$	VL29	VGMA8−(VGMA8−VGMA9)×	300/2750	**$3D_H$**	VL61	VGMA6−(VGMA6−VGMA7)×	1300/3450
$1E_H$	VL30	VGMA8−(VGMA8−VGMA9)×	200/2750	**$3E_H$**	VL62	VGMA6−(VGMA6−VGMA7)×	800/3450
$1F_H$	VL31	VGMA8−(VGMA8−VGMA9)×	100/2750	**$3F_H$**	VL63	VGMA6	

Table 7. FPD33584C Upper Gamma Voltages (compatible with NEC μPD17632A)

Data	Output Voltage (gamma C)			Data	Output Voltage (gamma C)		
00_H	VH0	VGMA1		20_H	VH32	VGMA3	
01_H	VH1	VGMA2+(VGMA1−VGMA2)×	7250/8050	21_H	VH33	VGMA4+(VGMA3−VGMA4)×	1500/1600
02_H	VH2	VGMA2+(VGMA1−VGMA2)×	6500/8050	22_H	VH34	VGMA4+(VGMA3−VGMA4)×	1400/1600
03_H	VH3	VGMA2+(VGMA1−VGMA2)×	5800/8050	23_H	VH35	VGMA4+(VGMA3−VGMA4)×	1300/1600
04_H	VH4	VGMA2+(VGMA1−VGMA2)×	5150/8050	24_H	VH36	VGMA4+(VGMA3−VGMA4)×	1200/1600
05_H	VH5	VGMA2+(VGMA1−VGMA2)×	4550/8050	25_H	VH37	VGMA4+(VGMA3−VGMA4)×	1100/1600
06_H	VH6	VGMA2+(VGMA1−VGMA2)×	4000/8050	26_H	VH38	VGMA4+(VGMA3−VGMA4)×	1000/1600
07_H	VH7	VGMA2+(VGMA1−VGMA2)×	3450/8050	27_H	VH39	VGMA4+(VGMA3−VGMA4)×	900/1600
08_H	VH8	VGMA2+(VGMA1−VGMA2)×	2950/8050	28_H	VH40	VGMA4+(VGMA3−VGMA4)×	800/1600
09_H	VH9	VGMA2+(VGMA1−VGMA2)×	2450/8050	29_H	VH41	VGMA4+(VGMA3−VGMA4)×	700/1600
$0A_H$	VH10	VGMA2+(VGMA1−VGMA2)×	2050/8050	$2A_H$	VH42	VGMA4+(VGMA3−VGMA4)×	600/1600
$0B_H$	VH11	VGMA2+(VGMA1−VGMA2)×	1650/8050	$2B_H$	VH43	VGMA4+(VGMA3−VGMA4)×	500/1600
$0C_H$	VH12	VGMA2+(VGMA1−VGMA2)×	1300/8050	$2C_H$	VH44	VGMA4+(VGMA3−VGMA4)×	400/1600
$0D_H$	VH13	VGMA2+(VGMA1−VGMA2)×	950/8050	$2D_H$	VH45	VGMA4+(VGMA3−VGMA4)×	300/1600
$0E_H$	VH14	VGMA2+(VGMA1−VGMA2)×	600/8050	$2E_H$	VH46	VGMA4+(VGMA3−VGMA4)×	200/1600
$0F_H$	VH15	VGMA2+(VGMA1−VGMA2)×	300/8050	$2F_H$	VH47	VGMA4+(VGMA3−VGMA4)×	100/1600
10_H	VH16	VGMA2		30_H	VH48	VGMA4	
11_H	VH17	VGMA3+(VGMA2−VGMA3)×	2450/2750	31_H	VH49	VGMA5+(VGMA4−VGMA5)×	3350/3450
12_H	VH18	VGMA3+(VGMA2−VGMA3)×	2200/2750	32_H	VH50	VGMA5+(VGMA4−VGMA5)×	3250/3450
13_H	VH19	VGMA3+(VGMA2−VGMA3)×	1950/2750	33_H	VH51	VGMA5+(VGMA4−VGMA5)×	3150/3450
14_H	VH20	VGMA3+(VGMA2−VGMA3)×	1700/2750	34_H	VH52	VGMA5+(VGMA4−VGMA5)×	3050/3450
15_H	VH21	VGMA3+(VGMA2−VGMA3)×	1500/2750	35_H	VH53	VGMA5+(VGMA4−VGMA5)×	2950/3450
16_H	VH22	VGMA3+(VGMA2−VGMA3)×	1300/2750	36_H	VH54	VGMA5+(VGMA4−VGMA5)×	2800/3450
17_H	VH23	VGMA3+(VGMA2−VGMA3)×	1100/2750	37_H	VH55	VGMA5+(VGMA4−VGMA5)×	2650/3450
18_H	VH24	VGMA3+(VGMA2−VGMA3)×	950/2750	38_H	VH56	VGMA5+(VGMA4−VGMA5)×	2500/3450
19_H	VH25	VGMA3+(VGMA2−VGMA3)×	800/2750	39_H	VH57	VGMA5+(VGMA4−VGMA5)×	2300/3450
$1A_H$	VH26	VGMA3+(VGMA2−VGMA3)×	650/2750	$3A_H$	VH58	VGMA5+(VGMA4−VGMA5)×	2100/3450
$1B_H$	VH27	VGMA3+(VGMA2−VGMA3)×	500/2750	$3B_H$	VH59	VGMA5+(VGMA4−VGMA5)×	1850/3450
$1C_H$	VH28	VGMA3+(VGMA2−VGMA3)×	400/2750	$3C_H$	VH60	VGMA5+(VGMA4−VGMA5)×	1600/3450

Table 7. FPD33584C Upper Gamma Voltages (compatible with NEC μPD17632A) (continued)

Data	Output Voltage (gamma C)			Data	Output Voltage (gamma C)		
$1D_H$	VH29	VGMA3+(VGMA2−VGMA3)×	300/2750	**$3D_H$**	VH61	VGMA5+(VGMA4−VGMA5)×	1300/3450
$1E_H$	VH30	VGMA3+(VGMA2−VGMA3)×	200/2750	**$3E_H$**	VH62	VGMA5+(VGMA4−VGMA5)×	800/3450
$1F_H$	VH31	VGMA3+(VGMA2−VGMA3)×	100/2750	**$3F_H$**	VH63	VGMA5	



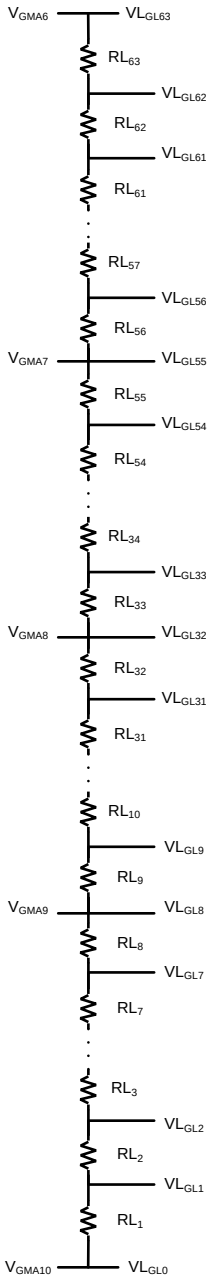


Figure 7. FPD33584D R-DAC Configuration (compatible with Hitachi HD66323)

Table 8. FPD33584D Lower Gamma Voltages (compatible with Hitach HD66323)

Data	Output Voltage (gamma D)			Data	Output Voltage (gamma D)		
00_H	VL0	VGMA10		**20_H**	VL32	VGMA8	
01_H	VL1	VGMA9−(VGMA9−VGMA10)×	3690/4613	**21_H**	VL33	VGMA7−(VGMA7−VGMA8)×	2783/2902
02_H	VL2	VGMA9−(VGMA9−VGMA10)×	2917/4613	**22_H**	VL34	VGMA7−(VGMA7−VGMA8)×	2664/2902
03_H	VL3	VGMA9−(VGMA9−VGMA10)×	2307/4613	**23_H**	VL35	VGMA7−(VGMA7−VGMA8)×	2545/2902

Table 8. FPD33584D Lower Gamma Voltages (compatible with Hitach HD66323) (continued)

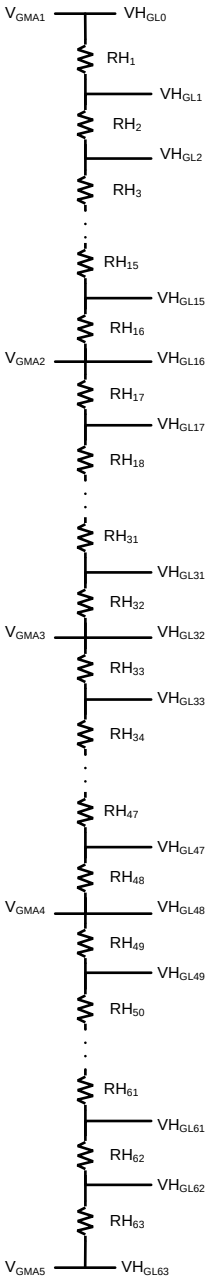
Data	Output Voltage (gamma D)			Data	Output Voltage (gamma D)		
04H	VL4	VGMA9−(VGMA9−VGMA10)×	1696/4613	**24H**	VL36	VGMA7−(VGMA7−VGMA8)×	2426/2902
05H	VL5	VGMA9−(VGMA9−VGMA10)×	1235/4613	**25H**	VL37	VGMA7−(VGMA7−VGMA8)×	2321/2902
06H	VL6	VGMA9−(VGMA9−VGMA10)×	774/4613	**26H**	VL38	VGMA7−(VGMA7−VGMA8)×	22217/2902
07H	VL7	VGMA9−(VGMA9−VGMA10)×	313/4613	**27H**	VL39	VGMA7−(VGMA7−VGMA8)×	2113/2902
08H	VL8	VGMA9		**28H**	VL40	VGMA7−(VGMA7−VGMA8)×	2009/2902
09H	VL9	VGMA8−(VGMA8−VGMA9)×	3646/3958	**29H**	VL41	VGMA7−(VGMA7−VGMA8)×	1905/2902
0AH	VL10	VGMA8−(VGMA8−VGMA9)×	3378/3958	**2AH**	VL42	VGMA7−(VGMA7−VGMA8)×	1786/2902
0BH	VL11	VGMA8−(VGMA8−VGMA9)×	3110/3958	**2BH**	VL43	VGMA7−(VGMA7−VGMA8)×	1667/2902
0CH	VL12	VGMA8−(VGMA8−VGMA9)×	2887/3958	**2CH**	VL44	VGMA7−(VGMA7−VGMA8)×	1548/2902
0DH	VL13	VGMA8−(VGMA8−VGMA9)×	2664/3958	**2DH**	VL45	VGMA7−(VGMA7−VGMA8)×	1429/2902
0EH	VL14	VGMA8−(VGMA8−VGMA9)×	2470/3958	**2EH**	VL46	VGMA7−(VGMA7−VGMA8)×	1310/2902
0FH	VL15	VGMA8−(VGMA8−VGMA9)×	2292/3958	**2FH**	VL47	VGMA7−(VGMA7−VGMA8)×	1190/2902
10H	VL16	VGMA8−(VGMA8−VGMA9)×	2113/3958	**30H**	VL48	VGMA7−(VGMA7−VGMA8)×	1071/2902
11H	VL17	VGMA8−(VGMA8−VGMA9)×	1949/3958	**31H**	VL49	VGMA7−(VGMA7−VGMA8)×	952/2902
12H	VL18	VGMA8−(VGMA8−VGMA9)×	1801/3958	**32H**	VL50	VGMA7−(VGMA7−VGMA8)×	818/2902
13H	VL19	VGMA8−(VGMA8−VGMA9)×	1652/3958	**33H**	VL51	VGMA7−(VGMA7−VGMA8)×	670/2902
14H	VL20	VGMA8−(VGMA8−VGMA9)×	1503/3958	**34H**	VL52	VGMA7−(VGMA7−VGMA8)×	521/2902
15H	VL21	VGMA8−(VGMA8−VGMA9)×	1369/3958	**35H**	VL53	VGMA7−(VGMA7−VGMA8)×	357/2902
16H	VL22	VGMA8−(VGMA8−VGMA9)×	1235/3958	**36H**	VL54	VGMA7−(VGMA7−VGMA8)×	179/2902
17H	VL23	VGMA8−(VGMA8−VGMA9)×	1101/3958	**37H**	VL55	VGMA7	
18H	VL24	VGMA8−(VGMA8−VGMA9)×	967/3958	**38H**	VL56	VGMA6−(VGMA6−VGMA7)×	3348/3527
19H	VL25	VGMA8−(VGMA8−VGMA9)×	833/3958	**39H**	VL57	VGMA6−(VGMA6−VGMA7)×	3125/3527
1AH	VL26	VGMA8−(VGMA8−VGMA9)×	714/3958	**3AH**	VL58	VGMA6−(VGMA6−VGMA7)×	2887/3527
1BH	VL27	VGMA8−(VGMA8−VGMA9)×	595/3958	**3BH**	VL59	VGMA6−(VGMA6−VGMA7)×	2619/3527
1CH	VL28	VGMA8−(VGMA8−VGMA9)×	476/3958	**3CH**	VL60	VGMA6−(VGMA6−VGMA7)×	2307/3527
1DH	VL29	VGMA8−(VGMA8−VGMA9)×	357/3958	**3DH**	VL61	VGMA6−(VGMA6−VGMA7)×	1845/3527
1EH	VL30	VGMA8−(VGMA8−VGMA9)×	239/3958	**3EH**	VL62	VGMA6−(VGMA6−VGMA7)×	1235/3527
1FH	VL31	VGMA8−(VGMA8−VGMA9)×	119/3958	**3FH**	VL63	VGMA6	

Table 9. FPD33584D Upper Gamma Voltages (compatible with Hitach HD66323)

Data	Output Voltage (gamma D)			Data	Output Voltage (gamma D)		
00_H	VH0	VGMA1		20_H	VH32	VGMA3	
01_H	VH1	VGMA2+(VGMA1−VGMA2)×	3690/4613	21_H	VH33	VGMA4+(VGMA3−VGMA4)×	2783/2902
02_H	VH2	VGMA2+(VGMA1−VGMA2)×	2917/4613	22_H	VH34	VGMA4+(VGMA3−VGMA4)×	2664/2902
03_H	VH3	VGMA2+(VGMA1−VGMA2)×	2307/4613	23_H	VH35	VGMA4+(VGMA3−VGMA4)×	2545/2902
04_H	VH4	VGMA2+(VGMA1−VGMA2)×	1696/4613	24_H	VH36	VGMA4+(VGMA3−VGMA4)×	2426/2902
05_H	VH5	VGMA2+(VGMA1−VGMA2)×	1235/4613	25_H	VH37	VGMA4+(VGMA3−VGMA4)×	2321/2902
06_H	VH6	VGMA2+(VGMA1−VGMA2)×	774/4613	26_H	VH38	VGMA4+(VGMA3−VGMA4)×	2217/2902
07_H	VH7	VGMA2+(VGMA1−VGMA2)×	313/4613	27_H	VH39	VGMA4+(VGMA3−VGMA4)×	2113/2902
08_H	VH8	VGMA2		28_H	VH40	VGMA4+(VGMA3−VGMA4)×	2009/2902
09_H	VH9	VGMA3+(VGMA2−VGMA3)×	3646/3958	29_H	VH41	VGMA4+(VGMA3−VGMA4)×	1905/2902
$0A_H$	VH10	VGMA3+(VGMA2−VGMA3)×	3378/3958	$2A_H$	VH42	VGMA4+(VGMA3−VGMA4)×	1786/2902
$0B_H$	VH11	VGMA3+(VGMA2−VGMA3)×	3110/3958	$2B_H$	VH43	VGMA4+(VGMA3−VGMA4)×	1667/2902
$0C_H$	VH12	VGMA3+(VGMA2−VGMA3)×	2887/3958	$2C_H$	VH44	VGMA4+(VGMA3−VGMA4)×	1548/2902
$0D_H$	VH13	VGMA3+(VGMA2−VGMA3)×	2664/3958	$2D_H$	VH45	VGMA4+(VGMA3−VGMA4)×	1429/2902
$0E_H$	VH14	VGMA3+(VGMA2−VGMA3)×	2470/3958	$2E_H$	VH46	VGMA4+(VGMA3−VGMA4)×	1310/2902
$0F_H$	VH15	VGMA3+(VGMA2−VGMA3)×	2292/3958	$2F_H$	VH47	VGMA4+(VGMA3−VGMA4)×	1190/2902
10_H	VH16	VGMA3+(VGMA2−VGMA3)×	2113/3958	30_H	VH48	VGMA4+(VGMA3−VGMA4)×	1071/2902
11_H	VH17	VGMA3+(VGMA2−VGMA3)×	1949/3958	31_H	VH49	VGMA4+(VGMA3−VGMA4)×	952/2902
12_H	VH18	VGMA3+(VGMA2−VGMA3)×	1801/3958	32_H	VH50	VGMA4+(VGMA3−VGMA4)×	818/2902
13_H	VH19	VGMA3+(VGMA2−VGMA3)×	1652/3958	33_H	VH51	VGMA4+(VGMA3−VGMA4)×	670/2902
14_H	VH20	VGMA3+(VGMA2−VGMA3)×	1503/3958	34_H	VH52	VGMA4+(VGMA3−VGMA4)×	521/2902
15_H	VH21	VGMA3+(VGMA2−VGMA3)×	1369/3958	35_H	VH53	VGMA4+(VGMA3−VGMA4)×	357/2902
16_H	VH22	VGMA3+(VGMA2−VGMA3)×	1235/3958	36_H	VH54	VGMA4+(VGMA3−VGMA4)×	179/2902
17_H	VH23	VGMA3+(VGMA2−VGMA3)×	1101/3958	37_H	VH55	VGMA4	
18_H	VH24	VGMA3+(VGMA2−VGMA3)×	967/3958	38_H	VH56	VGMA5+(VGMA4−VGMA5)×	3348/3527
19_H	VH25	VGMA3+(VGMA2−VGMA3)×	833/3958	39_H	VH57	VGMA5+(VGMA4−VGMA5)×	3125/3527
$1A_H$	VH26	VGMA3+(VGMA2−VGMA3)×	714/3958	$3A_H$	VH58	VGMA5+(VGMA4−VGMA5)×	2887/3527
$1B_H$	VH27	VGMA3+(VGMA2−VGMA3)×	595/3958	$3B_H$	VH59	VGMA5+(VGMA4−VGMA5)×	2619/3527

Table 9. FPD33584D Upper Gamma Voltages (compatible with Hitach HD66323) (continued)

Data	Output Voltage (gamma D)			Data	Output Voltage (gamma D)		
$1C_H$	VH28	VGMA3+(VGMA2−VGMA3)×	476/3958	**$3C_H$**	VH60	VGMA5+(VGMA4−VGMA5)×	2307/3527
$1D_H$	VH29	VGMA3+(VGMA2−VGMA3)×	357/3958	**$3D_H$**	VH61	VGMA5+(VGMA4−VGMA5)×	21845/3527
$1E_H$	VH30	VGMA3+(VGMA2−VGMA3)×	239/3958	**$3E_H$**	VH62	VGMA5+(VGMA4−VGMA5)×	1235/3927
$1F_H$	VH31	VGMA3+(VGMA2−VGMA3)×	119/3958	**$3F_H$**	VH63	VGMA5	1235/3527



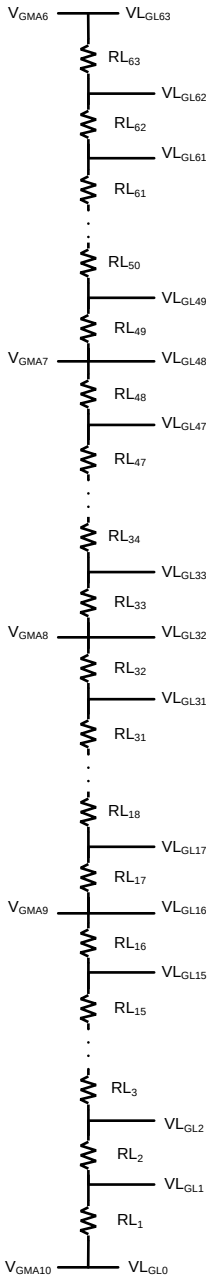


Figure 8. FPD33584F R-DAC Configuration

Table 10. FPD33584F Lower Gamma Voltages

Data	Output Voltage (gamma F)			Data	Output Voltage (gamma F)		
00_H	VL0	VGMA10		**20_H**	VL32	VGMA8	
01_H	VL1	VGMA9−(VGMA9−VGMA10)×	5536/6459	**21_H**	VL33	VGMA7−(VGMA7−VGMA8)×	1710/1829
02_H	VL2	VGMA9−(VGMA9−VGMA10)×	4762/6459	**22_H**	VL34	VGMA7−(VGMA7−VGMA8)×	1591/1829
03_H	VL3	VGMA9−(VGMA9−VGMA10)×	4152/6459	**23_H**	VL35	VGMA7−(VGMA7−VGMA8)×	1472/1829

Table 10. FPD33584F Lower Gamma Voltages (continued)

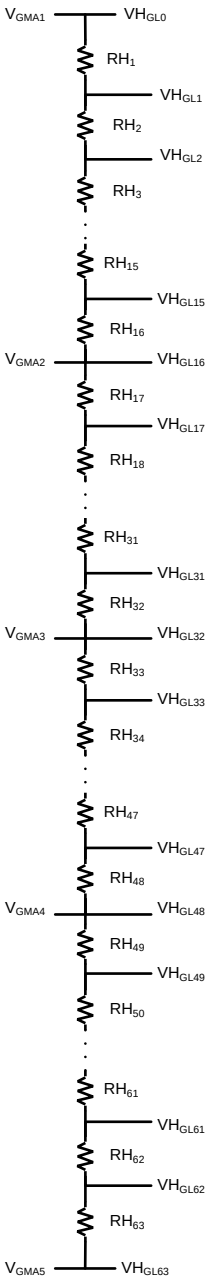
Data	Output Voltage (gamma F)			Data	Output Voltage (gamma F)		
04_H	VL4	VGMA9−(VGMA9−VGMA10)×	3542/6459	**24_H**	VL36	VGMA7−(VGMA7−VGMA8)×	1353/1829
05_H	VL5	VGMA9−(VGMA9−VGMA10)×	3081/6459	**25_H**	VL37	VGMA7−(VGMA7−VGMA8)×	1249/1829
06_H	VL6	VGMA9−(VGMA9−VGMA10)×	2620/6459	**26_H**	VL38	VGMA7−(VGMA7−VGMA8)×	1145/1829
07_H	VL7	VGMA9−(VGMA9−VGMA10)×	2159/6459	**27_H**	VL39	VGMA7−(VGMA7−VGMA8)×	1041/1829
08_H	VL8	VGMA9−(VGMA9−VGMA10)×	1846/6459	**28_H**	VL40	VGMA7−(VGMA7−VGMA8)×	937/1829
09_H	VL9	VGMA9−(VGMA9−VGMA10)×	1533/6459	**29_H**	VL41	VGMA7−(VGMA7−VGMA8)×	833/1829
$0A_H$	VL10	VGMA9−(VGMA9−VGMA10)×	1265/6459	**$2A_H$**	VL42	VGMA7−(VGMA7−VGMA8)×	714/1829
$0B_H$	VL11	VGMA9−(VGMA9−VGMA10)×	997/6459	**$2B_H$**	VL43	VGMA7−(VGMA7−VGMA8)×	595/1829
$0C_H$	VL12	VGMA9−(VGMA9−VGMA10)×	774/6459	**$2C_H$**	VL44	VGMA7−(VGMA7−VGMA8)×	476/1829
$0D_H$	VL13	VGMA9−(VGMA9−VGMA10)×	551/6459	**$2D_H$**	VL45	VGMA7−(VGMA7−VGMA8)×	357/1829
$0E_H$	VL14	VGMA9−(VGMA9−VGMA10)×	358/6459	**$2E_H$**	VL46	VGMA7−(VGMA7−VGMA8)×	238/1829
$0F_H$	VL15	VGMA9−(VGMA9−VGMA10)×	179/6459	**$2F_H$**	VL47	VGMA7−(VGMA7−VGMA8)×	119/1829
10_H	VL16	VGMA9		**30_H**	VL48	VGMA7	
11_H	VL17	VGMA8−(VGMA8−VGMA9)×	1950/2114	**31_H**	VL49	VGMA6−(VGMA6−VGMA7)×	4481/4600
12_H	VL18	VGMA8−(VGMA8−VGMA9)×	1801/2114	**32_H**	VL50	VGMA6−(VGMA6−VGMA7)×	4347/4600
13_H	VL19	VGMA8−(VGMA8−VGMA9)×	1652/2114	**33_H**	VL51	VGMA6−(VGMA6−VGMA7)×	4198/4600
14_H	VL20	VGMA8−(VGMA8−VGMA9)×	1503/2114	**34_H**	VL52	VGMA6−(VGMA6−VGMA7)×	4049/4600
15_H	VL21	VGMA8−(VGMA8−VGMA9)×	1369/2114	**35_H**	VL53	VGMA6−(VGMA6−VGMA7)×	3885/4600
16_H	VL22	VGMA8−(VGMA8−VGMA9)×	1235/2114	**36_H**	VL54	VGMA6−(VGMA6−VGMA7)×	3706/4600
17_H	VL23	VGMA8−(VGMA8−VGMA9)×	1101/2114	**37_H**	VL55	VGMA6−(VGMA6−VGMA7)×	3527/4600
18_H	VL24	VGMA8−(VGMA8−VGMA9)×	967/2114	**38_H**	VL56	VGMA6−(VGMA6−VGMA7)×	3348/4600
19_H	VL25	VGMA8−(VGMA8−VGMA9)×	833/2114	**39_H**	VL57	VGMA6−(VGMA6−VGMA7)×	3125/4600
$1A_H$	VL26	VGMA8−(VGMA8−VGMA9)×	714/2114	**$3A_H$**	VL58	VGMA6−(VGMA6−VGMA7)×	2887/4600
$1B_H$	VL27	VGMA8−(VGMA8−VGMA9)×	595/2114	**$3B_H$**	VL59	VGMA6−(VGMA6−VGMA7)×	2619/4600
$1C_H$	VL28	VGMA8−(VGMA8−VGMA9)×	476/2114	**$3C_H$**	VL60	VGMA6−(VGMA6−VGMA7)×	2306/4600
$1D_H$	VL29	VGMA8−(VGMA8−VGMA9)×	357/2114	**$3D_H$**	VL61	VGMA6−(VGMA6−VGMA7)×	1845/2600
$1E_H$	VL30	VGMA8−(VGMA8−VGMA9)×	238/2114	**$3E_H$**	VL62	VGMA6−(VGMA6−VGMA7)×	1235/4600
$1F_H$	VL31	VGMA8−(VGMA8−VGMA9)×	119/2114	**$3F_H$**	VL63	VGMA6	

Table 11. FPD33584F Upper Gamma Voltages

Data	Output Voltage (gamma F)			Data	Output Voltage (gamma F)		
00_H	VH0	VGMA1		20_H	VH32	VGMA3	
01_H	VH1	VGMA2+(VGMA1−VGMA2)×	5536/6459	21_H	VH33	VGMA4+(VGMA3−VGMA4)×	1710/1829
02_H	VH2	VGMA2+(VGMA1−VGMA2)×	4762/6459	22_H	VH34	VGMA4+(VGMA3−VGMA4)×	1591/1829
03_H	VH3	VGMA2+(VGMA1−VGMA2)×	4152/6459	23_H	VH35	VGMA4+(VGMA3−VGMA4)×	1472/1829
04_H	VH4	VGMA2+(VGMA1−VGMA2)×	3542/6459	24_H	VH36	VGMA4+(VGMA3−VGMA4)×	1353/1829
05_H	VH5	VGMA2+(VGMA1−VGMA2)×	3081/6459	25_H	VH37	VGMA4+(VGMA3−VGMA4)×	1249/1829
06_H	VH6	VGMA2+(VGMA1−VGMA2)×	2620/6459	26_H	VH38	VGMA4+(VGMA3−VGMA4)×	1145/1829
07_H	VH7	VGMA2+(VGMA1−VGMA2)×	2159/6459	27_H	VH39	VGMA4+(VGMA3−VGMA4)×	1041/1829
08_H	VH8	VGMA2+(VGMA1−VGMA2)×	1846/6459	28_H	VH40	VGMA4+(VGMA3−VGMA4)×	937/1829
09_H	VH9	VGMA2+(VGMA1−VGMA2)×	1533/6459	29_H	VH41	VGMA4+(VGMA3−VGMA4)×	833/1829
$0A_H$	VH10	VGMA2+(VGMA1−VGMA2)×	1265/6459	$2A_H$	VH42	VGMA4+(VGMA3−VGMA4)×	714/1829
$0B_H$	VH11	VGMA2+(VGMA1−VGMA2)×	997/6459	$2B_H$	VH43	VGMA4+(VGMA3−VGMA4)×	595/1829
$0C_H$	VH12	VGMA2+(VGMA1−VGMA2)×	774/6459	$2C_H$	VH44	VGMA4+(VGMA3−VGMA4)×	476/1829
$0D_H$	VH13	VGMA2+(VGMA1−VGMA2)×	551/6459	$2D_H$	VH45	VGMA4+(VGMA3−VGMA4)×	357/1829
$0E_H$	VH14	VGMA2+(VGMA1−VGMA2)×	358/6459	$2E_H$	VH46	VGMA4+(VGMA3−VGMA4)×	238/1829
$0F_H$	VH15	VGMA2+(VGMA1−VGMA2)×	179/6459	$2F_H$	VH47	VGMA4+(VGMA3−VGMA4)×	119/1829
10_H	VH16	VGMA2		30_H	VH48	VGMA4	
11_H	VH17	VGMA3+(VGMA2−VGMA3)×	1950/2114	31_H	VH49	VGMA5+(VGMA4−VGMA5)×	4481/4600
12_H	VH18	VGMA3+(VGMA2−VGMA3)×	1801/2114	32_H	VH50	VGMA5+(VGMA4−VGMA5)×	4347/4600
13_H	VH19	VGMA3+(VGMA2−VGMA3)×	1652/2114	33_H	VH51	VGMA5+(VGMA4−VGMA5)×	4198/4600
14_H	VH20	VGMA3+(VGMA2−VGMA3)×	1503/2114	34_H	VH52	VGMA5+(VGMA4−VGMA5)×	4049/4600
15_H	VH21	VGMA3+(VGMA2−VGMA3)×	1369/2114	35_H	VH53	VGMA5+(VGMA4−VGMA5)×	3885/4600
16_H	VH22	VGMA3+(VGMA2−VGMA3)×	1235/2114	36_H	VH54	VGMA5+(VGMA4−VGMA5)×	3706/4600
17_H	VH23	VGMA3+(VGMA2−VGMA3)×	1101/2114	37_H	VH55	VGMA5+(VGMA4−VGMA5)×	3527/4600
18_H	VH24	VGMA3+(VGMA2−VGMA3)×	967/2114	38_H	VH56	VGMA5+(VGMA4−VGMA5)×	3348/4600
19_H	VH25	VGMA3+(VGMA2−VGMA3)×	833/2114	39_H	VH57	VGMA5+(VGMA4−VGMA5)×	3125/4600
$1A_H$	VH26	VGMA3+(VGMA2−VGMA3)×	714/2114	$3A_H$	VH58	VGMA5+(VGMA4−VGMA5)×	2887/4600
$1B_H$	VH27	VGMA3+(VGMA2−VGMA3)×	595/2114	$3B_H$	VH59	VGMA5+(VGMA4−VGMA5)×	2619/4600
$1C_H$	VH28	VGMA3+(VGMA2−VGMA3)×	476/2114	$3C_H$	VH60	VGMA5+(VGMA4−VGMA5)×	2306/4600

Table 11. FPD33584F Upper Gamma Voltages (continued)

Data	Output Voltage (gamma F)			Data	Output Voltage (gamma F)		
1D$_H$	VH29	VGMA3+(VGMA2−VGMA3)×	357/2114	**3D$_H$**	VH61	VGMA5+(VGMA4−VGMA5)×	1845/4600
1E$_H$	VH30	VGMA3+(VGMA2−VGMA3)×	238/2114	**3E$_H$**	VH62	VGMA5+(VGMA4−VGMA5)×	1235/4600
1F$_H$	VH31	VGMA3+(VGMA2−VGMA3)×	119/2114	**3F$_H$**	VH63	VGMA5	



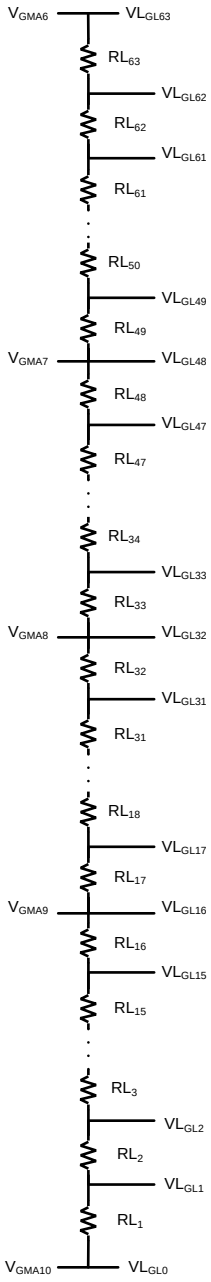


Figure 9. FPD33584G R-DAC Configuration

Table 12. FPD33584G Lower Gamma Voltages

Data	Output Voltage (gamma G)			Data	Output Voltage (gamma G)		
00_H	VL0	VGMA10		**20_H**	VL32	VGMA8	
01_H	VL1	VGMA9−(VGMA9−VGMA10)×	6027/6667	**21_H**	VL33	VGMA7−(VGMA7−VGMA8)×	1500/1604
02_H	VL2	VGMA9−(VGMA9−VGMA10)×	5432/6667	**22_H**	VL34	VGMA7−(VGMA7−VGMA8)×	1396/1604
03_H	VL3	VGMA9−(VGMA9−VGMA10)×	4837/6667	**23_H**	VL35	VGMA7−(VGMA7−VGMA8)×	1307/1604

Table 12. FPD33584G Lower Gamma Voltages (continued)

Data	Output Voltage (gamma G)			Data	Output Voltage (gamma G)		
04_H	VL4	VGMA9−(VGMA9−VGMA10)×	4257/6667	**24_H**	VL36	VGMA7−(VGMA7−VGMA8)×	1218/1604
05_H	VL5	VGMA9−(VGMA9−VGMA10)×	3692/6667	**25_H**	VL37	VGMA7−(VGMA7−VGMA8)×	1114/1604
06_H	VL6	VGMA9−(VGMA9−VGMA10)×	3186/6667	**26_H**	VL38	VGMA7−(VGMA7−VGMA8)×	1010/1604
07_H	VL7	VGMA9−(VGMA9−VGMA10)×	2769/6667	**27_H**	VL39	VGMA7−(VGMA7−VGMA8)×	906/1604
08_H	VL8	VGMA9−(VGMA9−VGMA10)×	2352/6667	**28_H**	VL40	VGMA7−(VGMA7−VGMA8)×	817/1604
09_H	VL9	VGMA9−(VGMA9−VGMA10)×	1920/6667	**29_H**	VL41	VGMA7−(VGMA7−VGMA8)×	713/1604
$0A_H$	VL10	VGMA9−(VGMA9−VGMA10)×	1533/6667	**$2A_H$**	VL42	VGMA7−(VGMA7−VGMA8)×	624/1604
$0B_H$	VL11	VGMA9−(VGMA9−VGMA10)×	1220/6667	**$2B_H$**	VL43	VGMA7−(VGMA7−VGMA8)×	520/1604
$0C_H$	VL12	VGMA9−(VGMA9−VGMA10)×	937/6667	**$2C_H$**	VL44	VGMA7−(VGMA7−VGMA8)×	431/1604
$0D_H$	VL13	VGMA9−(VGMA9−VGMA10)×	684/6667	**$2D_H$**	VL45	VGMA7−(VGMA7−VGMA8)×	327/1604
$0E_H$	VL14	VGMA9−(VGMA9−VGMA10)×	431/6667	**$2E_H$**	VL46	VGMA7−(VGMA7−VGMA8)×	208/1604
$0F_H$	VL15	VGMA9−(VGMA9−VGMA10)×	208/6667	**$2F_H$**	VL47	VGMA7−(VGMA7−VGMA8)×	104/1604
10_H	VL16	VGMA9		**30_H**	VL48	VGMA7	
11_H	VL17	VGMA8−(VGMA8−VGMA9)×	1949/2142	**31_H**	VL49	VGMA6−(VGMA6−VGMA7)×	4479/4583
12_H	VL18	VGMA8−(VGMA8−VGMA9)×	1756/2142	**32_H**	VL50	VGMA6−(VGMA6−VGMA7)×	4360/4583
13_H	VL19	VGMA8−(VGMA8−VGMA9)×	1592/2142	**33_H**	VL51	VGMA6−(VGMA6−VGMA7)×	4241/4583
14_H	VL20	VGMA8−(VGMA8−VGMA9)×	1443/2142	**34_H**	VL52	VGMA6−(VGMA6−VGMA7)×	4122/4583
15_H	VL21	VGMA8−(VGMA8−VGMA9)×	1294/2142	**35_H**	VL53	VGMA6−(VGMA6−VGMA7)×	4003/4583
16_H	VL22	VGMA8−(VGMA8−VGMA9)×	1160/2142	**36_H**	VL54	VGMA6−(VGMA6−VGMA7)×	3869/4583
17_H	VL23	VGMA8−(VGMA8−VGMA9)×	1026/2142	**37_H**	VL55	VGMA6−(VGMA6−VGMA7)×	3735/4583
18_H	VL24	VGMA8−(VGMA8−VGMA9)×	892/2142	**38_H**	VL56	VGMA6−(VGMA6−VGMA7)×	3571/4583
19_H	VL25	VGMA8−(VGMA8−VGMA9)×	758/2142	**39_H**	VL57	VGMA6−(VGMA6−VGMA7)×	3392/4583
$1A_H$	VL26	VGMA8−(VGMA8−VGMA9)×	639/2142	**$3A_H$**	VL58	VGMA6−(VGMA6−VGMA7)×	3184/4583
$1B_H$	VL27	VGMA8−(VGMA8−VGMA9)×	520/2142	**$3B_H$**	VL59	VGMA6−(VGMA6−VGMA7)×	2991/4583
$1C_H$	VL28	VGMA8−(VGMA8−VGMA9)×	416/2142	**$3C_H$**	VL60	VGMA6−(VGMA6−VGMA7)×	2753/4583
$1D_H$	VL29	VGMA8−(VGMA8−VGMA9)×	312/2142	**$3D_H$**	VL61	VGMA6−(VGMA6−VGMA7)×	2426/4583
$1E_H$	VL30	VGMA8−(VGMA8−VGMA9)×	208/2142	**$3E_H$**	VL62	VGMA6−(VGMA6−VGMA7)×	1875/4583
$1F_H$	VL31	VGMA8−(VGMA8−VGMA9)×	104/2142	**$3F_H$**	VL63	VGMA6	

Table 13. FPD33584G Upper Gamma Voltages

Data	Output Voltage (gamma G)			Data	Output Voltage (gamma G)		
00_H	VH0	VGMA1		20_H	VH32	VGMA3	
01_H	VH1	VGMA2+(VGMA1−VGMA2)×	6027/6667	21_H	VH33	VGMA4+(VGMA3−VGMA4)×	1500/1604
02_H	VH2	VGMA2+(VGMA1−VGMA2)×	5432/6667	22_H	VH34	VGMA4+(VGMA3−VGMA4)×	1396/1604
03_H	VH3	VGMA2+(VGMA1−VGMA2)×	4837/6667	23_H	VH35	VGMA4+(VGMA3−VGMA4)×	1307/1604
04_H	VH4	VGMA2+(VGMA1−VGMA2)×	4257/6667	24_H	VH36	VGMA4+(VGMA3−VGMA4)×	1218/1604
05_H	VH5	VGMA2+(VGMA1−VGMA2)×	3692/6667	25_H	VH37	VGMA4+(VGMA3−VGMA4)×	1114/1604
06_H	VH6	VGMA2+(VGMA1−VGMA2)×	3186/6667	26_H	VH38	VGMA4+(VGMA3−VGMA4)×	1010/1604
07_H	VH7	VGMA2+(VGMA1−VGMA2)×	2769/6667	27_H	VH39	VGMA4+(VGMA3−VGMA4)×	906/1604
08_H	VH8	VGMA2+(VGMA1−VGMA2)×	2352/6667	28_H	VH40	VGMA4+(VGMA3−VGMA4)×	817/1604
09_H	VH9	VGMA2+(VGMA1−VGMA2)×	1920/6667	29_H	VH41	VGMA4+(VGMA3−VGMA4)×	713/1604
$0A_H$	VH10	VGMA2+(VGMA1−VGMA2)×	1533/6667	$2A_H$	VH42	VGMA4+(VGMA3−VGMA4)×	624/1604
$0B_H$	VH11	VGMA2+(VGMA1−VGMA2)×	1220/6667	$2B_H$	VH43	VGMA4+(VGMA3−VGMA4)×	520/1604
$0C_H$	VH12	VGMA2+(VGMA1−VGMA2)×	937/6667	$2C_H$	VH44	VGMA4+(VGMA3−VGMA4)×	431/1604
$0D_H$	VH13	VGMA2+(VGMA1−VGMA2)×	684/6667	$2D_H$	VH45	VGMA4+(VGMA3−VGMA4)×	327/1604
$0E_H$	VH14	VGMA2+(VGMA1−VGMA2)×	431/6667	$2E_H$	VH46	VGMA4+(VGMA3−VGMA4)×	208/1604
$0F_H$	VH15	VGMA2+(VGMA1−VGMA2)×	208/6667	$2F_H$	VH47	VGMA4+(VGMA3−VGMA4)×	104/1604
10_H	VH16	VGMA2		30_H	VH48	VGMA4	
11_H	VH17	VGMA3+(VGMA2−VGMA3)×	1949/2142	31_H	VH49	VGMA5+(VGMA4−VGMA5)×	4479/4583
12_H	VH18	VGMA3+(VGMA2−VGMA3)×	1756/2142	32_H	VH50	VGMA5+(VGMA4−VGMA5)×	4360/4583
13_H	VH19	VGMA3+(VGMA2−VGMA3)×	1592/2142	33_H	VH51	VGMA5+(VGMA4−VGMA5)×	4241/4583
14_H	VH20	VGMA3+(VGMA2−VGMA3)×	1443/2142	34_H	VH52	VGMA5+(VGMA4−VGMA5)×	4122/4583
15_H	VH21	VGMA3+(VGMA2−VGMA3)×	1294/2142	35_H	VH53	VGMA5+(VGMA4−VGMA5)×	4003/4583
16_H	VH22	VGMA3+(VGMA2−VGMA3)×	1160/2142	36_H	VH54	VGMA5+(VGMA4−VGMA5)×	3869/4583
17_H	VH23	VGMA3+(VGMA2−VGMA3)×	1026/2142	37_H	VH55	VGMA5+(VGMA4−VGMA5)×	3735/4853
18_H	VH24	VGMA3+(VGMA2−VGMA3)×	892/2142	38_H	VH56	VGMA5+(VGMA4−VGMA5)×	3571/4583
19_H	VH25	VGMA3+(VGMA2−VGMA3)×	758/2142	39_H	VH57	VGMA5+(VGMA4−VGMA5)×	3392/4583
$1A_H$	VH26	VGMA3+(VGMA2−VGMA3)×	639/2142	$3A_H$	VH58	VGMA5+(VGMA4−VGMA5)×	3184/4583
$1B_H$	VH27	VGMA3+(VGMA2−VGMA3)×	520/2142	$3B_H$	VH59	VGMA5+(VGMA4−VGMA5)×	2991/4583
$1C_H$	VH28	VGMA3+(VGMA2−VGMA3)×	416/2142	$3C_H$	VH60	VGMA5+(VGMA4−VGMA5)×	2753/4583

Table 13. FPD33584G Upper Gamma Voltages (continued)

Data	Output Voltage (gamma G)			Data	Output Voltage (gamma G)		
1D$_H$	VH29	VGMA3+(VGMA2−VGMA3)×	312/2142	**3D$_H$**	VH61	VGMA5+(VGMA4−VGMA5)×	2426/4583
1E$_H$	VH30	VGMA3+(VGMA2−VGMA3)×	208/2142	**3E$_H$**	VH62	VGMA5+(VGMA4−VGMA5)×	1875/4583
1F$_H$	VH31	VGMA3+(VGMA2−VGMA3)×	104/2142	**3F$_H$**	VH63	VGMA5	

Table 14. FPD33584 R-DAC Resistance Values

R	A (Ω)	B (Ω)	C (Ω)	D (Ω)	F (Ω)	G (Ω)	R	A (Ω)	B (Ω)	C (Ω)	D (Ω)	F (Ω)	G (Ω)
Rx1	1830	402	800	923	923	640	**Rx33**	104	134	100	119	119	104
Rx2	1027	402	750	774	774	595	**Rx34**	104	134	100	119	119	104
Rx3	739	402	700	610	610	595	**Rx35**	104	134	100	119	119	89
Rx4	625	402	650	610	610	580	**Rx36**	104	134	100	119	119	89
Rx5	521	402	600	461	461	565	**Rx37**	104	134	100	104	104	104
Rx6	417	402	550	461	461	506	**Rx38**	104	134	100	104	104	104
Rx7	417	402	550	461	461	417	**Rx39**	104	134	100	104	104	104
Rx8	313	402	500	313	313	417	**Rx40**	104	134	100	104	104	89
Rx9	313	402	500	313	313	432	**Rx41**	104	134	100	104	104	104
Rx10	208	402	400	268	268	387	**Rx42**	104	134	100	119	119	89
Rx11	208	402	400	268	268	313	**Rx43**	104	134	100	119	119	104
Rx12	149	402	350	223	223	283	**Rx44**	119	134	100	119	119	89
Rx13	149	357	350	223	223	253	**Rx45**	119	134	100	119	119	104
Rx14	134	357	350	193	193	253	**Rx46**	119	134	100	119	119	119
Rx15	134	313	300	179	179	223	**Rx47**	119	149	100	119	119	104
Rx16	119	298	300	179	179	208	**Rx48**	119	149	100	119	119	104
Rx17	119	268	300	164	164	193	**Rx49**	119	164	100	119	119	104
Rx18	119	268	250	149	149	193	**Rx50**	119	179	100	134	134	119
Rx19	119	268	250	149	149	164	**Rx51**	134	179	100	149	149	119
Rx20	119	253	250	149	149	149	**Rx52**	134	193	100	149	149	119
Rx21	104	238	200	134	134	149	**Rx53**	149	193	100	164	164	119
Rx22	104	223	200	134	134	134	**Rx54**	149	208	150	179	179	134
Rx23	104	208	200	134	134	134	**Rx55**	149	208	150	179	179	134
Rx24	104	208	150	134	134	134	**Rx56**	149	238	150	179	179	164
Rx25	104	193	150	134	134	134	**Rx57**	193	238	200	223	223	179
Rx26	104	193	150	119	119	119	**Rx58**	223	253	200	238	238	208
Rx27	104	179	150	119	119	119	**Rx59**	253	253	250	268	268	193
Rx28	104	179	100	119	119	104	**Rx60**	313	268	250	313	313	238
Rx29	104	164	100	119	119	104	**Rx61**	521	268	300	461	461	327
Rx30	104	164	100	119	119	104	**Rx62**	714	268	500	610	610	551
Rx31	104	149	100	119	119	104	**Rx63**	923	268	800	1235	1235	1875
Rx32	104	149	100	119	119	104	**R^{total}**	14998	15005	15850	15000	15000	15002

Table 15. FPD33584 I/O Configuration

	INPUTS				OUTPUTS	
optional	RPI2				Y384	
optional	RPIO2				Y383	
	DIO2				Y382	
	D22P					
	D22N				.	
	D21P				.	
	D21N				.	
	D20P				.	
	D20N				.	
	D12P				.	
	D12N				.	
	D11P				.	
	D11N				.	
	D10P				.	
	D10N				.	
	VDD1				.	
	SHL				.	
	VGMA10				.	
optional	VGMA9				.	
optional	VGMA8				.	
optional	VGMA7				.	
	VGMA6				.	
	VDD2		FPD33584		.	
	VSS2				.	
	VGMA5				.	
optional	VGMA4				.	
optional	VGMA3				.	
optional	VGMA2				.	
	VGMA1				.	
	VSS1				.	
	CLKP				.	
	CLKN				.	
	CLK1				.	
	POL				.	
optional	DATPOL				.	
	D02P				.	
	D02N				.	
	D01P				.	
	D01N				.	
	D00P				.	
	D00N				.	
	DIO1				Y3	
optional	RPO1				Y2	
optional	RPI1				Y1	

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