FAIRCHILD SEMICONDUCTOR®

November 2012

FAN2504
200 mA CMOS LDO Regulator

Features

- Ultra-Low Power Consumption
- 200 mV Dropout Voltage at 200 mA
- 75 µA Ground Current at 200 mA
- Enable/Shutdown Control
- SOT23-5 package
- Thermal Limiting
- 300 mA Peak Current
- 3.3 V Typical Output Voltage

Applications

- Cellular Phones and Accessories
- PDAs
- Portable Cameras and Video Recorders
- Laptop, Notebook, and Palmtop Computers

Description

FAN2504 micro-power low-dropout voltage regulator uses CMOS technology to offer a new level of cost-effective performance in GSM and TDMA cellular handsets, laptops and notebook portable computers, and other portable devices. Features include extremely low power consumption, low shutdown current, low dropout voltage, exceptional loop stability able to accommodate a wide variety of external capacitors, and compact SOT23-5 surface-mount packaging. FAN2504 offers significant improvements over older BiCMOS designs and is pin-compatible with many popular devices. The output is thermally protected against overload.

To utilize the FAN2504 bypass function, a bypass capacitor can be connected to the bypass pin (pin 4) for noise reduction.

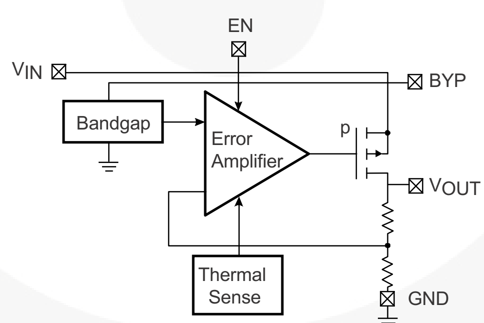


Figure 1. Block Diagram

Ordering Information

Part Number	V_{OUT}	Pin 4 Function	Top Mark	Package	Packing Method
FAN2504S33X	3.3	Bypass	AG3	SOT-23 5L	3000 on Tape and Reel, 7-inch Reel, 8mm Tape

Pin Configuration

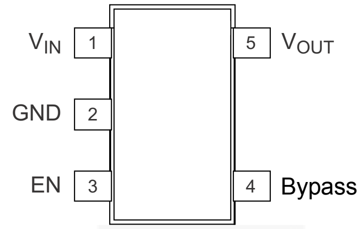


Figure 2. Pin Configuration

Pin Descriptions

Pin Name	Pin No.	Type	Description
Bypass	4	Passive	**Bypass.** Connect 470 pF capacitor for noise reduction.
EN	3	Digital Input	**Enable.** 0: Shutdown V_{OUT}. 1: Enable V_{OUT}.
V_{IN}	1	Power in	**Voltage Input.** Supply voltage input.
V_{OUT}	5	Power out	**Voltage Output.** Regulated output voltage.
GND	2	Power	**Ground.**

Absolute Maximum Ratings (1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Min.	Typ.	Max.	Unit
Power Supply Voltages				
V_{IN} (Measured to GND)	0		7	V
Enable Input (EN)				
Applied Voltage (Measured to GND)(2)	0		7	V
$\overline{\text{ERR}}$ Output				
Applied Voltage (Measured to GND)(2)	0		7	V
Power				
Dissipation(3)	Internally Limited			
Temperature				
Junction	-65		150	°C
Lead Soldering (5 seconds)			260	°C
Storage	-65		150	°C
Electrostatic Discharge(4)	4			kV

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Based upon thermally limited junction temperature:

$$P_D = \frac{T_{J(max)} - T_A}{\Theta_{JA}}$$

4. Human Body Model is 4kV minimum using Mil Std. 883E, method 3015.7. Machine Model is 400V minimum using JEDEC method A115-A.

Recommended Operating Conditions

The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Nom.	Max.	Unit
V_{IN}	Input Voltage Range	2.7		6.5	V
V_{OUT}	Output Voltage Range, Adjustable	V_{REF}		V_{IN} - V_{DC}	V
V_{EN}	Enable Input Voltage	0		V_{IN}	V
T_J	Junction Temperature	-40		-125	°C
θ_{JA}	Thermal Resistance		220		°C/W
θ_{JC}	Thermal Resistance		130		°C/W

Electrical Characteristics [5, 6]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Regulator						
V_{DO}	Drop Out Voltage	I_{OUT} = 100 μA		2.5	4	mV
		I_{OUT} = 50 mA		50	75	mV
		I_{OUT} = 100 mA		100	140	mV
		I_{OUT} = 150 mA		150	180	mV
		I_{OUT} = 200 mA		170	200	mV
ΔV_{DO}	Output Voltage Accuracy		-2		2	%
I_{GND}	Ground Pin Current	I_{OUT} = 200 mA			75	μA
Protection						
	Current Limit	Thermally Protected				
I_{GSD}	Shutdown Current	EN = 0 V			1	μA
T_{SH}	Thermal Protection Shutdown Temperature		150			°C
Enable Input						
V_{IL}	Logic Low Voltage			1.2	0.4	V
V_{IH}	Logic High Voltage		2.0	1.4		V
I_{IH}	Input Current High				1	μA
I_I	Input Current Low				1	μA

Switching Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Enable Input[7]					
Response Time				500	μs

Performance Characteristics [5, 6]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	$V_{IN} = (V_{OUT} + 1)$ to 6.5 V		0.3		% / V
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	I_{OUT} = 0.1 to 200 mA		1.0	2.0	%
e_N	Output Noise	f = 10 Hz to 1 KHz at V_{IN}, C_{OUT} = 10 μF, C_{BYP} = 0.01 μF		<7		$\mu V/\sqrt{Hz}$
		f > 10 KHz at V_{IN}, C_{OUT} = 10 μF, C_{BYP} = 0.01 μF		<0.01		
PSRR	Power Supply Rejection	f = 120 Hz at V_{IN}, C_{OUT} = 10 μF, C_{BYP} = 0.01 μF		43		dB

Note:

5. Unless otherwise stated, T_A = 25°C, $V_{IN} = V_{OUT}$ + 1 V, I_{OUT} = 100 μF, V_{IH} > 2.0 V.
6. Bold values indicate -40 ≤ T_J ≤ 125°C.
7. When using repeated cycling.

Typical Performance Characteristics

Figure 3. Power Supply Rejection Ratio

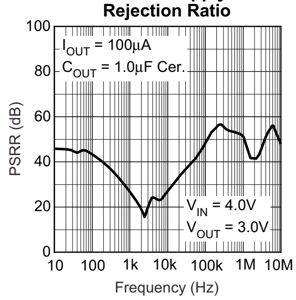


Figure 4. Power Supply Rejection Ratio

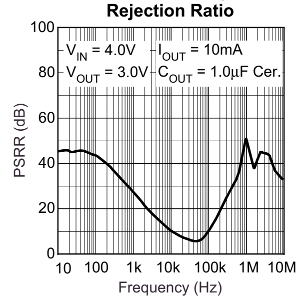


Figure 5. Power Supply Rejection Ratio

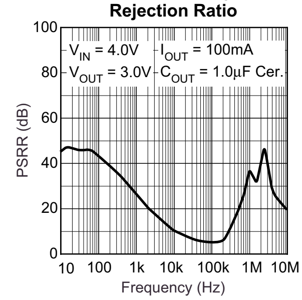


Figure 6. Power Supply Rejection Ratio

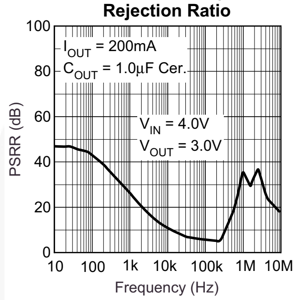


Figure 7. Power Supply Rejection Ratio

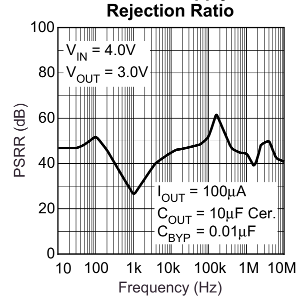


Figure 8. Power Supply Rejection Ratio

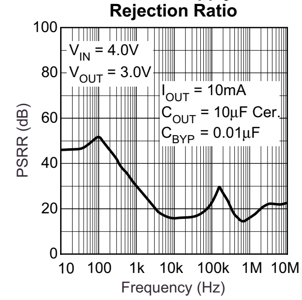


Figure 9. Power Supply Rejection Ratio

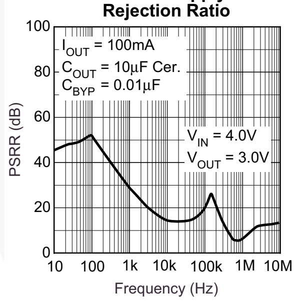


Figure 10. Power Supply Rejection Ratio

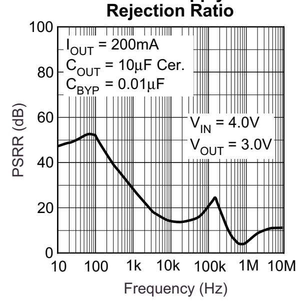


Figure 11. Power Supply Rejection Ratio vs. Voltage

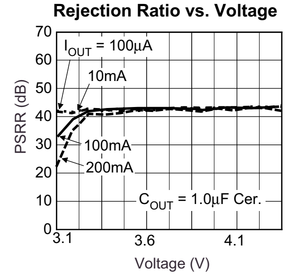


Figure 12. Power Supply Rejection Ratio vs. Voltage

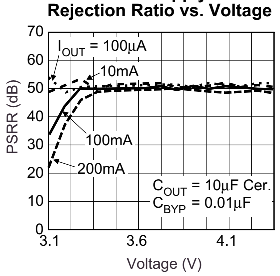


Figure 13. Noise Performance

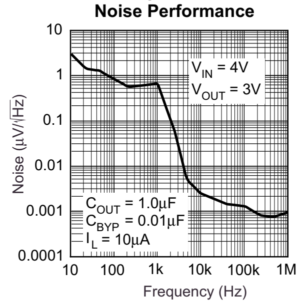
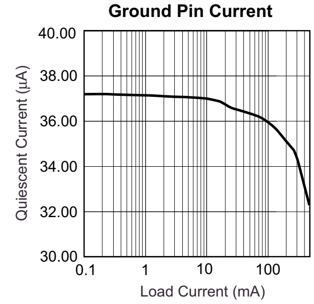


Figure 14. Ground Pin Current



Typical Performance Characteristics (Continued)

Figure 15. Ground Pin Current

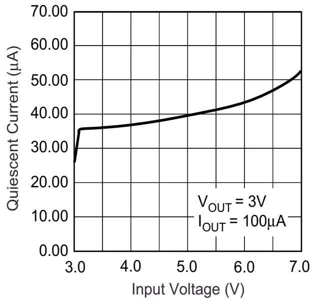


Figure 16. Ground Pin Current

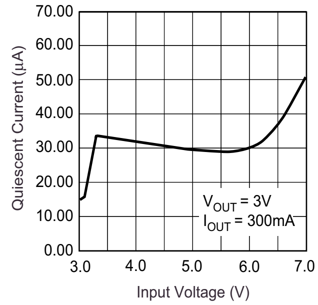


Figure 17. Ground Pin Current

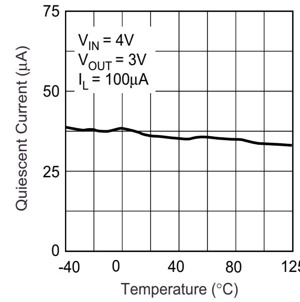


Figure 18. Ground Pin Current

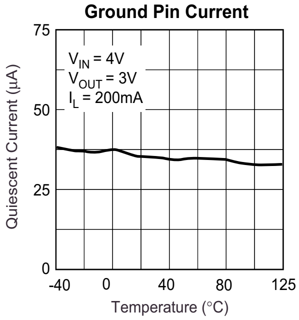


Figure 19. Dropout Voltage

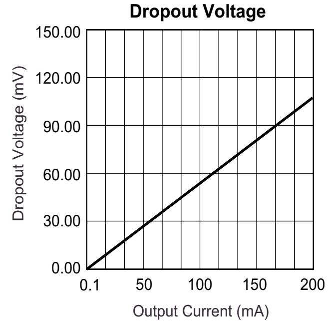


Figure 20. Dropout Characteristics

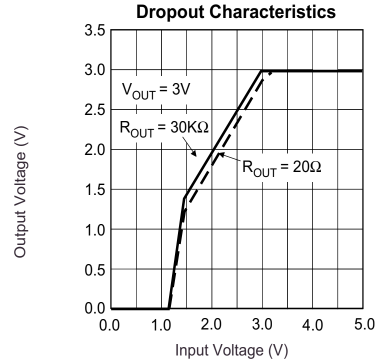


Figure 21. Dropout Voltage

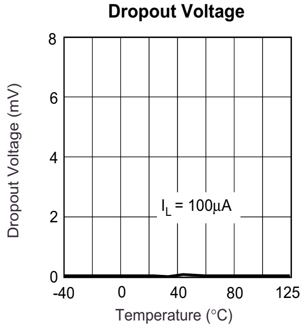


Figure 22. Dropout Voltage

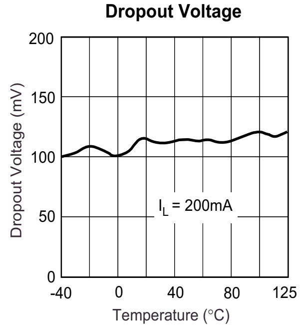
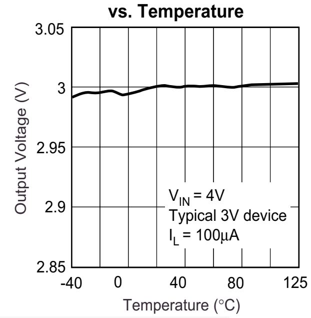


Figure 23. Output Voltage vs. Temperature



Functional Characteristics

Figure 24. Enable Pin Delay

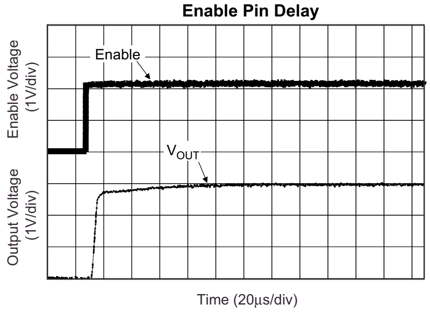
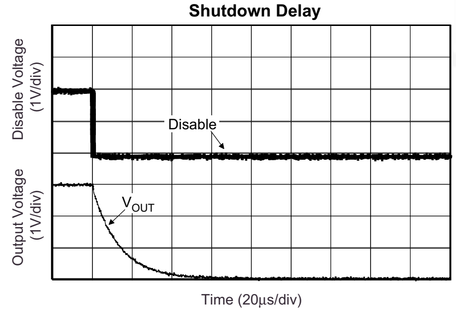


Figure 25. Shutdown Delay



Functional Description

Designed utilizing CMOS process technology, the FAN2504 is carefully optimized for use in compact battery-powered devices, offering a unique combination of low power consumption, extremely low dropout voltages, high tolerance for a variety of output capacitors, and the ability to disable the output to less than 1 µA under user control. In the circuit, a difference amplifier controls the current through a series-pass P-Channel MOSFET, comparing the load voltage at the output with an onboard low-drift band gap reference. The series resistance of the pass P-Channel MOSFET is approximately 1 Ω, resulting in an unusually low dropout voltage under load when compared to older bipolar pass-transistor designs.

Protection circuitry is provided for overload conditions. When the device reaches temperatures exceeding the specified maximums, an onboard circuit shuts down the output, where it remains suspended until it has cooled before re-enabling. The user is also free to shut down the device using the Enable control pin at any time.

Careful design of the output regulator amplifier assures loop stability over a wide range of ESR values in the external output capacitor. A wide range of values and types can be accommodated, allowing the user to select a capacitor meeting space, cost, and performance requirements, and still enjoy reliable operation over temperature, load, and tolerance variations.

Depending on the model selected, a number of control and status functions enhance the operation of the LDO regulator. The Enable pin allows the user to shut-down the regulator output to conserve power, reducing supply current to less than 1 µA. In noise-sensitive applications, an external Bypass capacitor connection is provided that allows the user to achieve optimal noise performance at the output.

Applications Information

External Capacitors – Selection

FAN2504 allows the user to utilize a wide variety of capacitors compared to other LDO products. An innovative design approach offers significantly reduced sensitivity to ESR (Effective Series Resistance), which degrades regulator loop stability in older designs. While the improvements greatly simplify the design task, capacitor quality still must be considered to achieve optimal circuit performance. In general, ceramic capacitors offer superior ESR performance, at a lower cost and a smaller case size than tantalum. Those with X7R or Y5V dielectric offer the best temperature coefficient characteristics. The combination of tolerance and variation over temperature in some capacitor types can result in significant variations, resulting in unstable performance over rated conditions.

Output Capacitor

An output capacitor is required to maintain regulator loop stability. Unlike many other LDO regulators, FAN2504 is nearly insensitive to output capacitor ESR. Stable operation is achieved with a wide variety of capacitors with ESR values ranging from 10 mΩ to 10Ω or more. Tantalum, aluminum electrolytic, or multilayer ceramic can be used. A nominal value of at least 1 µF is recommended.

Bypass Capacitor

In the fixed-voltage configuration, connecting a capacitor between the Bypass pin and ground can significantly reduce noise on the output. Values ranging from 470 pF to 10 nF can be used, depending on the sensitivity to output noise in the application.

At the high-impedance Bypass pin, care must be taken in the circuit layout to minimize noise pickup and capacitors must be selected to minimize current loading (leakage). Noise pickup from external sources can be considerable. Leakage currents into the Bypass pin directly affect regulator accuracy and should be kept as low as possible; high-quality ceramic and film types are recommended for their low leakage characteristics. Cost-sensitive applications not concerned with noise can omit this capacitor.

Control Functions

Enable Pin

Applying a voltage of 0.8 V or less at the Enable pin disables the output, reducing the quiescent output current to less than 1 µA; while a voltage of 1.5 V or greater enables the device. If this shutdown function is not needed, the pin can be connected to the V_{IN} pin. Allowing this pin to float causes erratic operation.

Thermal Protection

FAN2504 is designed to supply high peak output currents of up to 1 A for brief periods. However, this output load causes the device temperature to exceed maximum ratings due to power dissipation. During output overload conditions, when the die temperature exceeds the shutdown limit temperature of 150°C, onboard thermal protection disables the output until the temperature drops below this limit, at which point the output is re-enabled. During a thermal shutdown situation, the user may assert the power-down function at the Enable pin, reducing power consumption to the minimum level $I_{GND} \cdot V_{IN}$.

Thermal Characteristics

FAN2504 is designed to supply 200 mA at the specified output voltage with an operating die (junction) temperature of up to 125°C. Once the power dissipation and thermal resistance is known, the maximum junction temperature of the device can be calculated. While the power dissipation is calculated from known electrical parameters, the thermal resistance is a result of the thermal characteristics of the compact SOT23-5 surface-mount package and the surrounding PC board copper to which it is mounted.

The power dissipation is equal to the product of the input to output voltage differential and the output current, plus the ground current multiplied by the input voltage, or:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN}I_{GND}$$

The ground pin current I_{GND} can be found in the charts provided in the Electrical Characteristics section.

The relationship describing the thermal behavior of the package is:

$$P_{D(max)} = \left\{ \frac{T_{J(max)} - T_A}{\theta_{JA}} \right\}$$

where $T_{J(max)}$ is the maximum allowable junction temperature of the die, which is 125°C, and T_A is the ambient operating temperature. θ_{JA} is dependent on the surrounding PC board layout and can be empirically obtained. While the θ_{JC} (junction-to-case) of the SOT23-5 package is specified at 130°C /W, the θ_{JA} of the minimum PWB footprint will be at least 235°C /W. This can be improved by providing a heat sink of surrounding copper ground on the PWB.

Depending on the size of the copper area, the resulting θ_{JA} can range from approximately 180°C/W for one square inch to nearly 130°C/W for 4 square inches. The addition of backside copper with through-holes, stiffeners, and other enhancements can reduce this value. The heat contributed by the dissipation of other devices nearby must be included in design considerations.

Once the limiting parameters in these two relationships have been determined, the design can be modified to ensure that the device remains within specified operating conditions at all times.

If overload conditions are not considered, it is possible for the device to enter a thermal cycling loop, in which the circuit enters a shutdown condition, cools, re-enables, and then again overheats and shuts down repeatedly due to an unmanaged fault condition.

General PWB Layout Considerations

To achieve the full performance of the device, careful circuit layout and grounding technique must be observed. Establishing a small local ground, to which the GND pin, the output, and bypass capacitors are connected; is recommended, while the input capacitor should be grounded to the main ground plane. The quiet local ground is then routed back to the main ground plane using feed-through vias. In general, the high-frequency compensation components (input, bypass, and output capacitors) should be located as close to the device as possible. The proximity of the output capacitor is especially important to achieve optimal noise compensation from the onboard error amplifier, especially during high load conditions. A large copper area in the local ground provides the heat sinking discussed above when high power dissipation significantly increases the temperature of the device. Component-side copper provides significantly better thermal performance for this surface-mount device, compared to that obtained when using only copper planes on the underside.

Physical Dimensions

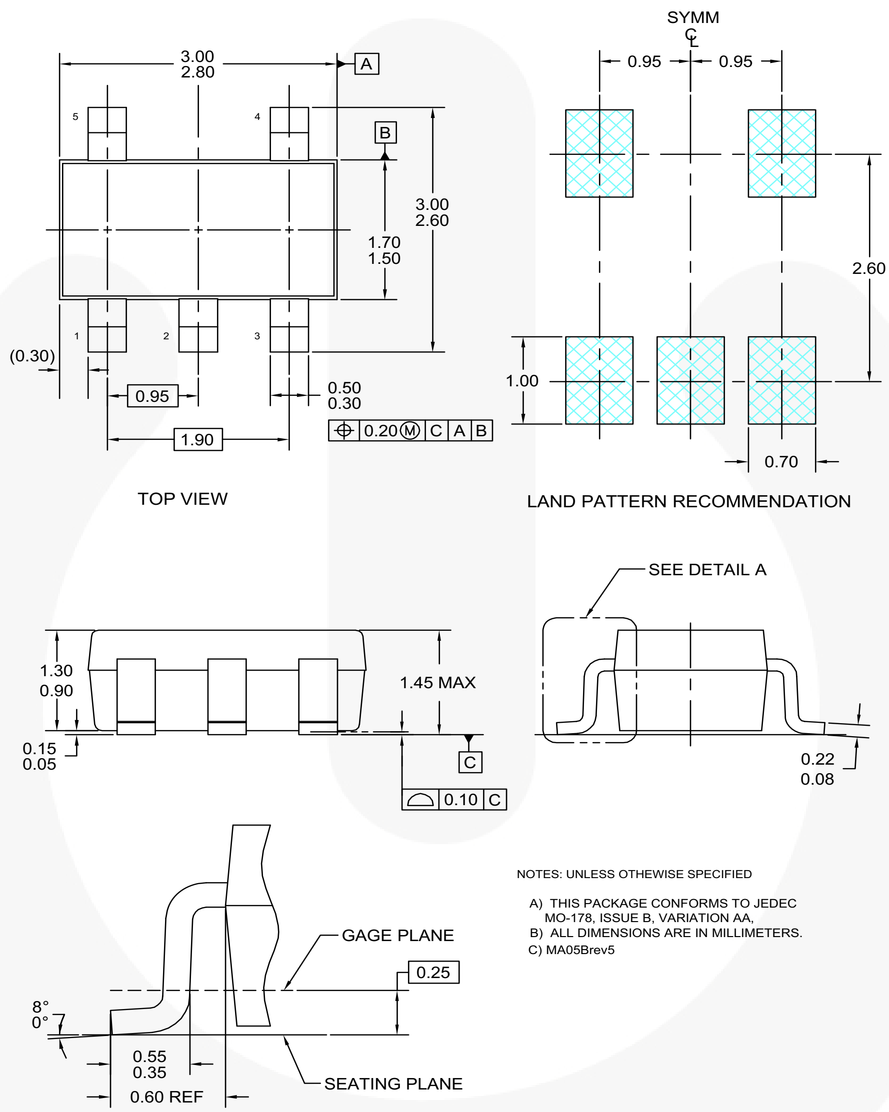


Figure 26. 5-Lead, SOT-23, JEDEC MO-178, 1.6mm

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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TinyBuck™
TinyCalc™
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TINYOPTO™
TinyPower™
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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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