SONY

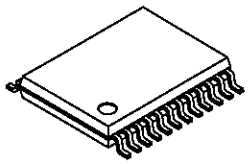
CXA2096N

Digital CCD Camera Head Amplifier

Description

The CXA2096N is a bipolar IC developed as a head amplifier for digital CCD cameras. This IC provides the following functions: correlated double sampling, AGC for the CCD signal, A/D sample and hold, blanking, A/D reference voltage, and an output driver.

24 pin SSOP (Plastic)



Features

- High sensitivity made possible by a high-gain AGC amplifier
- Blanking function provided for the purpose of calibrating the CCD output signal black level
- Regulator output pin provided for A/D converter reference voltage
- Built-in sample-and-hold circuits for camera signals required by external A/D converters

Absolute Maximum Ratings

• Supply voltage	V_{CC}	11	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	P_D	417	mW

Operating Conditions

Supply voltage	V_{CC}1, 2, 3	3.0 to 3.6	V

Applications

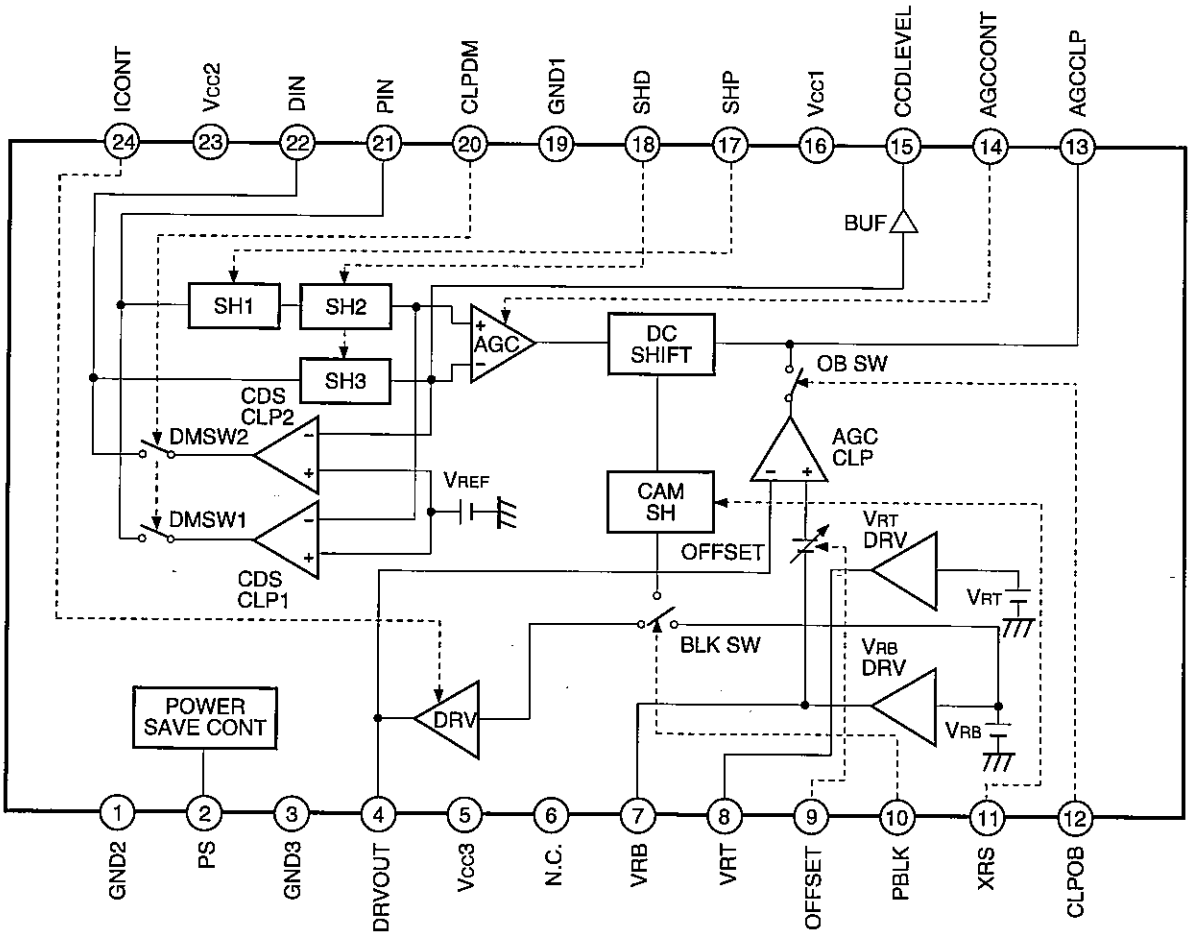
DVC/still cameras for consumer use

Structure

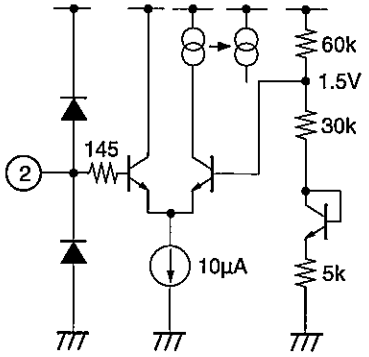
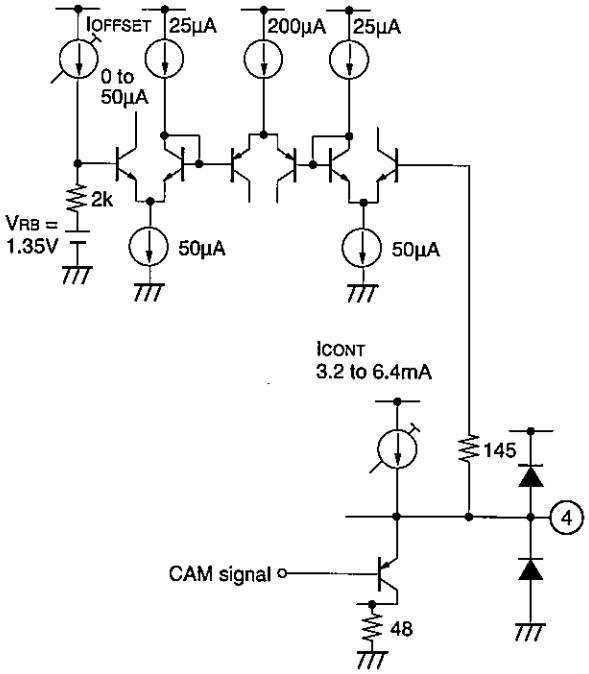
Bipolar silicon monolithic IC

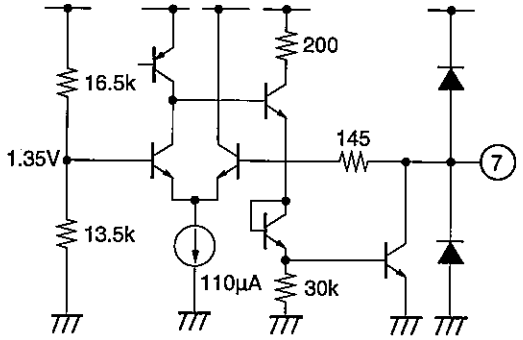
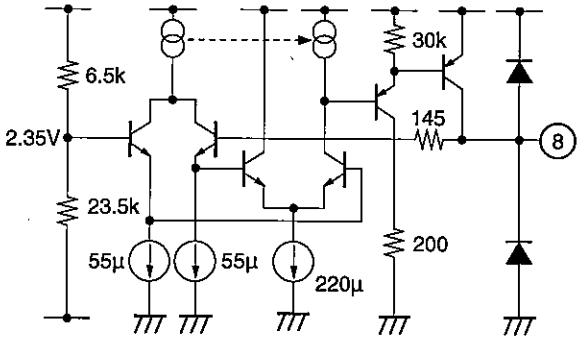
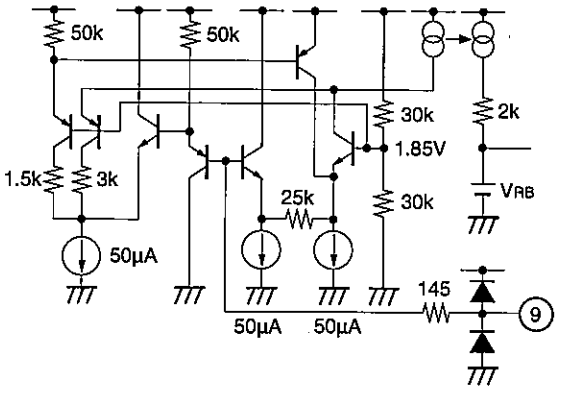
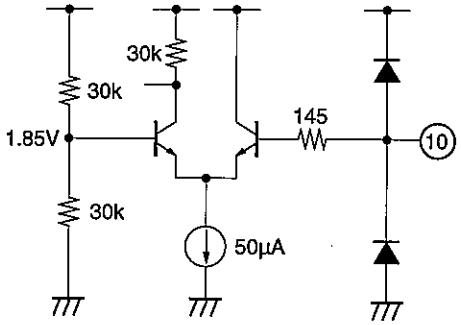
E97449C1Z

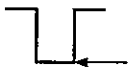
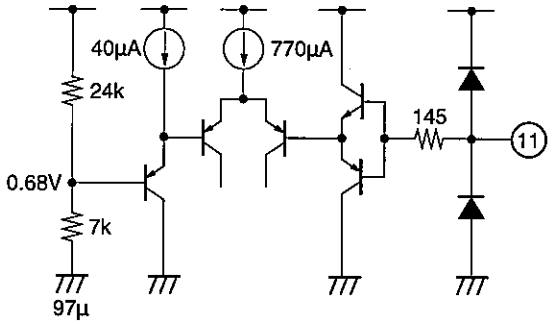
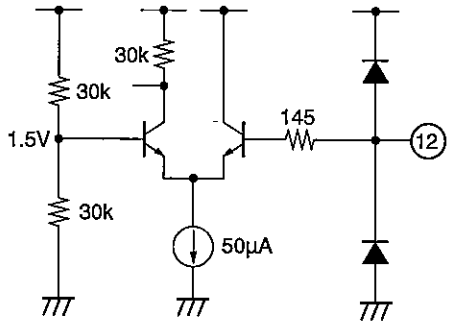
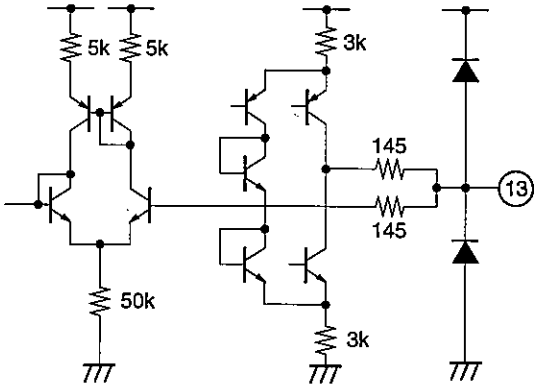
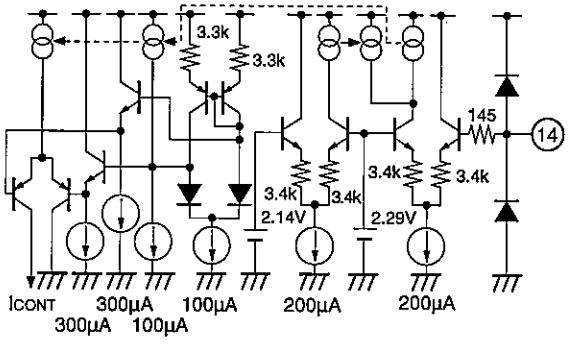
Block Diagram and Pin Configuration

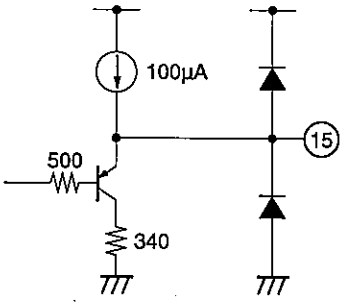
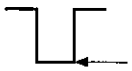
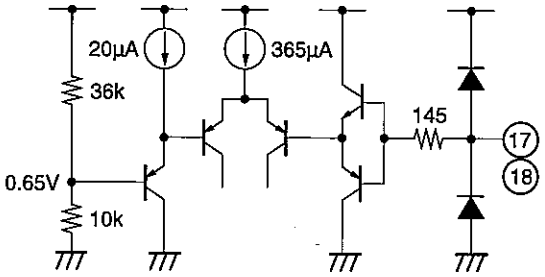
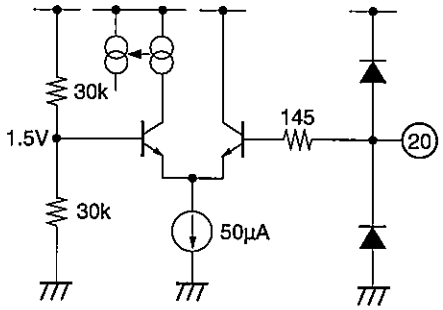
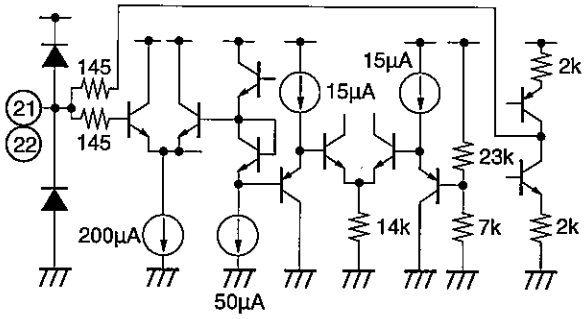
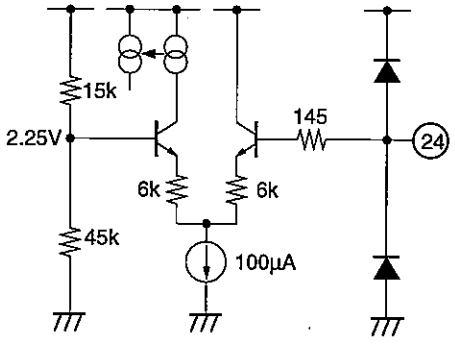


Pin Description (Vcc1, 2, 3 = 3V)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1 3 19	GND2 GND3 GND1	GND		Ground.
2	PS	VTH = 1.5V		Power saving mode.
4	DRVOUT	V_{RB} to V_{RB} + 100mV		Driver output for A/D converter capable of DC coupling. Dynamic range = 1Vp-p.
5 16 23	Vcc3 Vcc1 Vcc2	Vcc		Power supply.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	N.C.			No connection; normally ground.
7	VRB	1.35V		1.35V regulator output. Be sure to decouple this pin near the IC pins to prevent the oscillation and external noise when this pin is not used. (Recommended capacitor value: 4.7µF)
8	VRT	2.35V		2.35V regulator output. Be sure to decouple this pin near the IC pins to prevent the oscillation and external noise when this pin is not used. (Recommended capacitor value: 4.7µF)
9	OFFSET	1.5 to 3V & 0V		Controls the output offset. When 3V: V_{RB} When 1.5V: V_{RB} + 100mV When 0V (preset mode): V_{RB} + 35mV
10	PBLK	VTH = 1.85V Active: Low		Camera signal preblanking pulse input. Active when Low. Calibrates the black level of the AGC output waveform. When PBLK is Low, the DRVOUT potential is forced to V_{RB}.

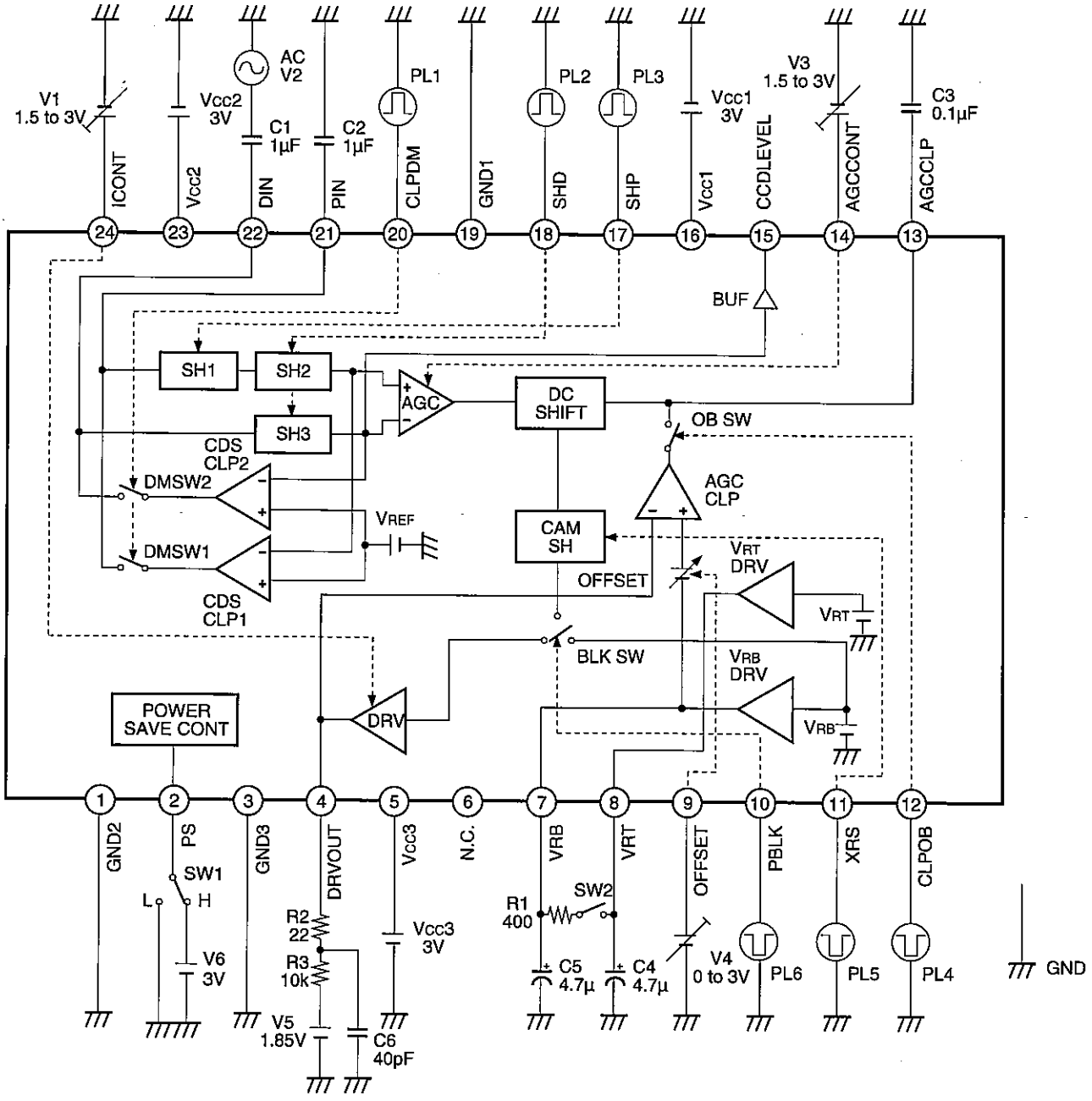
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11	XRS	VTH = 0.68V  Sampling		Camera signal sample-and-hold pulse input.
12	CLPOB	VTH = 1.5V  Active: Low		Clamp pulse used to clamp the optical black portion of the camera signal after it passes through the AGC amplifier.
13	AGCCLP	Approx. 1.3V		AGC clamp capacitor. (Recommended value: 0.1µF)
14	AGCCONT	1.5 to 3.0V		AGC gain control. When 1.5V: –1dB (Minimum gain) When 3.0V: 31.5dB (Maximum gain)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	CCDLEVEL	CCD signal black level of DIN input approx. 2.2V		Enables monitoring of the SH3 output camera signal.
17	SHP	VTH = 0.65V  Sampling		Preset level sample-and-hold pulse input.
18	SHD			Data level sample-and-hold pulse input.
20	CLPDM	VTH = 1.5V  Active: Low		Clamp pulse used to clamp the dummy pixel portion of the input CCD signal.
21 22	PIN DIN	Black level approx. 2.1V		CCD signal input.
24	ICONT	1.5 to 3V		DRVOUT output waveform rise time control. When 1.5V: Maximum rise time When 3V: Minimum rise time

Electrical Characteristics (Ta = 25°C, Vcc1, 2, 3 = 3V)

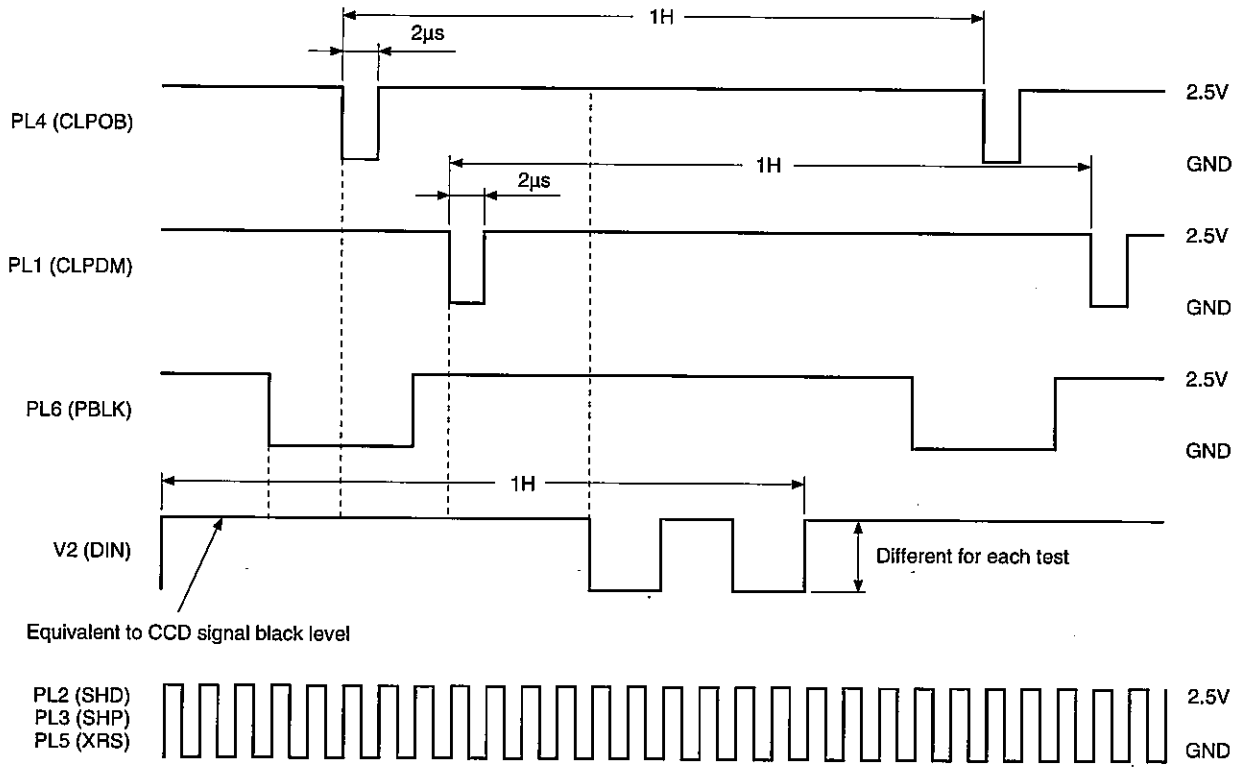
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consump-tion	PS = OFF (PS indicates Power Save)	I_{DC}	AGCCONT = 1.5V, open between V_{RT} and V_{RB} PS = 3V, I_{CONT} = 3V	25.1	37.1	49.0	mA
	PS = ON	I_{DP}	PS = 0V	0	1.8	4.2	
AGC	Maximum gain	A CONT max.	DIN = 1µs, 20mVp-p pulse AGCCONT = 3V, I_{CONT} = 3V	28.5	31.3	—	dB
	Minimum gain	A CONT min.	DIN = 1µs, 500mVp-p pulse AGCCONT = 1.5V, I_{CONT} = 3V	—	–0.8	1.4	
	Range of gain variance	AGC G	A CON max. – A CON min.	27.1	32.1	—	
	Dynamic range maximum	AGCmax. D	AGCCONT = 3V DRVOUT output signal at saturation level	800	970	—	mV
	Dynamic range typical	$AGC_{TYP.}$ D	AGCCONT = 2V DRVOUT output signal at saturation level	900	960	—	
DRV	Offset high	CAOF high	OFFSET = 1.5V	80	98	—	mV
	Offset low	CAOF low	OFFSET = 3.0V	—	2	5	
	Offset preset	CAOF pre	OFFSET = 0V	25	34	40	
REF	V_{RT} DC level	VRTO	With a 400Ω load	2300	2340	2400	mV
	V_{RB} DC level	VRBO	With a 400Ω load	1300	1353	1400	
	$V_{RT} - V_{RG}$	ΔVR	With a 400Ω load	950	988	1050	
BLK	Offset	BLKOF	BLKOF (PBLK = 3V) – BLKOF (PBLK = 0V)	–15	9	30	mV
SH3	Dynamic range	SH3 D	DIN = 1µs, 1Vp-p pulse	600	790	—	mV

Electrical Characteristics Measurement Circuit

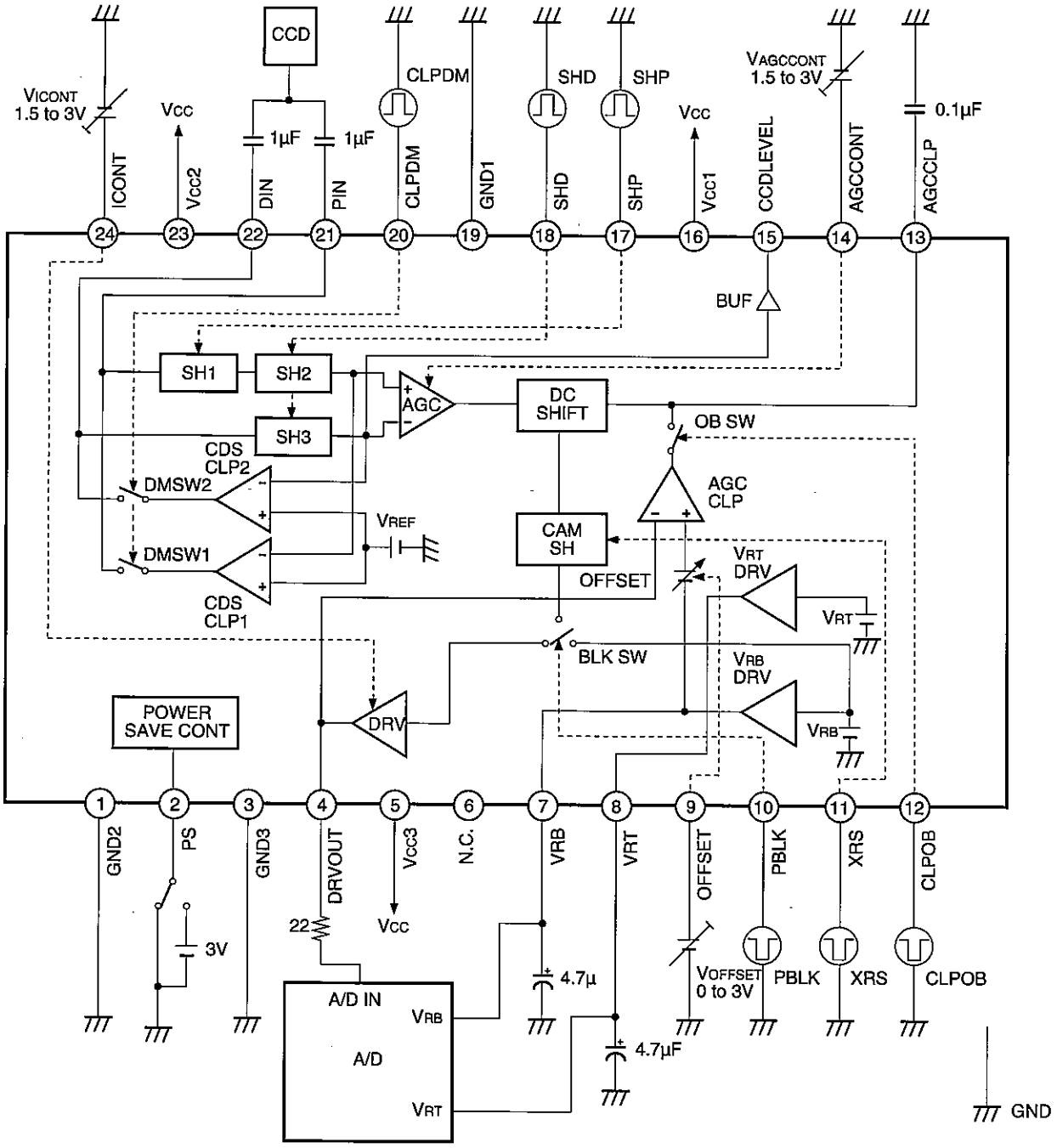


SW1	POWER SAVE
H	OFF
L	ON

Measurement Timing Chart



Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

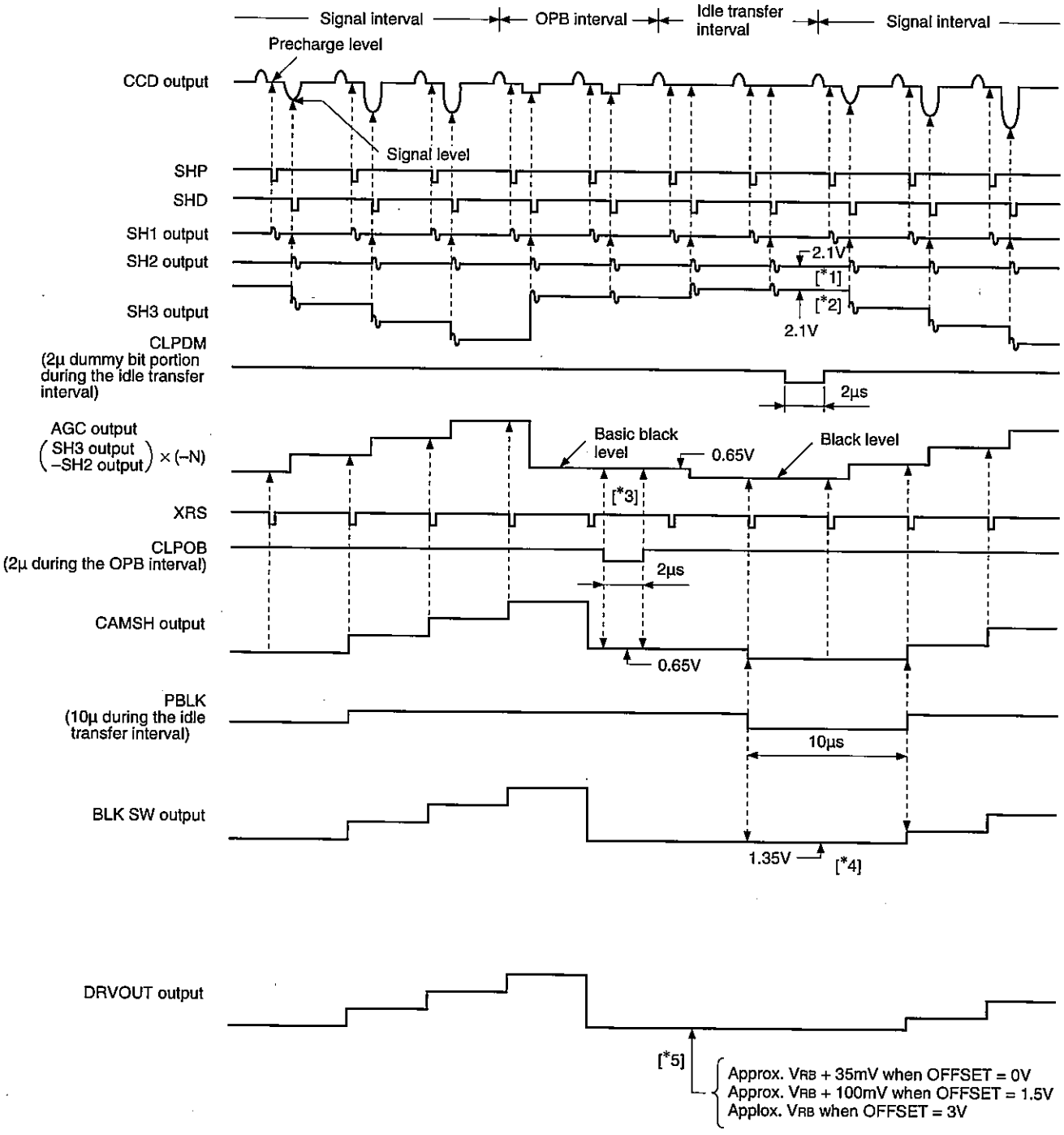
Description of Operation

Refer to the Block Diagram.

Operating Conditions

The camera signal processing system operates when PS is High.

Timing Chart (when Vcc = 3V)



CDS (SH1, SH2, SH3):
The CCD signal from the CCD image sensor is input to PIN and DIN where correlated double sampling (CDS) is performed by SH1, SH2 and SH3. The precharge level of the CCD output signal is sampled, held and output by the SH2 output, and the signal level is sampled, held and output by the SH3 output. SH1 and SH2 are the sample-and-hold circuits for the precharge level; SH3 is the sample-and-hold circuit for the signal level.

CDSCLP 1, 2:
CDSCLP1 and 2 stabilize the input signal DC level, clamp (CLPDM) the input signal during the idle transfer interval for the purpose of eliminating the AGC input offset, and adjust the DC level ([*1], [*2]) of SH2 and SH3 in line with V_{REF}. CDSCLP1 is the clamp circuit for the precharge level, and CDSCLP2 is the clamp circuit for the signal level.

AGC:
AGC is the gain control amplifier for the camera signal.
The gain can be varied from –1 to +31dB by adjusting the AGCCONT voltage control $V_{AGCCONT}$ from 1.5 to 3.0V.

CAM SH:
CAM SH is the sample-and-hold circuit for synchronizing the data read-in timing for the external A/D. Sampling is possible according to the approximately 10ns sampling pulse width input to XRS.

AGCCLP:
The basic black level is set ([*3]) by clamping the AGC output waveform with the CLPOB clock during the OPB interval. When PBLK is High and CLPOB is Low, the clamping circuit operates, adjusting the AGCCLP current so that the DRVOUT potential equals the OFFSET potential (which is determined by the voltage applied to the OFFSET pin), thus setting the AGCCLP potential. The AGCCLP capacitance is connected to the AGCCLP pin.

DC SHIFT:
This circuit functions when AGCCLP operates, following the AGCCLP potential and forcing a DC shift of the AGC output waveform OPB interval to the basic black level. When AGCCLP is not operating, the basic black level is maintained at its previous setting.

BLK SW:
The black level is calibrated by blanking the black level signal of the AGC output waveform so that it does not fall below the basic black level and replacing the DC potential with V_{RB}. ([*4])
The signal is blanked when PBLK is Low.

OFFSET:
OFFSET controls the DRV output waveform black level offset.
The offset of the DRVOUT camera signals can be adjusted when a voltage is applied to OFFSET. ([*5])
The voltage controlled by OFFSET is output as the DRV output DC offset via AGCCLP, DCSHIFT, CAMSH and BLKSW.
When the OFFSET voltage is 1.5 to 3.0V, DRVOUT DC can vary in a linear fashion from V_{RB} + 100mV to V_{RB}.
In addition, when the OFFSET voltage is 0V, DRVOUT DC is preset to V_{RB} + 35mV.

DRV:

DRV drives the external A/D. The current that flows to the last-stage amplifier in DRV is controlled by applying voltage to the ICONT pin, making it possible to adjust the rise time of the output waveform, which affects the external A/D load capacitance. The variable range is 1.5 to 3V, with 1.5V yielding the maximum and 3V yielding the minimum. The optimum rise time for the external A/D input capacitance can be selected.

V_{RT}DRV, V_{RB}DRV:

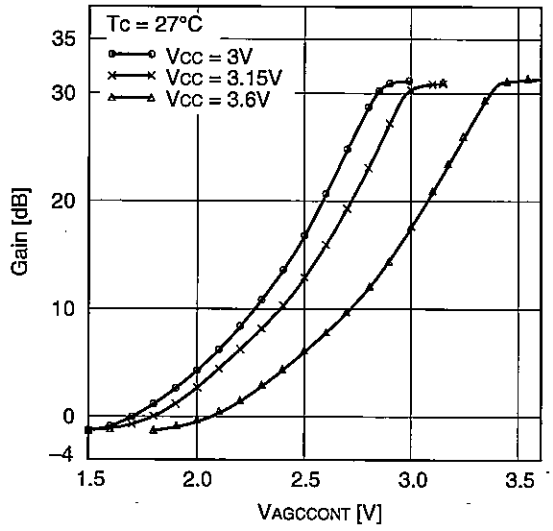
These are the external A/D reference voltage drivers. These circuits are connected to A/D V_{RT} and V_{RB}, supplying 2.35V and 1.35V, respectively, when V_{CC} is 3V. The IC's internal primary voltage is also generated on the basis of the V_{RT} and V_{RB} voltage. (V_{RB}, V_B and V_{CENT})

POWER SAVE CONTROL:

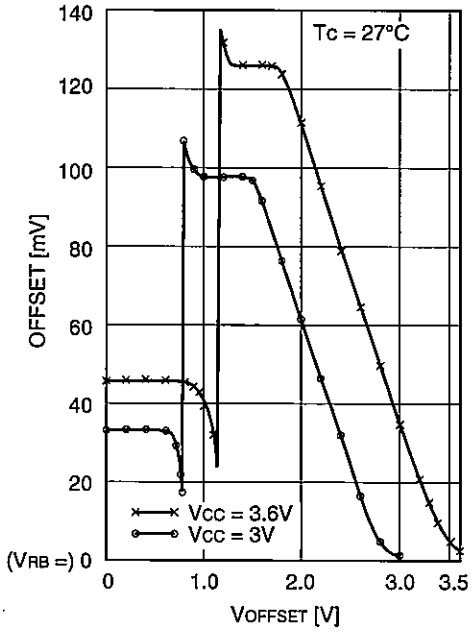
The PS pin is the power save pin; the operating state is enabled when this pin is High, while the power saving function operates when it is Low.

Characteristics Graphs

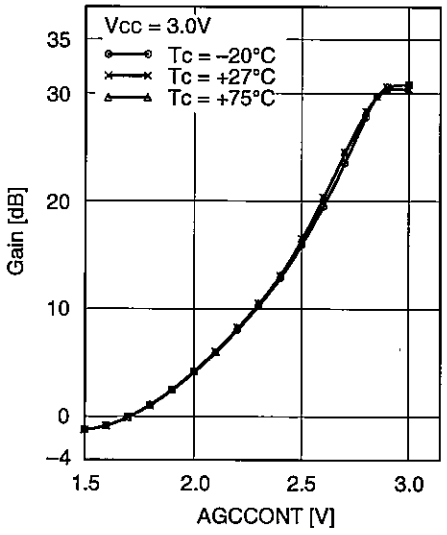
AGCCONT control supply voltage characteristics
$V_{AGCCONT}$ vs. Gain



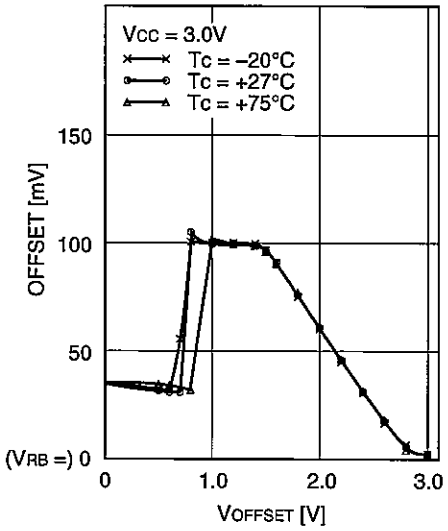
OFFSET control supply voltage characteristics
V_{OFFSET} vs. OFFSET



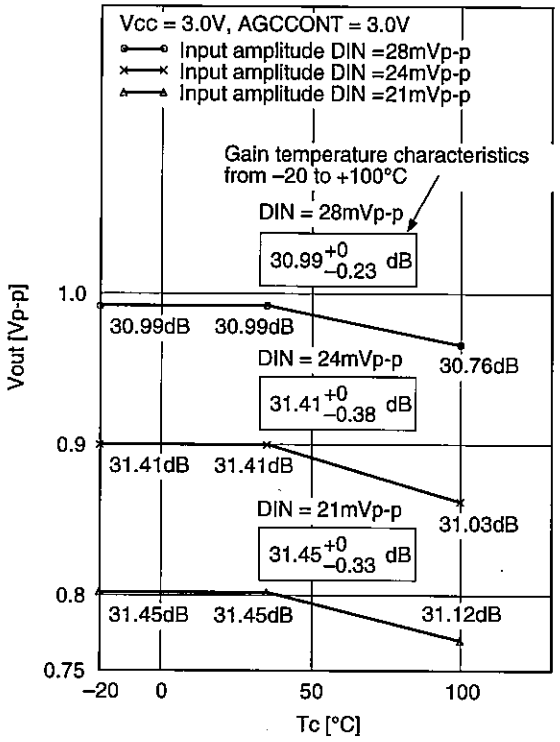
AGCCONT control temperature characteristics
AGCCONT vs. Gain



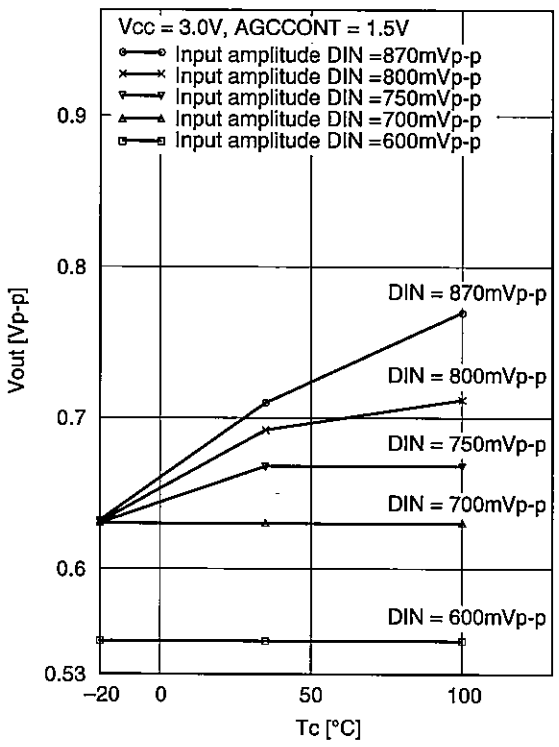
OFFSET control temperature characteristics
V_{OFFSET} vs. OFFSET



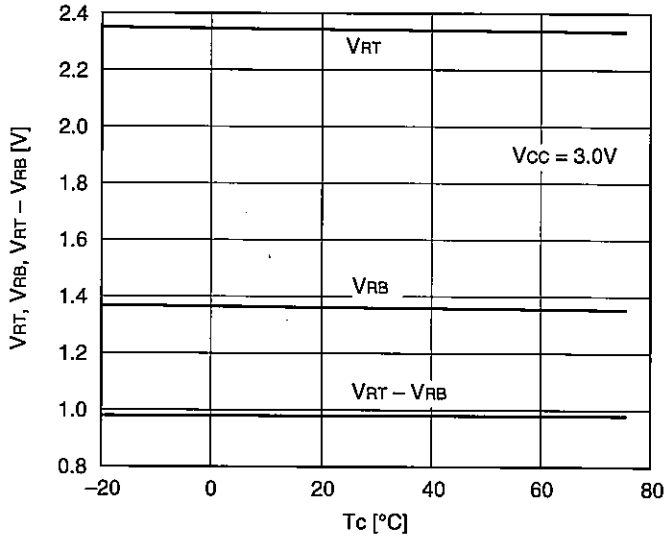
Maximum signal amplitude temperature characteristics (Max. gain) Tc vs. Vout



Maximum signal amplitude temperature characteristics (Min. gain) Tc vs. Vout



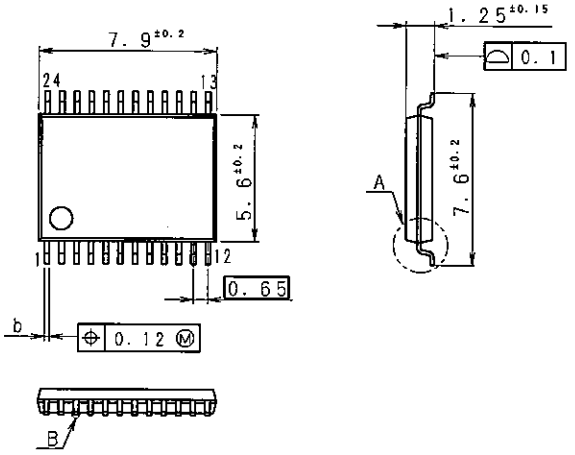
VRT, VRB, VRT – VRB temperature characteristics Tc vs. VRT, VRB, VRT – VRB

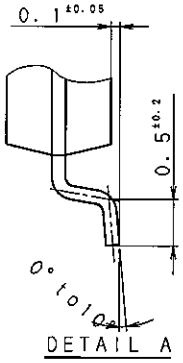


Package Outline Unit: mm

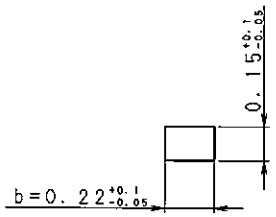
Ass'y: AOI

24PIN SSOP (PLASTIC)





DETAIL A



DETAIL B

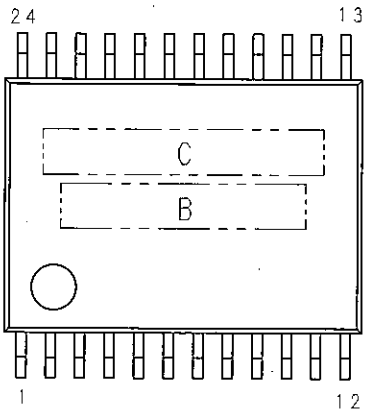
SONY CODE	SSOP-24P-L381
JEITA CODE	P-SSOP24-7.9X5.6-0.65
JEDEC CODE	———

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.13g

PART No. AP-2000-24MAN2		Rev. 0
ISSUED 10.09.10	REVISED -	
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR KYUSHU.	
REMARKS PKG CODE SM-024-CAN		

Marking



MARKING C: CXA2096N

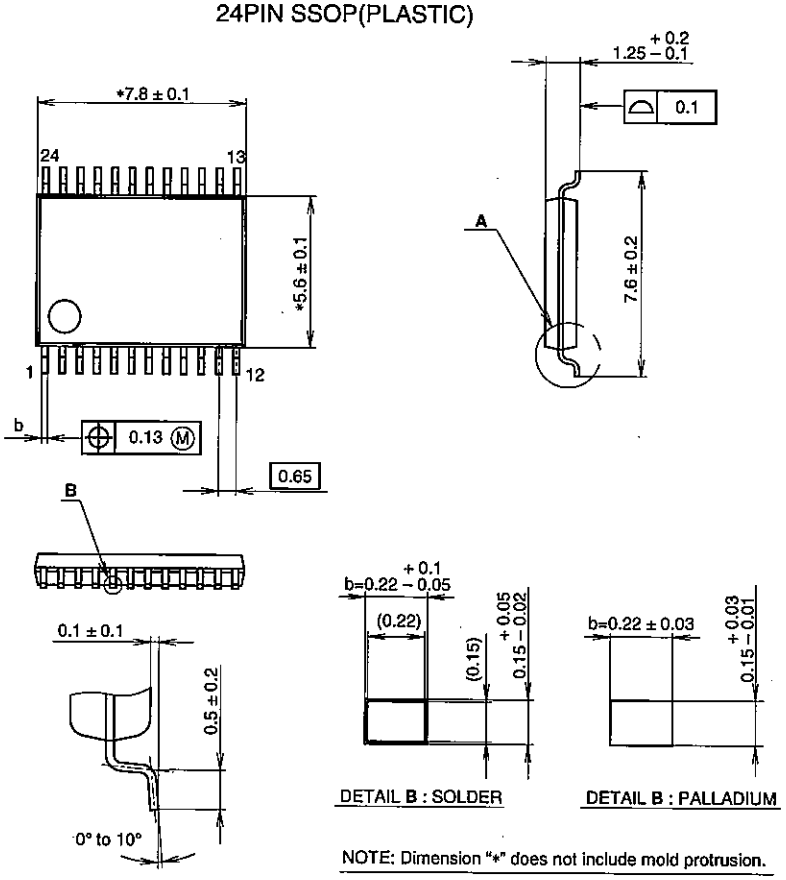
注1) C部は製品名 (Max 8文字) を配置する.
(8文字を超える場合は製品名省略指示規定に従う.)
2) B部はロット番号 (Max 7文字) を配置する.

< INSTRUCTIONS >
1) TYPE NO. (MAX 8 CHARACTERS) IN SECTION C.
(FOR MORE THAN 8 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B.

Package Outline Unit: mm

Ass'y: SDT

24PIN SSOP(PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

DETAIL A

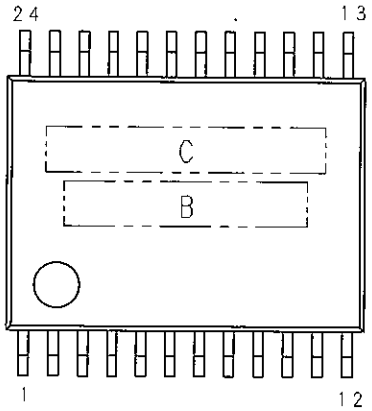
SONY CODE	SSOP-24P-L01
EIAJ CODE	SSOP024-P-0056
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).

Marking



MARKING C: CXA2096N

注1) C部は製品名(Max8文字)を配置する.
(8文字を超える場合は製品名省略標示規定に従う.)
2) B部はロット番号(Max7文字)を配置する.

< INSTRUCTIONS >
1) TYPE NO. (MAX 8 CHARACTERS) IN SECTION C.
(FOR MORE THAN 8 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) LOT NO. (MAX 7 CHARACTERS) IN SECTION B.