

## DS96172/DS96174 RS-485/RS-422 Quad Differential Line Drivers

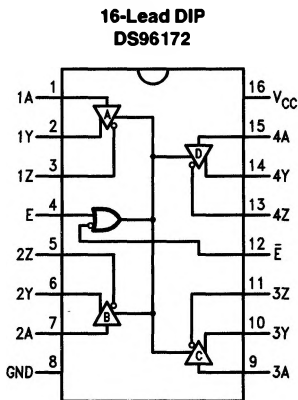
### General Description

The DS96172 and DS96174 are high speed quad differential line drivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to -7.0V common mode range. A thermal shutdown feature is also provided and occurs at junction temperature of approximately 160°C. The DS96172 features an active high and active low Enable, common to all four drivers. The DS96174 features separate active high Enables for each driver pair. Compatible RS-485 receivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96173, DS96175, DS96176 AND DS96177.

### Features

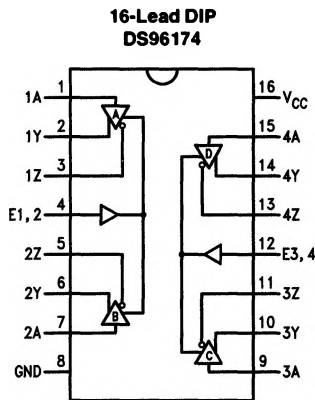
- Meets EIA Standard RS-485 and RS-422A
- Monotonic differential output switching
- Transmission rate to 10 Mbs
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: -7V to +12V
- Operates from single +5V supply
- Thermal shutdown protection
- DS96172/DS96174 are lead and function compatible with the SN75172/75174 or the AM26LS31/MC3487 respectively

### Connection Diagrams



Top View

TL/F/9626-1



Top View

TL/F/9626-2

**Order Number DS96172CJ or DS96174CJ**  
**See NS Package Number J16A**  
**Order Number DS96172CN or DS96174CN**  
**See NS Package Number N16A**

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                  |                 |
|----------------------------------|-----------------|
| Storage Temperature Range        |                 |
| Ceramic DIP                      | -65°C to +175°C |
| Molded DIP                       | -65°C to +150°C |
| Operating Temperature Range      | 0°C to +70°C    |
| Lead Temperature                 |                 |
| Ceramic DIP (soldering, 60 sec.) | 300°C           |
| Molded DIP (soldering, 10 sec.)  | 265°C           |
| Supply Voltage                   | 7V              |
| Enable Input Voltage             | 5.5V            |
| Maximum Power Dissipation*       | 25°C            |
| J-Cavity Package                 | 1.74W           |
| N-Molded Package                 | 1.98W           |

\*Derate cavity package 14 mW/°C above 25°C; derate molded DIP package 16 mW/°C above 25°C.

**Recommended Operating Conditions**

|                                         | Min  | Typ | Max  | Units |
|-----------------------------------------|------|-----|------|-------|
| Supply Voltage ( $V_{CC}$ )             | 4.75 | 5   | 5.25 | V     |
| Common Mode Output Voltage ( $V_{OC}$ ) | -7   |     | +12  | V     |
| Output Current HIGH ( $I_{OH}$ )        |      |     | -60  | mA    |
| Output Current LOW ( $I_{OL}$ )         |      |     | 60   | mA    |
| Operating Temperature ( $T_A$ )         | 0    | 25  | 70   | °C    |

**Electrical Characteristics**

over recommended temperature and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

| Symbol           | Parameter                                                   | Conditions                                 | Min             | Typ      | Max       | Units   |
|------------------|-------------------------------------------------------------|--------------------------------------------|-----------------|----------|-----------|---------|
| $V_{IH}$         | Input Voltage HIGH                                          |                                            | 2               |          |           | V       |
| $V_{IL}$         | Input Voltage LOW                                           |                                            |                 |          | 0.8       | V       |
| $V_{OH}$         | Output Voltage HIGH                                         | $I_{OH} = -20$ mA                          |                 | 3.1      |           | V       |
| $V_{OL}$         | Output Voltage LOW                                          | $I_{OL} = 20$ mA                           |                 | 0.8      |           | V       |
| $V_{IC}$         | Input Clamp Voltage                                         | $I_I = -18$ mA                             |                 |          | -1.5      | V       |
| $ V_{OD1} $      | Differential Output Voltage                                 | $I_O = 0$ mA                               |                 |          | 6         | V       |
| $ V_{OD2} $      | Differential Output Voltage                                 | $R_L = 54\Omega$ , Figure 1                | 1.5             | 2        |           | V       |
|                  |                                                             | $R_L = 100\Omega$ , Figure 1               | 2               | 2.3      |           | V       |
| $\Delta V_{OD} $ | Change in Magnitude of Differential Output Voltage (Note 4) | $R_L = 54\Omega$ or $100\Omega$ , Figure 1 |                 |          | $\pm 0.2$ | V       |
| $V_{OC}$         | Common Mode Output Voltage (Note 5)                         | $R_L = 54\Omega$ , Figure 1                |                 |          | 3         | V       |
| $\Delta V_{OC} $ | Change in Magnitude of Common Mode Output Voltage (Note 4)  |                                            |                 |          | $\pm 0.2$ | V       |
| $I_O$            | Output Current with Power Off                               | $V_{CC} = 0V$ , $V_O = -7.0V$ to $12V$     |                 |          | $\pm 100$ | $\mu A$ |
| $I_{OZ}$         | High Impedance State Output Current                         | $V_O = -7.0V$ to $12V$                     |                 | $\pm 50$ | $\pm 200$ | $\mu A$ |
| $I_{IH}$         | Input Current HIGH                                          | $V_I = 2.7V$                               |                 |          | 20        | $\mu A$ |
| $I_{IL}$         | Input Current LOW                                           | $V_I = 0.5V$                               |                 |          | -100      | $\mu A$ |
| $I_{OS}$         | Short Circuit Output Current (Note 6)                       | $V_O = -7.0V$                              |                 |          | -250      | mA      |
|                  |                                                             | $V_O = 0V$                                 |                 |          | -150      |         |
|                  |                                                             | $V_O = V_{CC}$                             |                 |          | 150       |         |
|                  |                                                             | $V_O = 12V$                                |                 |          | 250       |         |
| $I_{CC}$         | Supply Current (All Drivers)                                | No Load                                    | Outputs Enabled | 50       | 70        | mA      |
|                  |                                                             |                                            | Output Disabled | 50       | 60        |         |

## Switching Characteristics $V_{CC} = 5V, T_A = 25^\circ C$

| Symbol    | Parameter                                        | Conditions                   | Min | Typ | Max | Units |
|-----------|--------------------------------------------------|------------------------------|-----|-----|-----|-------|
| $t_{DD}$  | Differential Output Delay Time                   | $R_L = 60\Omega$ , Figure 2  |     | 15  | 25  | ns    |
| $t_{TD}$  | Differential Output Transition Time              |                              |     | 15  | 25  | ns    |
| $t_{PLH}$ | Propagation Delay Time, Low-to-High Level Output | $R_L = 27\Omega$ , Figure 3  |     | 12  | 20  | ns    |
| $t_{PHL}$ | Propagation Delay Time, High-to-Low Level Output |                              |     | 12  | 20  | ns    |
| $t_{PZH}$ | Output Enable Time to High Level                 | $R_L = 110\Omega$ , Figure 4 |     | 30  | 45  | ns    |
| $t_{PZL}$ | Output Enable Time to Low Level                  | $R_L = 110\Omega$ , Figure 5 |     | 30  | 45  | ns    |
| $t_{PHZ}$ | Output Disable Time from High Level              | $R_L = 110\Omega$ , Figure 4 |     | 25  | 35  | ns    |
| $t_{PLZ}$ | Output Disable Time from Low Level               | $R_L = 110\Omega$ , Figure 5 |     | 30  | 45  | ns    |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:** Unless otherwise specified min/max limits apply across the  $0^\circ C$  to  $+70^\circ C$  range for the DS96172/DS96174. All typicals are given for  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .

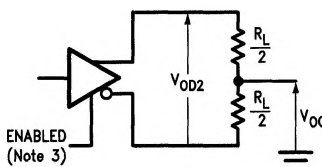
**Note 3:** All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

**Note 4:**  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$  respectively, that occur when the input is changed from a high level to a low level.

**Note 5:** In EIA Standards RS-422A and RS-485,  $V_{OC}$ , which is the average of the two output voltages with respect to ground, is called output offset voltage,  $V_{OS}$ .

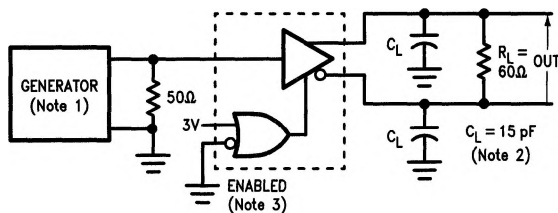
**Note 6:** Only one output at a time should be shorted.

## Parameter Measurement Information



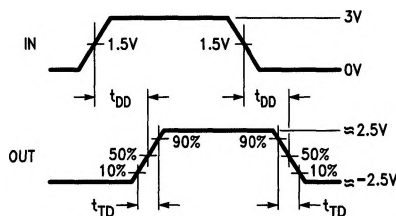
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FIGURE 1. Differential and Common Mode Output Voltage



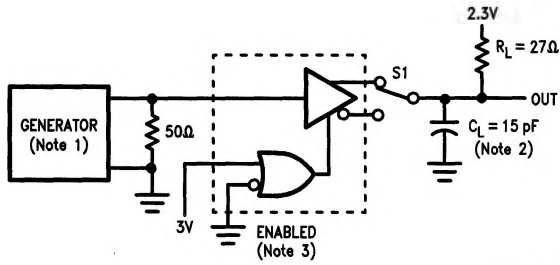
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FIGURE 2. Differential Output Delay and Transition Times

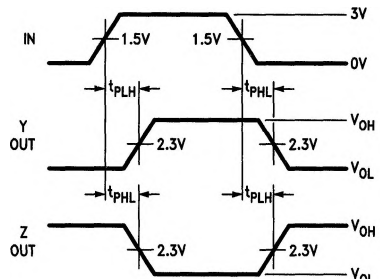


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Parameter Measurement Information (Continued)

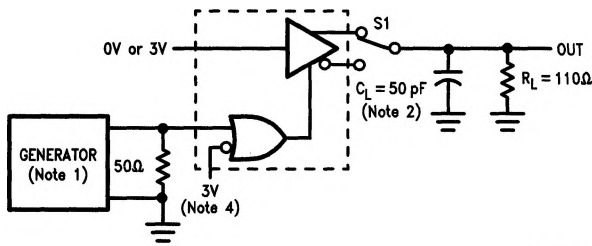


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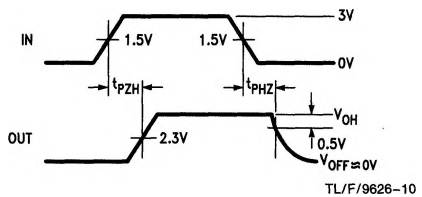
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FIGURE 3. Propagation Delay Times

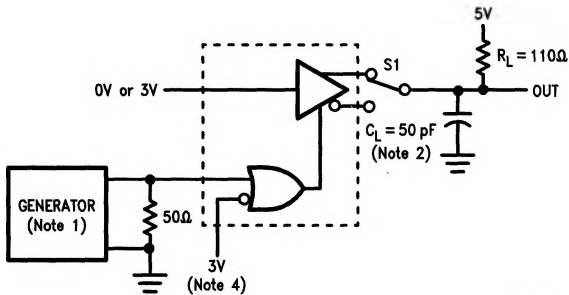


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FIGURE 4.  $t_{pZH}$  and  $t_{pHZ}$

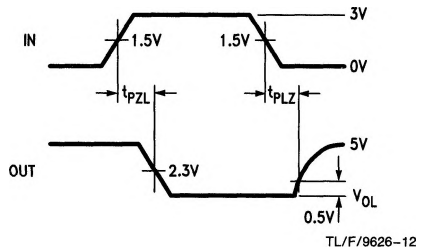


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FIGURE 5.  $t_{pZL}$  and  $t_{pLZ}$



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**Note 1:** The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle = 50%,  $t_r \leq 5.0$  ns,  $t_f \leq 5.0$  ns,  $Z_0 = 50\Omega$ .

**Note 2:**  $C_L$  includes probe and jig capacitance.

**Note 3:** DS96172 with active high and active low Enables is shown here. DS96174 has active high Enable only.

**Note 4:** To test the active low Enable  $\bar{E}$  of DS96172, ground E and apply an inverted waveform to  $\bar{E}$ . DS96174 has active high Enable only.

## Function Tables

DS96172

| Input<br>A | Enables |   | Outputs |   |
|------------|---------|---|---------|---|
|            | E       | E | Y       | Z |
| H          | H       | X | H       | L |
| L          | H       | X | L       | H |
| H          | X       | L | H       | L |
| L          | X       | L | L       | H |
| X          | L       | H | Z       | Z |

DS96174

| Input | Enable | Outputs |   |
|-------|--------|---------|---|
|       |        | Y       | Z |
| H     | H      | H       | L |
| L     | H      | L       | H |
| X     | L      | Z       | Z |

H = High Level  
L = Low Level

X = Immaterial  
Z = High Impedance (off)

## Typical Application

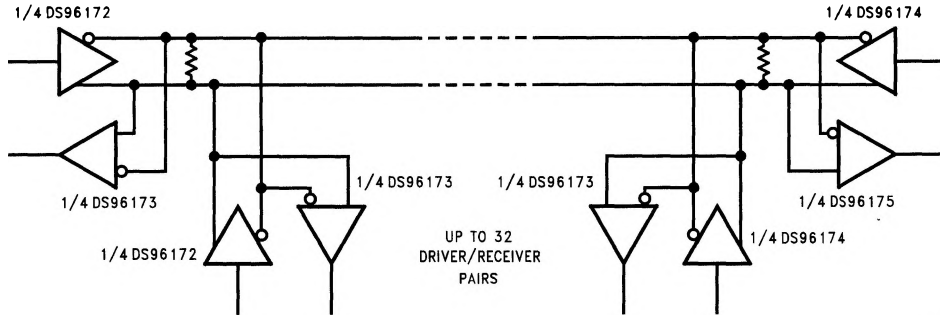


FIGURE 6

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**Note:** The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.