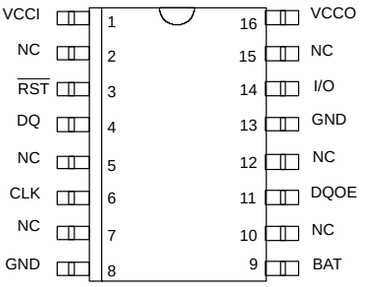
DALLAS SEMICONDUCTOR

# DS1205S
MultiKey Chip

## FEATURES

- Three secure read/write data partitions of 384 bits each
- One non-secure read/write data partition of 512 bits
- Secure data cannot be deciphered by reverse engineering
- Guaranteed unique, 48-bit, laser etched serial number
- 64-bit password and I.D. fields provide positive identification and security for each secure data partition
- Maximum data transfer rate of 2 million bits/second
- Low-power CMOS circuitry
- Access via 3-wire or 1-wire interface
- Applications include proprietary data, financial transactions, secure personnel areas, and systems access control

## PIN ASSIGNMENT




DS1205S 16-Pin SOIC (300 mil)
See Mech. Drawings Section

## PIN DESCRIPTION

| | | |
|---|---|---|
| $V_{CCI}$ | – | +5V Supply (Battery Backup Mode) |
| $\overline{RST}$ | – | Reset (3-Wire) |
| DQ | – | Data (3-Wire) |
| CLK | – | Clock (3-Wire) |
| GND | – | Ground |
| BAT | – | Battery (+) (Battery Backup Mode) |
| DQOE | – | Data Available (3-Wire) |
| I/O | – | Data I/O (1-Wire) |
| $V_{CCO}$ | – | Battery (+) (Battery Powered Mode) |

## DESCRIPTION

The DS1205S MultiKey Chip is an enhanced version of the DS1204U Electronic Key which has both a standard 3-wire interface (data, clock, and reset) and a 1-wire interface. The DS1205S MultiKey has three secure read/write subkeys which are each 384 bits in length. In addition, there is a 512-bit read/write scratchpad which can be used as a non-secure data area or as a holding register for data transfer to one of the three subkeys. Each subkey within the part is uniquely addressable on byte boundaries.

## OPERATING MODES

There are two modes of operation for powering the DS1205S MultiKey Chip. In the Normal Mode (Battery Backup), $V_{CC}$ power is supplied to the part on the $V_{CCI}$ pin, while the battery backup source is applied to the BAT pin. In this mode of operation, the chip supply is switched internally between $V_{CCI}$ and BAT (depending on which is higher) and this level is presented internally to the $V_{CCO}$ pin. In the Battery Operate Mode, the battery supply is connected directly to the $V_{CCO}$ pin while the $V_{CCI}$ and BAT pins are grounded.

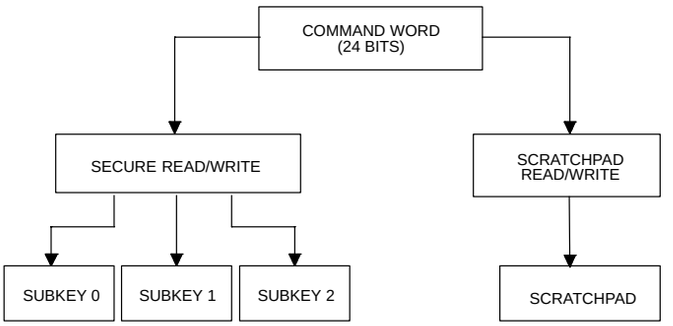
## INTERFACES

Two interfaces to the DS1205S are provided. The 1-wire interface requires a 1-wire I/O command for addressing the device. An additional function command word is then passed through the 1-wire interface to access the various DS1205S functions. The 3-wire interface (data (DQ), $\overline{\text{reset}}$ ($\overline{\text{RST}}$), and clock (CLK)) requires only the function command word. The four 1-wire I/O commands that deal with the unique lasered ROM are available only through the 1-wire interface. All other functions are available through either interface.

## FUNCTIONS

A command word written written to the DS1205S MultiKey specifies the operation to be performed and the partition to be operated on. There are two classes of functions available. One class includes operations on the read/write secure partitions. The other class includes operations on the read/write scratchpad (Figure 1).

## COMMAND OPERATIONS Figure 1




The 24 bit function command word is organized into three fields of eight bits each. These one byte fields include the function to be performed, the memory partition to be accessed and the starting byte address for the data transfer operation. The starting byte address and the partition codes are required to be given in both real and complement form. If these values do not match, access to the part will be denied (Figure 2).

The function command word is presented to the DS1205S LSB first. The first byte contains the 8-bit function code that defines which of the six valid function codes is to be executed. Each function code is valid for only certain partition and starting address combinations. Figure 3 illustrates the valid partition code, starting address and function code combinations. The second byte consists of the 2-bit partition code, identifying which partition is being accessed, and the 6-bit starting byte address, which specifies where to start the access of the given partition. The third byte consists of the complement of the 2-bit partition code and the complement of the 6-bit starting byte address.

**COMMAND WORD STRUCTURE** Figure 2

| MSB | | LSB |
|---|---|---|
| $(KK)_C(AAAAAA)_C$ | (KK)(AAAAAA) | FFFFFFFF |

(KK) = Two-bit number specifying which partition is to be accessed. 00 specifies subkey 0. 01 specifies subkey 1. 10 specifies subkey 2. 11 specifies the scratchpad.

$(KK)_C$ = Complement of (KK) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

(AAAAAA) = Address field containing address bits that define the starting byte address of the partition to be accessed.

$(AAAAAA)_C$ = Complement of (AAAAAA) on a bit-by-bit basis. If the numbers are not complements the command word is invalid and no action will be taken.

FFFFFFFF = Function code field. Specifies the action to be taken.

**LOCATIONS, AND FUNCTION CODES FOR EACH COMMAND WORD** Figure 3

| COMMAND | VALID PARTITION CODE KK | VALID BYTE ADDRESS AAAAAA | VALID FUNCTION CODE FFFF FFFF |
|---|---|---|---|
| Set Scratchpad | 11 | 0 - 63 | 1001 0110 |
| Get Scratchpad | 11 | 0 - 63 | 0110 1001 |
| Set Secure Data | 00, 01, 10 | 16 - 63 | 1001 1001 |
| Get Secure Data | 00, 01, 10 | 16 - 63 | 0110 0110 |
| Set Security Match | 00, 01, 10 | 000000 | 0101 1010 |
| Move Block | 00, 01, 10 | 000000 | 0011 1100 |

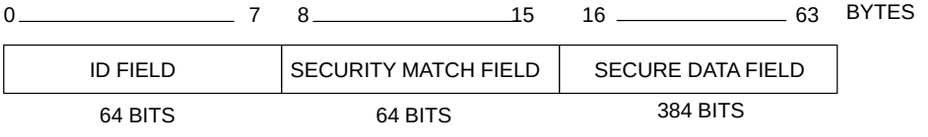
## SECURE PARTITION COMMANDS

Each of the three secure partitions within the DS1205S MultiKey is comprised of a 64-bit I.D. field, a 64-bit security match code and a 384-bit secure data field (Figure 4). The three commands that operate on the secure partitions are:

1) Set Security Match
2) Set Secure Data
3) Get Secure Data

As a guard against attackers, the security match code can never be read. Similarly, tampering through reprogramming will immediately clear the entire secure partition.

**SECURE PARTITION ORGANIZATION** Figure 4



## SET SECURITY MATCH

The Set Security Match command is used to enter data into the I.D. and security match fields of the selected secure partition. The DS1205S will respond to the command by outputting the 64-bit I.D. field of the selected secure partition. The next 64 clock cycles are used to echo the I.D. field back to the DS1205S. Upon receipt of the correct I.D., the DS1205S MultiKey will erase the contents of the selected secure partition. The part is then ready to receive the the new 64-bit I.D. and the 64-bit security match code. The flow sequence is shown in Figure 5.

## SET SECURE DATA

The Set Secure Data command is used to write data into the selected secure partition. After the command is received by the DS1205S, the 64-bit I.D. field of the selected secure partition is output. The next 64 bits of input comprise a password that must match the security match code of the selected secure partition. If the password and the security match are identical, data is written to the secure data field starting at the address specified in the command word. If the password and the security match code are not identical, the DS1205S will terminate the transaction immediately. The flow sequence is shown in Figure 6.

## GET SECURE DATA

The Get Secure Data command is used to retrieve data from the selected secure partition. After the command word is received by the DS1205S, the 64-bit I.D. field of the selected secure partition is returned. The next 64 bits are the password being written to the DS1205S. If the presented password and the security match code of the selected secure partition are identical, the DS1205S will output the contents of the secure data field starting from the byte specified in the command word. If the presented password is not identical to the security match code, the DS1205S MultiKey will use the password as a “seed” for its internal random number generator. This results in a repeatable, seemingly valid yet false response to the invalid password. The flow sequence is shown in Figure 7.

## SCRATCHPAD READ/WRITE COMMANDS

The 512-bit read/write scratchpad of the DS1205S MultiKey is not protected by a security match code. This partition is byte addressable. The scratchpad can be used to store unsecured data or it can act as a staging area to build and verify data structures to be transferred to a secure partition. The three commands that operate on the read/write scratchpad are:

1. Set Scratchpad Data
2. Get Scratchpad Data
3. Move Block

## SET SCRATCHPAD DATA

The Set Scratchpad Data command is used to enter data into the DS1205S MultiKey scratchpad. The command word must specify the starting byte address for the data transfer. Valid byte addresses are 0 through 63. The DS1205S MultiKey will write data to the scratchpad until byte 63 has been written or until the $\overline{RST}$ line goes to a logic low level. The flow sequence is shown in Figure 8.

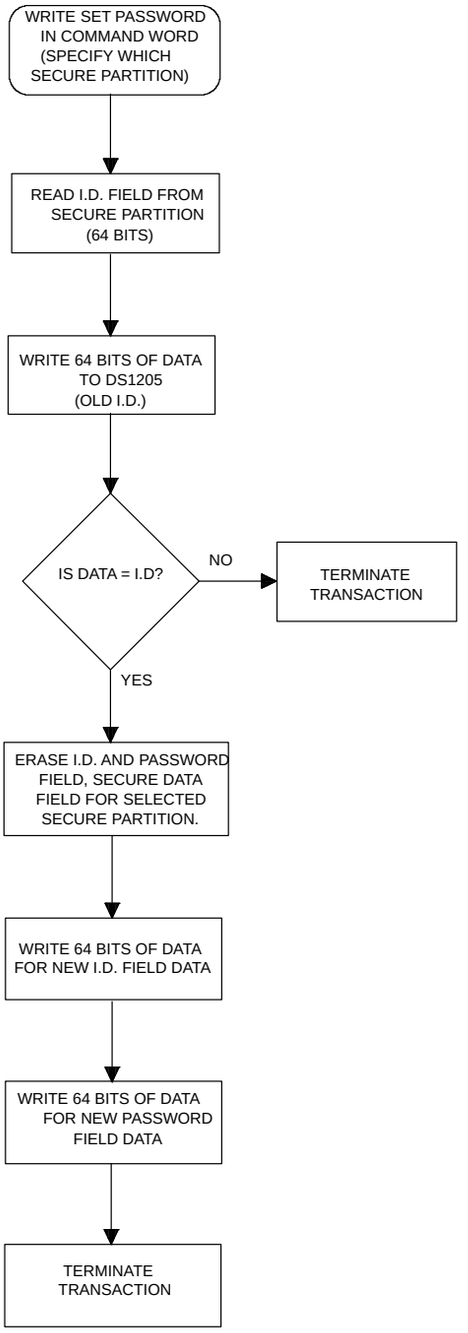
## GET SCRATCHPAD DATA

The Get Scratchpad data command is used to retrieve data from the 512-bit scratchpad. The command word must specify the starting byte address for the data retrieval. Valid byte addresses are 0 through 63. The DS1205S MultiKey will retrieve data from the scratchpad until byte 63 has been read or the $\overline{RST}$ line goes to a logic low level. The flow sequence is shown in Figure 9.

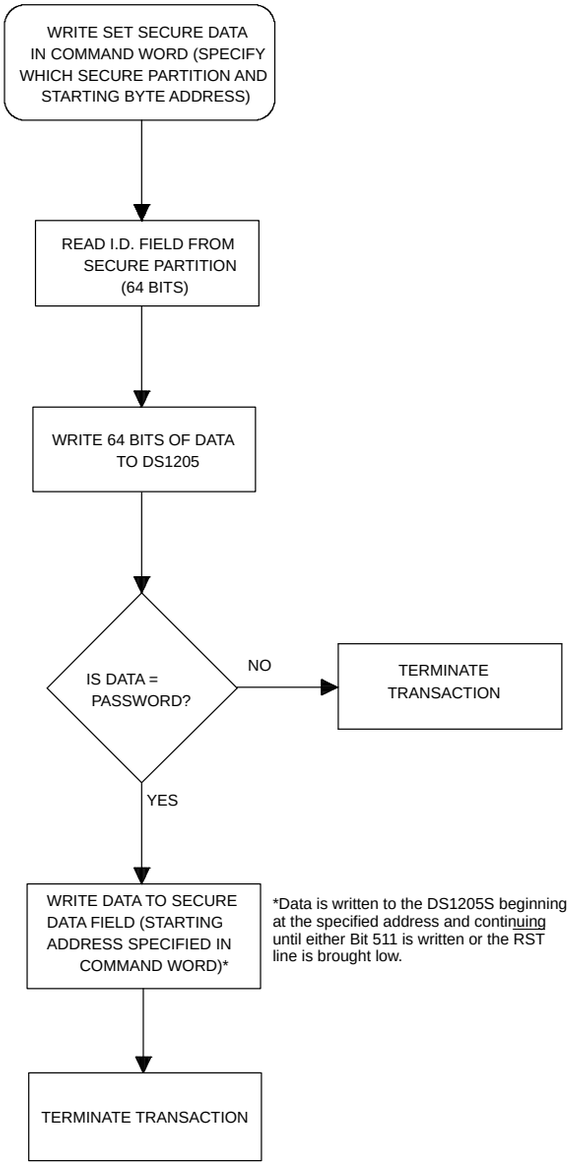
## MOVE BLOCK

The Move Block command is used to transfer data, which has been previously entered into the scratchpad and verified, to one of the three secure subkeys. Data can be transferred as one large block of 512 bits or it can be transferred in blocks of 64 bits each (Figure 10). There are nine valid block selectors which are used to specify which block or blocks are to be transferred (Figure 11). As a further precaution against accidental erasure of a secure subkey, the 64-bit password of the destination subkey must be entered and match the destination subkey. If the passwords fail to match, the operation is terminated. The flow sequence is shown in Figure 12.

**SET SECURITY MATCH** Figure 5

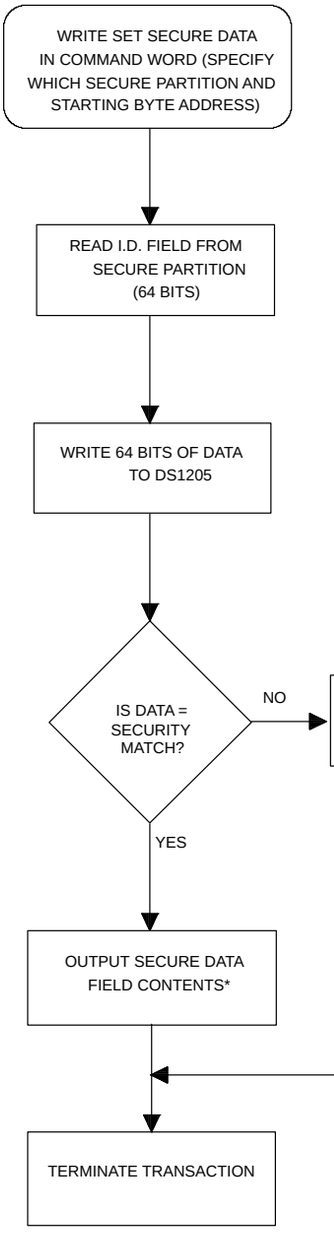



**SET SECURE DATA** Figure 6



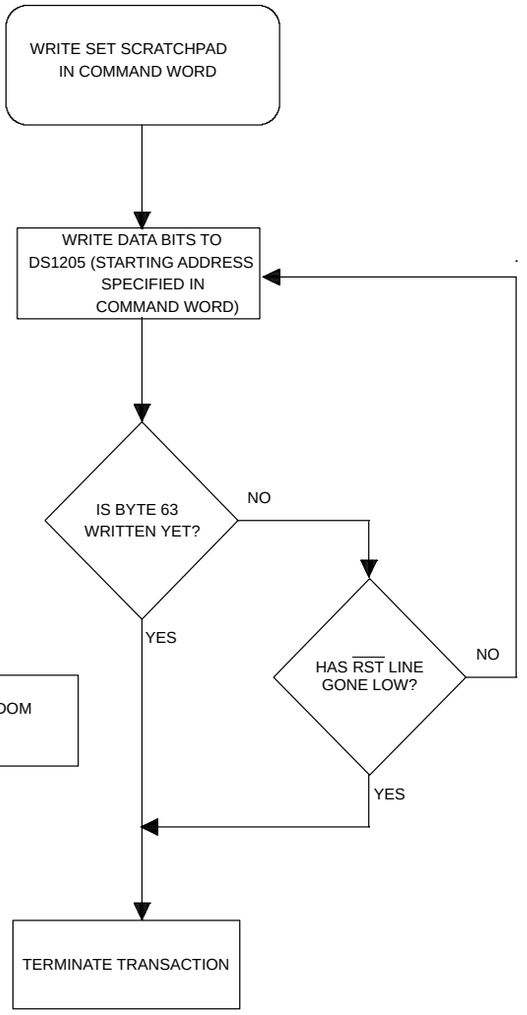

*Data is written to the DS1205S beginning at the specified address and continuing until either Bit 511 is written or the RST line is brought low.

**GET SECURE DATA** Figure 7

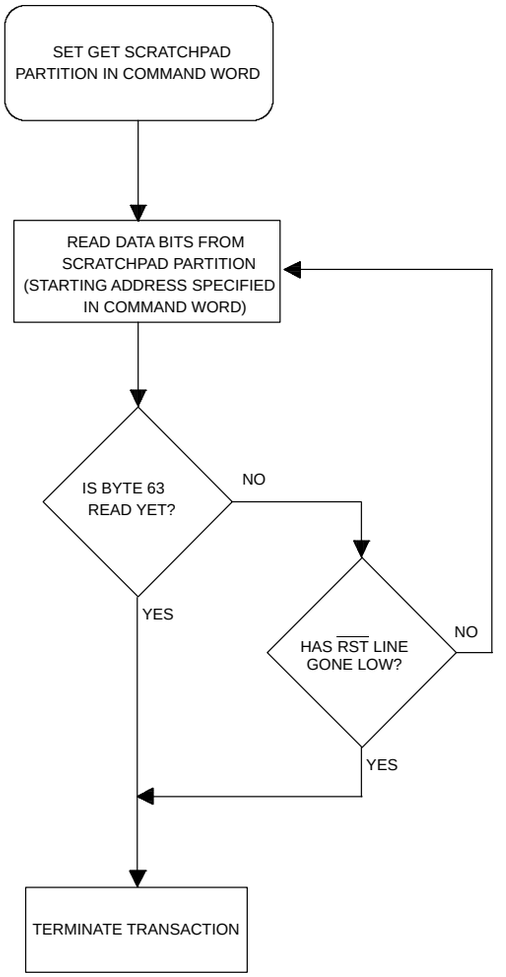



*Data is read from the DS1205S beginning at the specified address and continuing until either Bit 511 is read or the $\overline{RST}$ line is brought low.

**SET SCRATCHPAD** Figure 8



**SET SCRATCHPAD** Figure 9



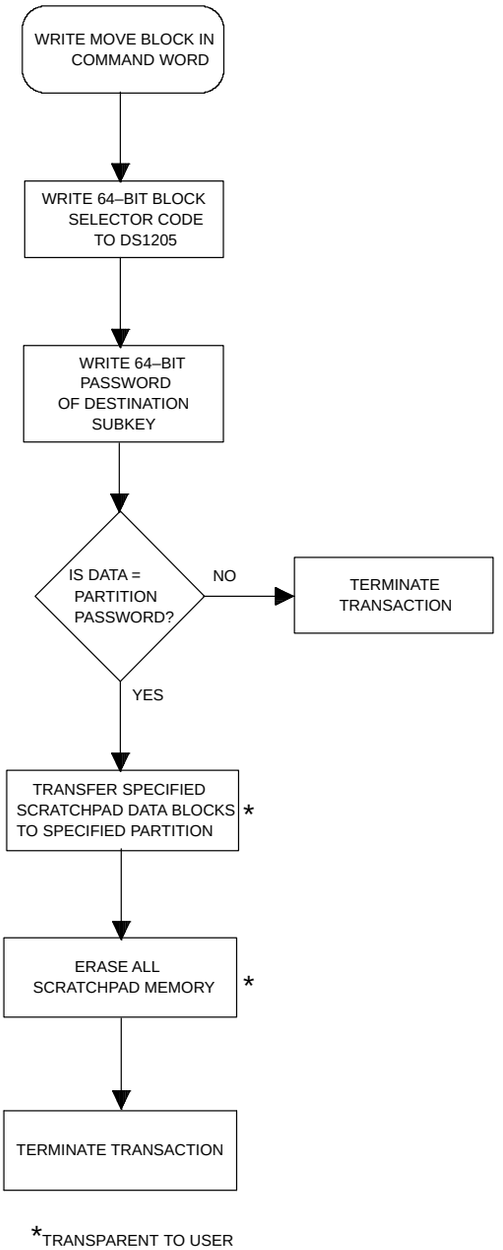

**BLOCK SELECTIONS** Figure 10

| BLOCK NUMBER | BYTE ADDRESS SCRATCHPAD | IN: SUBKEY |
|---|---|---|
| 0 | 0-7 | 0-7(ID) |
| 1 | 8-15 | 8-15 (PASSWORD) |
| 2 | 16-23 | 16-23 (SECURED) |
| 3 | 24-31 | 24-31 (SECURED) |
| 4 | 32-39 | 32-39 (SECURED) |
| 5 | 40-47 | 40-47 (SECURED) |
| 6 | 48-55 | 48-55 (SECURED) |
| 7 | 56-63 | 56-63 (SECURED) |

**BLOCK SELECTOR CODES FOR MOVE BLOCK COMMAND** Figure 11

| BLOCK # | SELECTOR CODE |
|---|---|
| 0 | 4C69 6E64 9DB3 9A9A (H) |
| 1 | 4C69 919B 624C 9A9A (H) |
| 2 | 4C96 6E9B 62B3 659A (H) |
| 3 | 4366 616B 6D43 6A6A (H) |
| 4 | BC99 9E94 92BC 9595 (H) |
| 5 | B369 9164 9D4C 9A65 (H) |
| 6 | B396 6E64 9DB3 6565 (H) |
| 7 | B396 919B 624C 6565 (H) |
| ALL BLOCKS | 7F5A 5D57 517F 5656 (H) |

**MOVE BLOCK** Figure 12

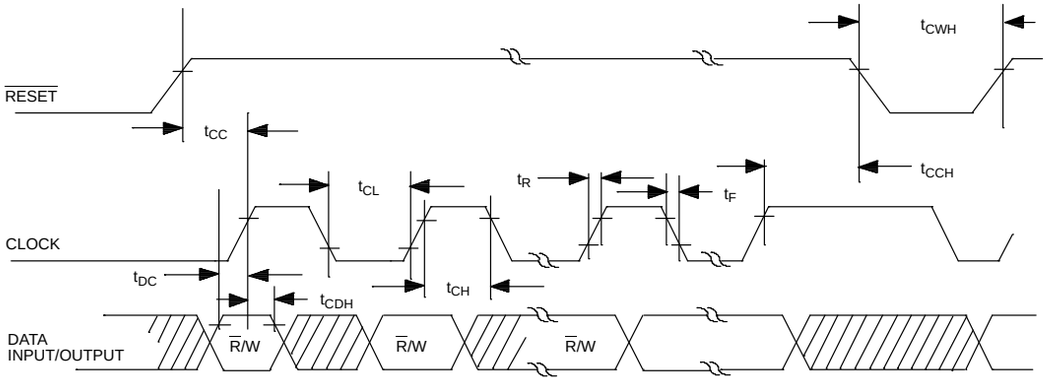



## 3-WIRE BUS

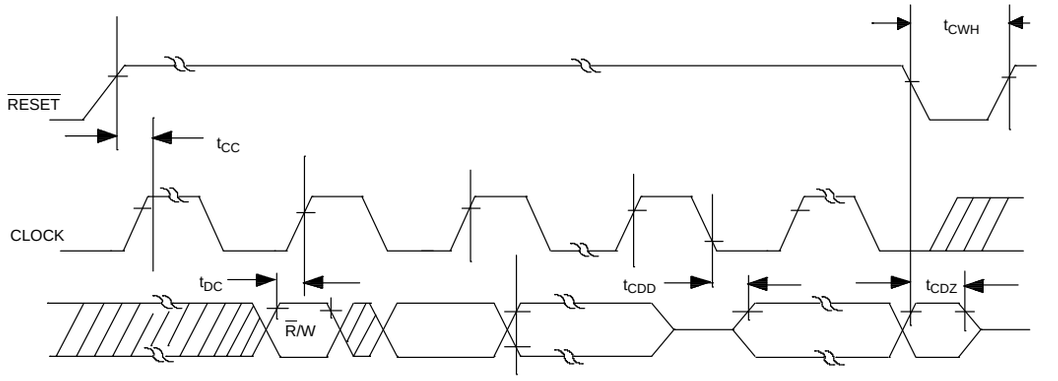
The 3-wire bus is comprised of three signals. These are the $\overline{RST}$ ($\overline{reset}$) signal, the CLK (clock) signal, and the DQ (data) signal. All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ signal provides a method of terminating a data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfers terminate if $\overline{RST}$ is low and the DQ pin goes to a high impedance state. When data transfers to the DS1205S are terminated by the $\overline{RST}$ signal going low, the transition of the $\overline{RST}$ going low must occur during a high level of the CLK signal. Failure to ensure that the CLK signal is high will result in the corruption of the last bit transferred. Data transfers are illustrated in Figure 13 and Figure 14 for normal modes of operation.

**WRITE DATA TIMING DIAGRAM** Figure 13




**READ DATA TIMING DIAGRAM** Figure 14




## 1-WIRE PROTOCOL

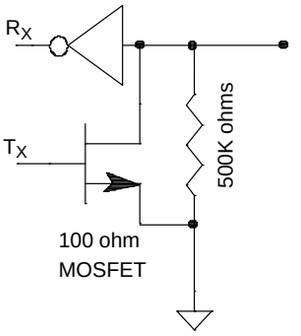
The 1-wire protocol defines the system as a single bus master system with single or multiple slaves. In all instances, the DS1205S is a slave. The bus master is typically a microcontroller. The discussion of this protocol is broken down into two topics: hardware configuration and transaction sequence.

### Hardware Configuration

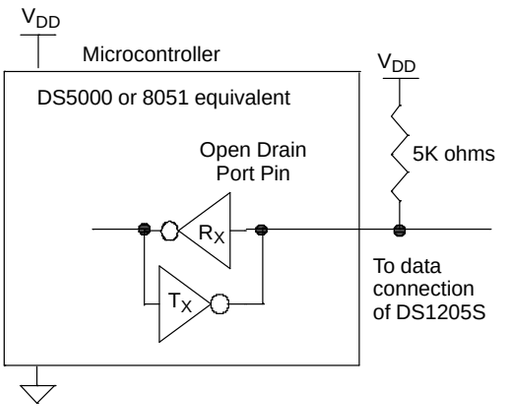
The 1-wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-wire bus must have open drain connections. The DS1205S is an open drain part with an internal circuit equivalent to that shown in Figure 15. Ideally, the bus master should also be open drain; but if this is not feasible, two standard TTL pins can be tied together, one as an output and one as an input. When using a bus master with an open drain port, the bus requires a pull-up resistor at the master end of the bus. The system bus master circuit should be equivalent to the one shown in Figure 16. The value of the pull-up resistor should be greater than 5K ohms. If the pull-up value is less, the bus may not be pulled to an adequately low state (< 0.6 volts).

The idle state for the 1-wire bus is high. If, for any reason, a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left for more than 560 µS, all components on the bus will be reset.

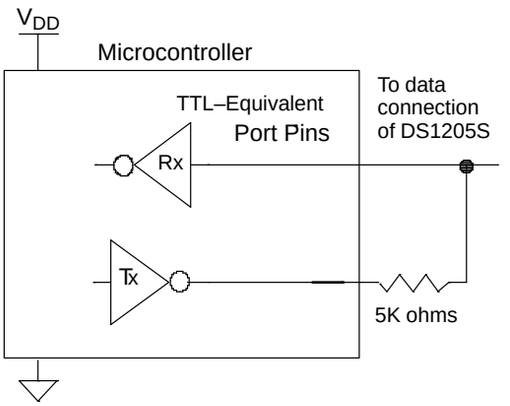
**EQUIVALENT CIRCUIT** Figure 15




**BUS MASTER OPEN DRAIN CIRCUIT**
Figure 16A




**BUS MASTER STANDARD TTL CIRCUIT**
Figure 16B




## Transaction Sequence

The protocol for accessing the DS1205S is as follows:

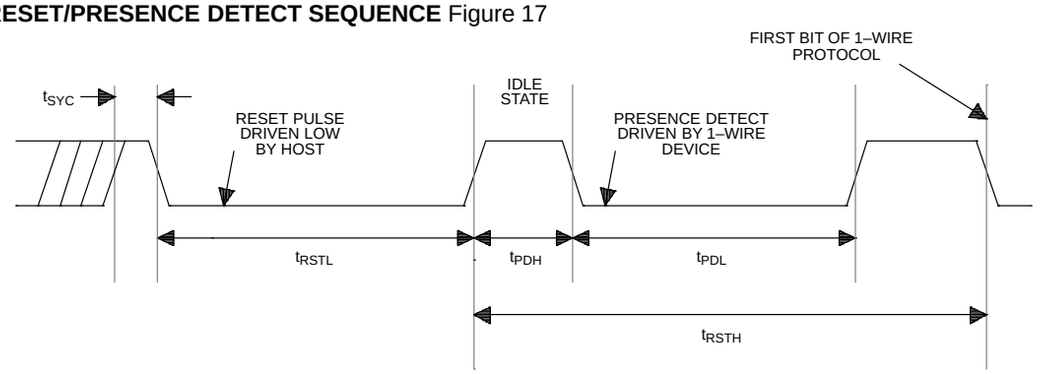
Reset
Presence Detect
1-wire Command Word
Device Command Word
Transaction/Data
CRC

Reset/Presence Detect - All transactions on the 1-wire bus begin with the reset sequence. The reset sequence is started by holding the data line low for 560 µS. The DS1205S is designed to be held in the reset state whenever it is not connected to the bus. When it is connected to the bus, the data line is pulled high, the part is taken out of reset, and the part is ready to issue the presence detect.

After detecting a high state on the data line, the DS1205S waits 15 µS minimum and issues its presence detect. This presence detect is a low-going pulse that last 70 µS. This response to the reset pulse lets the bus master know that the DS1205S is on the bus and is ready to operate. The presence detect helps the bus master to discriminate the communication signals from noise as the DS1205S is taken on and off the bus. Refer to the timing diagram in Figure 17.

After the DS1205S has responded to the reset pulse with a presence detect, the bus master drives the bus to the idle state for a minimum of 1 µS. The 1 µS interval is like a frame sync. After each bit is transmitted on the bus, there is a frame strobe to sync up for the next transmission. Refer to Figure 17.

**RESET/PRESENCE DETECT SEQUENCE** Figure 17




1-Wire I/O Commands - Once the bus master has detected a presence, it can issue one of the four different 1-wire I/O commands. These commands deal with the laser-etched ROM code which has the following format.

| Type ID | Unique Serial Number | CRC |
|---|---|---|
| 8 bits | 48 bits | 8 bits |

All 1-wire commands are eight bits long. A list of these commands are as follows:

CCh Pass Thru Mode

This command saves time by allowing direct access to the DS1205S without identifying it by ROM ID number. This command can only be used when there is a single slave on the bus. If more than one device is present, there will be bus contention.

33h Read ROM Data

This command allows the bus master to read the DS1205S's unique 48-bit ID number and CRC. This command can only be used if there is a single DS1205S on the bus. If more than one is present, there will be bus contention.

55H Match ROM Data

This mode allows the bus master to single out a specific DS1205S on a multidrop bus. The bus master selects the specific slave by the ROM ID number for the transaction. This command can be used with a single or multiple device on the bus.

F0h Search ROM Data

When a system is initially brought up, the bus master might not know the number or types of devices on the bus. By invoking the Search ROM Data command the bus master can, by process of elimination, find the ID numbers of all the devices on the bus. Once this is known, the bus master can then go back and read the device type that corresponds to each ID number.

The ROM search process is the repetition of a simple 3-step routine: read a bit, read the complement of the same bit, then write the desired value of that bit. The bus master performs this simple 3-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. The bus is reset and the process is repeated again, selecting a different set of bit values. The bus master controls the search according to what values are written as select bits.

The following example of the ROM search process assumes four different devices are connected to the same 1-wire bus. The ROM data of the four devices is as shown:

ROM1 00110101...
ROM2 10101010...
ROM3 11110101...
ROM4 00010001...

The search process is as follows:

1. The bus master begins by resetting all devices present on the 1-wire bus. After this, the bus master will attempt to read the family code, serial number, and CRC value for the part.
2. The bus master will then issue the Search ROM Data command on the 1-wire bus.
3. The bus master performs two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the first bit of the devices on the bus.

4. The bus master writes a 0. This deselects ROM2 and ROM3 for the remainder of this search pass, leaving only ROM1 and ROM4 connected to the 1-wire bus.
5. The bus master performs two more reads and receives a 0 bit followed by a 1 bit. This indicates that all devices still coupled to the bus have 0's as their second ROM data bit.
6. The bus master then writes a 0 to keep both ROM1 and ROM4 coupled.
7. The bus master executes two reads and receives two 0 bits. This indicates that both 1 bits and 0 bits exist as the third bit of the ROM data of the attached devices.
8. The bus master writes a 0 bit. This deselects ROM1 leaving ROM4 as the only device still connected.
9. The bus master reads the remainder of the ROM bits for ROM4 and continues to access the part if desired. This completes the first pass and uniquely identifies one part on the 1-wire bus.

At this point, the bus master repeats the process described above to determine the address of the remaining devices on the 1-wire bus by repeating steps 1 though 7.

Note the following:

The bus master learns the unique ID number (ROM data pattern) of one 1-wire device on each ROM Search operation. The time required to derive the part's unique ID is:

960 µS + 3(8+64) X 0.06mS = 13.92mS

The bus master is therefore capable of identifying 60 different 1-wire devices per second.

Additionally, the data obtained from the two reads of each set of three have the following interpretations:

00 - There are still devices attached which have conflicting bits in this position.

01 - All devices still coupled have a zero bit in this bit position.

10 - All devices still coupled have a one bit in this bit position.

11 - There are no devices attached to the 1-wire bus.

Transmitting/Receiving Data - All communications on the 1-wire bus begin with the reset and presence detect sequence. This sequence ensures the DS1205S is in the listening mode. The bus master must then transmit the 1-wire command to the DS1205S. To transmit the first bit of the 1-wire I/O command, the master pulls the bus low for 1 µS. This low-going edge informs the DS1205S that the first bit is being sent. After 1 µS, the master does one of two things:

1. holds the line low for an additional 70 µS to output a 0 (write a 0) or,
2. lets the bus go high for an additional 70 µS (write a 1).

The state of the bus during this 70 µS time phase determines the value of the bit. The DS1205S will sense any rising edge during this 70 µS time phase as a one. After the 70 µS has lapsed, the bus master must then drive the bus high for 1 µS. This is the frame sync mentioned earlier. This process is repeated until all the eight bits are transmitted. Refer to the timing diagram in Figure 18.

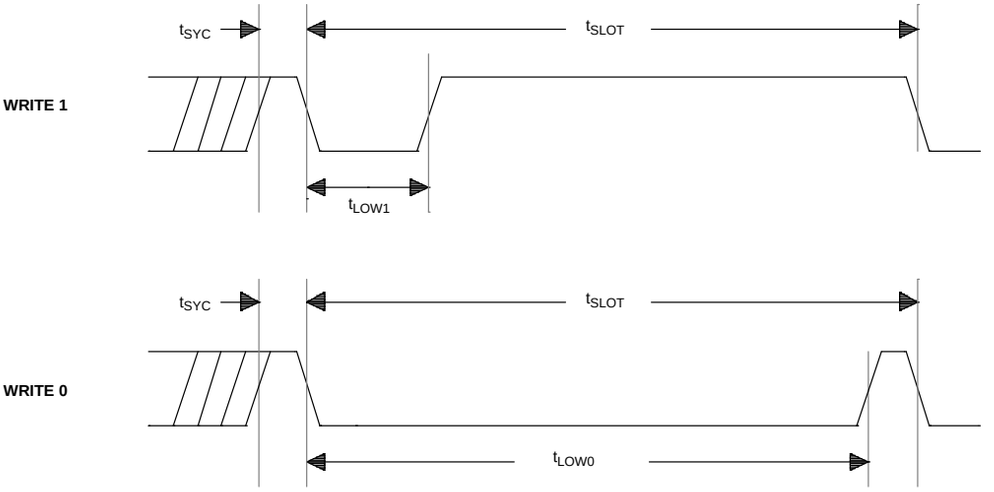
The bus master now reads the family code identifier, followed by the data and a CRC. The read cycle is similar to the write cycle. It is started with the bus master pulling the bus low for 1 µS. This informs the DS1205S that it should have data on the bus no later than the 1 µS from the falling edge. After the 1 µS, the bus master lets go of the bus and the DS1205S drives the bus. The slave must hold the data on the bus for an additional 14 µS minimum (59 µS maximum). During the DS1205S holding time, the bus master reads the state of the bus. Ideally, the bus master should read data from the bus 15 µs after the falling edge. The entire cycle time for one bit lasts a minimum of 70 µS (140 µS maximum) from the falling edge. At the end of the cycle, the bus master drives the bus high for 1 µS. Again, this is like a frame sync for the next bit. This read sequence is repeated until all the data has been read. See the timing diagram in Figure 19 for details. If for any reason the transaction needs to be terminated before all the data is read, the DS1205S must be reset.

CRC Generation - To validate the transmitted data from the DS1205S, the bus master must generate a CRC value for the data as it is received. This generated value is compared to the value stored in the last eight bits of the DS1205S. The bus master computes the CRC over the 8-bit family code and all 48 ID number data bits, but NOT over the stored CRC value itself. The CRC is calculated using the following polynomial.

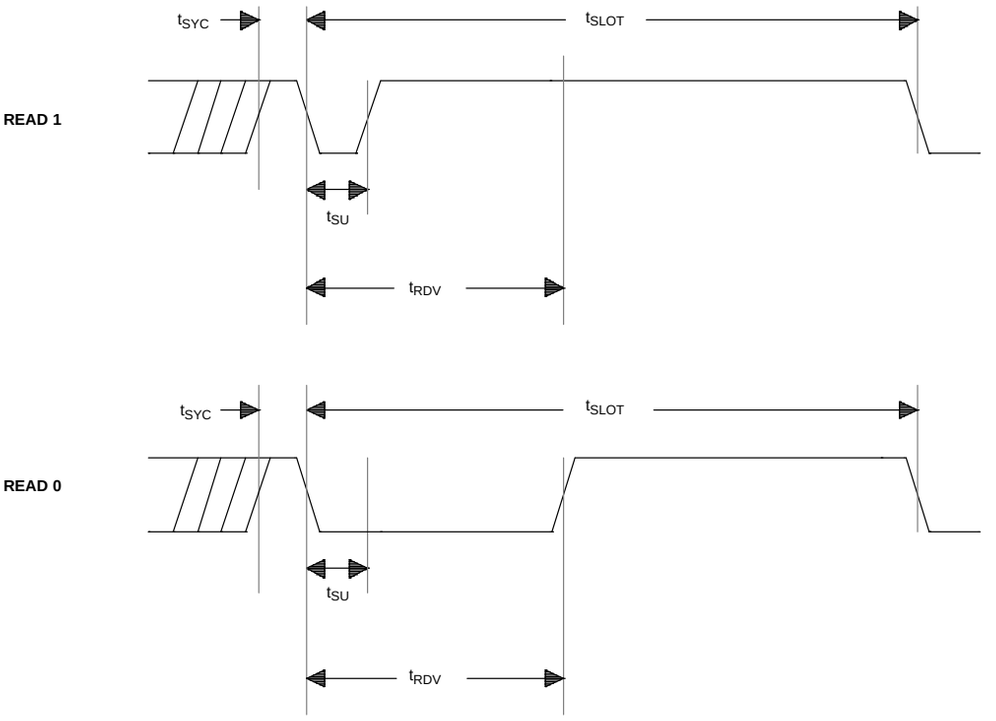
$$CRC = px^3 + px^2 + 1$$

If the two CRC values match, the transmission is error-free.

**1-WIRE WRITE TIMING** Figure 18




**1-WIRE READ TIMING** Figure 19



## PASS-THRU MODE

A host connected to the 1-wire bus may send function commands directly to the DS1205S without preceding them with 1-wire I/O commands by using the pass-thru command (CCh). This command bypasses the serial number and consequently it can only be used when there is one DS1205S on the 1-wire bus.

## 1-WIRE/3-WIRE ARBITRATION

The DS1205S can utilize both the 1-wire and the 3-wire busses simultaneously. Neither input bus has priority over the other. Instead, if both inputs are being used, the signal arriving first will take precedence. More simply, if the 1-wire interface becomes active before the 3-wire interface, all communications will take place on the 1-wire bus. The 3-wire bus will be ignored in this case. The same condition occurs for the 1-wire interface if the 3-wire interface becomes active first.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on any Pin Relative to Ground | -0.5V to +7.0V |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -55°C to +125°C |
| Soldering Temperature | 260°C for 10 seconds |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 | $V_{IH}$ | 2.0 | | | V | 1 |
| Logic 0 | $V_{IL}$ | -0.3 | | +0.8 | V | 1 |
| Supply | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |

## DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}$ = 5V $\pm$ 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{IL}$ | | | +500 | µA | |
| Output Leakage | $I_{OL}$ | | | +500 | µA | |
| Output Current @ 2.4V | $I_{OH}$ | -1 | | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | | | +1 | mA | |
| $\overline{RST}$ Input Resistance | $Z_{RST}$ | 100 | | 1000 | Kohm | |
| D/Q Input Resistance | $Z_{DQ}$ | 100 | | 1000 | Kohm | |
| CLK Input Resistance | $Z_{CLK}$ | 100 | | 1000 | Kohm | |
| Active Current | $I_{CC1}$ | | 3 | 6 | mA | 5,6 |
| Standby Current | $I_{CC2}$ | | | 100 | µA | 5,6 |
| Batt. Operate Consumption | $I_{BAT}$ | | 200 | 500 | nC | 7,8 |
| Batt. Operate Standby Current | $I_{BATS}$ | | 30 | 200 | nA | 7 |
| Batt. Voltage | $V_{BAT}$ | 2.0 | | 3.6 | V | 1 |
| Output Supply Current | $I_{CCO}$ | | | 10 | mA | 11 |

## CAPACITANCE

($t_A$= 25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 7 | pF | |

## AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, $V_{CC}$ = 5V ± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Data to CLK Setup | $t_{DC}$ | 35 | | | ns | 2 |
| CLK to Data Hold | $t_{CDH}$ | 40 | | | ns | 2 |
| CLK to Data Delay | $t_{CDD}$ | | | 200 | ns | 2,3,4 |
| CLK Low Time | $t_{CL}$ | 250 | | | ns | 2 |
| CLK High Time | $t_{CH}$ | 250 | | | ns | 2 |
| CLK Frequency | $t_{CLK}$ | DC | | 2.0 | MHz | 2 |
| CLK Rise & Fall | $t_R$,$t_F$ | | | 500 | ns | 2 |
| $\overline{RST}$ to CLK Setup | $t_{CC}$ | 1 | | | µs | 2 |
| CLK to $\overline{RST}$ Hold | $t_{CCH}$ | 40 | | | ns | 2 |
| $\overline{RST}$ Inactive Time | $t_{CWH}$ | 250 | | | ns | 2 |
| RST to I/O High Z | $t_{CDZ}$ | | | 50 | ns | 2 |

## AC ELECTRICAL CHARACTERISTICS: 1-WIRE INTERFACE

(0°C to 70°C, $V_{CC}$ = 5V± 10%)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Time Slot Period | $t_{SLOT}$ | 70 | | 140 | µs | |
| Write 1 Low Time | $t_{LOW1}$ | 1 | | 15 | µs | |
| Write 0 Low Time | $t_{LOW0}$ | 70 | | 140 | µs | |
| Read Data Valid | $t_{RDV}$ | 15 | | | µs | |
| Read Data Setup | $t_{SU}$ | 1 | | | µs | 10 |
| Frame Sync | $t_{SYC}$ | 1 | | | µs | |
| Reset Low Time | $t_{RSTL}$ | 560 | | | µs | |
| Reset High Time | $t_{RSTH}$ | 560 | | | µs | 9 |
| Presence Detect High | $t_{PDH}$ | 15 | | 70 | µs | |
| Presence Detect Low | $t_{PDL}$ | 70 | | 280 | µs | |

**NOTES:**

1. All voltages are referenced to ground.
2. $V_{IH}$ = 2.0V or $V_{IL}$ = 0.8V with 10 ns maximum rise and fall time.
3. $V_{OH}$ = 2.4V and $V_{OL}$ = 0.4V.
4. Load capacitance = 50 pF.
5. Measured with outputs open.
6. (Normal battery backup operation) $V_{CC1}$ = 5.0 Volts $\pm$ 10%; $V_{BAT}$ = 3.0 Volts.
7. (Battery operate mode) $V_{CCO}$ = 3.0 Volts.
8. Per transaction (512 bits + protocol).
9. An additional reset or communication sequence cannot begin until the reset high time has expired.
10. Read data setup time refers to the time the host must pull the 1-wire pin low to read a bit. Data is guaranteed to be valid within 1 µS of this falling edge and will remain valid for 14 µS minimum (15 µS total falling edge on 1-wire).
11. $V_{CCO} = V_{CCI}$ - 0.3V