CYWUSB6934
CYWUSB6932

WirelessUSB™ LS 2.4 GHz DSSS Radio SoC

Features

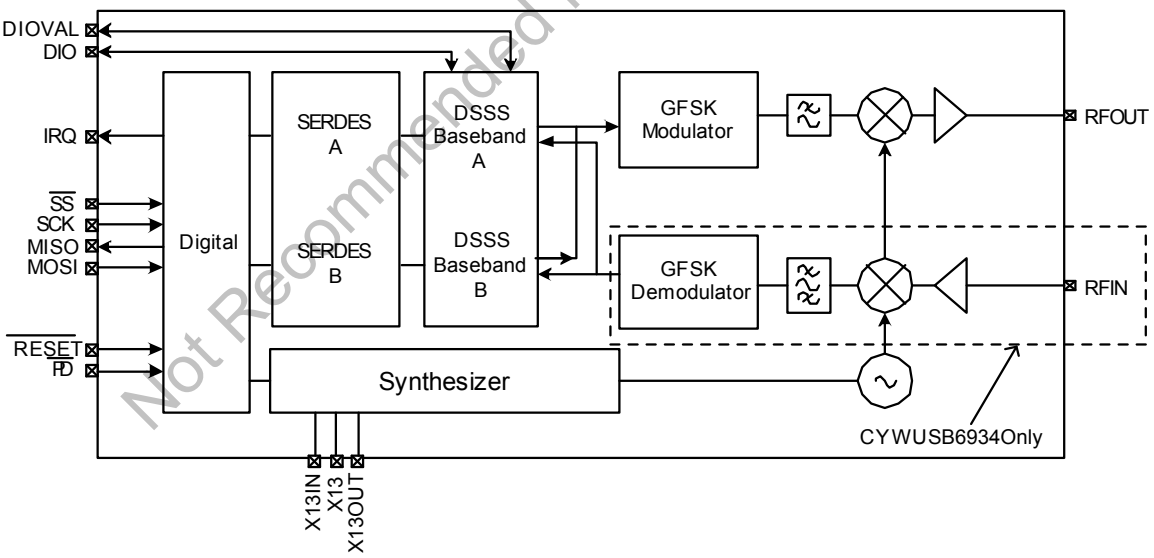
- 2.4-GHz radio transceiver
- Operates in the unlicensed Industrial, Scientific, and Medical (ISM) band (2.4 GHz to 2.483 GHz)
- Receive sensitivity: –90 dBm
- Up to 0 dBm output power
- Range of up to 10 meters or more
- Data throughput of up to 62.5 kbits/sec
- Highly integrated low cost, minimal number of external components required
- Dual direct sequence spread spectrum (DSSS reconfigurable baseband correlators
- SPI microcontroller interface (up to 2-MHz data rate)
- 13-MHz ± 50-ppm input clock operation
- Low standby current < 1 µA
- Integrated 30-bit Manufacturing ID
- Operating voltage from 2.7 V to 3.6 V
- Operating temperature from 0° to 70°C
- Offered in a small footprint 48 quad flat pack no leads (QFN)

Functional Description

The CYWUSB6932[1]/CYWUSB6934 Integrated Circuits (ICs) are highly integrated 2.4-GHz DSSS radio system-on-chip (SoC) ICs. From the serial peripheral interface (SPI) to the antenna, these ICs are single-chip 2.4-GHz DSSS Gaussian Frequency Shift Keying (GFSK) baseband modems that connect directly to a microcontroller via simple serial interface.

The CYWUSB6932 transmit-only IC and the CYWUSB6934 transceiver IC are available in a small footprint 48-pin QFN package.

Logic Block Diagram – CYWUSB6932/CYWUSB6934



Note
1. CYWUSB6932 is now obsolete and is no longer supported.

Contents

Applications

- PC human interface devices (HIDs)
  - Mice
  - Keyboards
  - Joysticks
- Peripheral gaming devices
  - Game controllers
  - Console keyboards
- General
  - Presenter tools
  - Remote controls
  - Consumer electronics
  - Barcode scanners
  - POS peripherals
  - Toys

Applications Support

The CYWUSB6932/CYWUSB6934 ICs are supported by the CY3632 WirelessUSB Development Kit. The development kit provides all of the materials and documents needed to cut the cord on wired applications such as:

1. Two radio modules that connect directly to two prototyping platform boards
2. Comprehensive WirelessUSB protocol code examples
3. A WirelessUSB Listener tool
4. All of the associated schematics, gerber files, and bill of materials.

The CY4632 WirelessUSB LS keyboard mouse reference design provides a production-worthy example of a wireless mouse and keyboard system.

The CY3633 WirelessUSB LS gaming development kit provides support for designing a wireless gamepad for the major gaming consoles and is offered as an accessory to the CY3632 WirelessUSB development kit.

Functional Overview

The CYWUSB6932/CYWUSB6934 ICs provide a complete WirelessUSB LS SPI to antenna radio modem. The SoC is designed to implement wireless devices operating in the worldwide 2.4-GHz ISM frequency band (2.400 GHz to 2.4835 GHz). It is intended for systems compliant with world-wide regulations covered by ETSI EN 301 489-1 V1.4.1, ETSI EN 300 328-1 V1.3.1 (European countries); FCC CFR 47 Part 15 (USA and Industry Canada) and ARIB STD-T66 (Japan).

The CYWUSB6934 IC contains a 2.4-GHz radio transceiver, a GFSK modem and a dual DSSS reconfigurable baseband. The CYWUSB6932 IC contains a 2.4-GHz radio transmit-only, a GFSK modem and a DSSS baseband. The radio and baseband are both code- and frequency-agile. Forty-nine spreading codes selected for optimal performance (Gold codes) are supported across 78 1-MHz channels yielding a theoretical spectral capacity of 3822 channels. Both ICs support a range of up to 10 meters or more.

2.4-GHz Radio

The receiver and transmitter are a single-conversion low-Intermediate Frequency (low-IF) architecture with fully integrated IF channel matched filters to achieve high performance in the presence of interference. An integrated Power Amplifier (PA) provides an output power control range of 30 dB in seven steps.

Table 1. Internal PA Output Power Step Table

PA Setting	Typical Output Power (dBm)
7	0
6	–2.4
5	–5.6
4	–9.7
3	–16.4
2	–20.8
1	–24.8
0	–29.0

Both the receiver and transmitter integrated Voltage Controlled Oscillator (VCO) and synthesizer have the agility to cover the complete 2.4-GHz GFSK radio transmitter ISM band. The synthesizer provides the frequency-hopping local oscillator for the transmitter and receiver. The VCO loop filter is also integrated on-chip.

GFSK Modem

The transmitter uses a DSP-based vector modulator to convert the 1-MHz chips to an accurate GFSK carrier.

The receiver uses a fully integrated Frequency Modulator (FM) detector with automatic data slicer to demodulate the GFSK signal.

Dual DSSS Baseband

Data is converted to DSSS chips by a digital spreader. De-spreading is performed by an oversampled correlator. The DSSS baseband cancels spurious noise and assembles properly correlated data bytes.

The DSSS baseband has three operating modes: 64 chips/bit Single Channel, 32 chips/bit Single Channel, and 32 chips/bit Single Channel Dual Data Rate (DDR).

64 Chips/Bit Single Channel

The baseband supports a single data stream operating at 15.625 kbits/sec. The advantage of selecting this mode is its ability to tolerate a noisy environment. This is because the 15.625 kbits/sec data stream utilizes the longest PN Code resulting in the highest probability for recovering packets over the air. This mode can also be selected for systems requiring data transmissions over longer ranges.

32 Chips/Bit Single Channel

The baseband supports a single data stream operating at 31.25 kbits/sec.

32 Chips/Bit Single Channel Dual Data Rate (DDR)

The baseband spreads bits in pairs and supports a single data stream operating at 62.5 kbits/sec.

Serializer/Deserializer (SERDES)

The CYWUSB6934 IC has a data Serializer/Deserializer (SERDES), which provides byte-level framing of transmit and receive data. Bytes for transmission are loaded into the SERDES and receive bytes are read from the SERDES via the SPI interface. The SERDES provides double buffering of transmit and receive data. While one byte is being transmitted by the radio the next byte can be written to the SERDES data register insuring there are no breaks in transmitted data.

After a receive byte has been received it is loaded into the SERDES data register and can be read at any time until the next byte is received, at which time the old contents of the SERDES data register will be overwritten. The CYWUSB6932 IC only has a data serializer.

Application Interfaces

Both ICs have a fully synchronous SPI slave interface for connectivity to the application MCU. Configuration and byte-oriented data transfer can be performed over this interface. An interrupt is provided to trigger real time events.

An optional SERDES Bypass mode (DIO) is provided for applications that require a synchronous serial bit-oriented data path. This interface is for data only.

Clocking and Power Management

A 13-MHz crystal (±50 ppm or better) is directly connected to X13IN and X13 without the need for external capacitors. Both ICs have a programmable trim capability for adjusting the on-chip load capacitance supplied to the crystal.

Below are the requirements for the crystal to be directly connected to X13IN and X13:

- Nominal frequency: 13 MHz
- Operating mode: Fundamental mode
- Resonance mode: Parallel resonant
- Frequency stability: ± 50 ppm
- Series resistance: ≤ 100 ohms
- Load capacitance: 10 pF
- Drive level: 10 uW to 100 uW

The Radio Frequency (RF) circuitry has on-chip decoupling capacitors. Both devices are powered from a 2.7 V to 3.6 V DC supply. Both devices can be shutdown to a fully static state using the PD pin.

Receive Signal Strength Indicator (RSSI)

The RSSI register (Reg 0x22) (applies only to the CYWUSB6934 IC) returns the relative signal strength of the ON-channel signal power and can be used to:

1. Determine the connection quality
2. Determine the value of the noise floor
3. Check for a quiet channel before transmitting.

The internal RSSI voltage is sampled through a 5-bit analog-to-digital converter (ADC). A state machine controls the conversion process. Under normal conditions, the RSSI state machine initiates a conversion when an ON-channel carrier is detected and remains above the noise floor for over 50 µs. The conversion produces a 5-bit value in the RSSI register (Reg 0x22, bits 4:0) along with a valid bit, RSSI register (Reg 0x22, bit 5). The state machine then remains in HALT mode and does not reset for a new conversion until the receive mode is toggled off and on. Once a connection has been established, the RSSI register can be read to determine the relative connection quality of the channel. A RSSI register value lower than 10 indicates that the received signal strength is low, a value greater than 28 indicates a strong signal level.

To check for a quiet channel before transmitting, first set up receive mode properly and read the RSSI register (Reg 0x22). If the valid bit is zero, then force the Carrier Detect register (Reg 0x2F, bit 7=1) to initiate an ADC conversion. Then, wait greater than 50 µs and read the RSSI register again. Next, clear the Carrier Detect Register (Reg 0x2F, bit 7=0) and turn the receiver OFF. Measuring the noise floor of a quiet channel is inherently a 'noisy' process so, for best results, this procedure should be repeated several times (~20) to compute an average noise floor level. A RSSI register value of 0-10 indicates a channel that is relatively quiet. A RSSI register value greater than 10 indicates the channel is probably being used. A RSSI register value greater than 28 indicates the presence of a strong signal.

Application Interfaces

SPI Interface

The CYWUSB6932/CYWUSB6934 ICs have a four-wire SPI communication interface between an application MCU and one or more slave devices. The SPI interface supports single-byte and multi-byte serial transfers. The four-wire SPI communications interface consists of Master Out-Slave In (MOSI), Master In-Slave Out (MISO), Serial Clock (SCK), and Slave Select (SS).

The SPI receives SCK from an application MCU on the SCK pin. Data from the application MCU is shifted in on the MOSI pin. Data to the application MCU is shifted out on the MISO pin. The active-low Slave Select (SS) pin must be asserted to initiate a SPI transfer.

The application MCU can initiate a SPI data transfer via a multi-byte transaction. The first byte is the Command/Address byte, and the following bytes are the data bytes as shown in Figure 2 through Figure 3. The SS signal should not be deasserted between bytes. The SPI communications is as follows:

- Command Direction (bit 7) = “0” Enables SPI read transaction. A “1” enables SPI write transactions.
- Command Increment (bit 6) = “1” Enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access, otherwise the same address is accessed.
- Six bits of address.
- Eight bits of data.

The SPI communications interface has a burst mechanism, where the command byte can be followed by as many data bytes as desired. A burst transaction is terminated by deasserting the slave select (SS = 1). For burst read transactions, the application MCU must abide by the timing shown in Figure 12.

The SPI communications interface single read and burst read sequences are shown in Figure 1 and Figure 2, respectively.

The SPI communications interface single write and burst write sequences are shown in Figure 3 and Figure 4, respectively.