

512K x 24 Static RAM Module

Features

- High-density 12-Megabit SRAM module
- Access time: 10 ns
- Single 3.3V power supply
- Low active power(1000 W max.)
- TTL-compatible inputs and outputs
- Available in standard 119-ball BGA
- Interface to Motorola digital signal processor (DSP) and analog devices

Functional Description

The CYM8301BV33 is a 3.3V high-performance 12-Megabit static RAM organized as a 512K words by 24 bits. This module is constructed from three 512K x 8 SRAM dice mounted on a multi layer laminate substrate combined to form a 24 bit SRAM. CYM8301BV33 is a ideal single-chip solution for Motorola's DSP5630X or a two chip solution to Analog Devices ADSP2106XL.

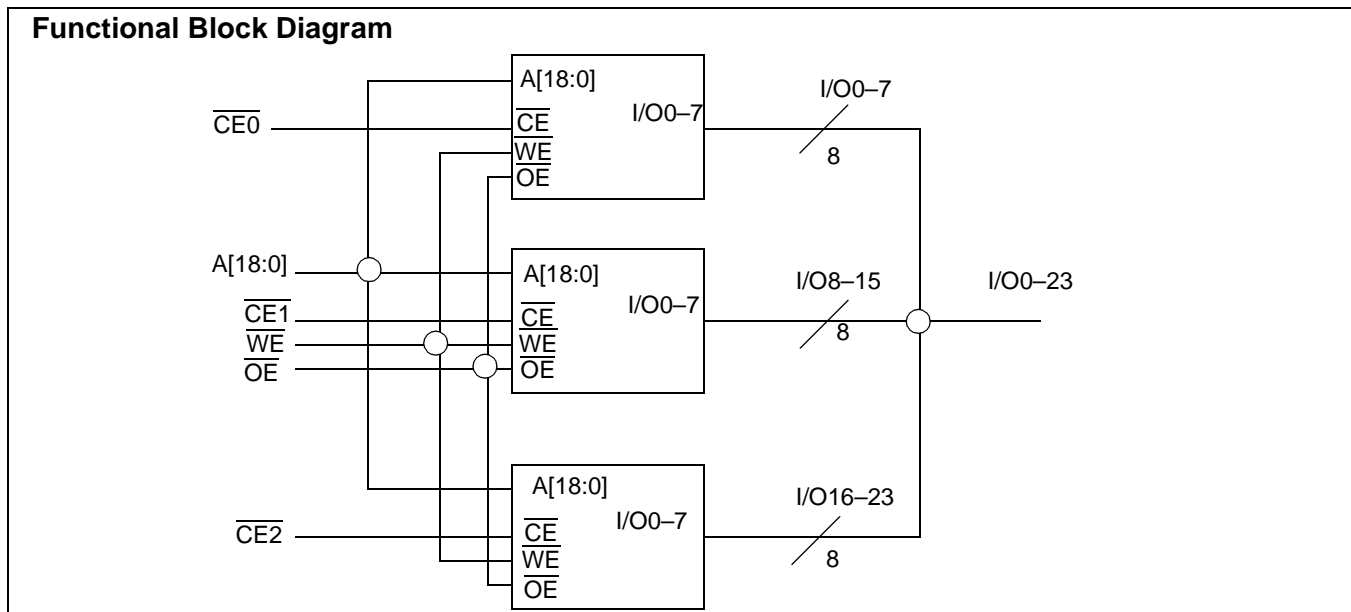
Each data byte is separately controlled by the individual chip selects(CE0,CE1,CE2). CE0 controls I/O0-7. CE1 controls I/O7-15. CE2 controls I/O16-23.

Writing the data bytes into the SRAM is accomplished when the chip select (\overline{CS}_x) controlling that byte is LOW and Write Enable (\overline{WE}) is LOW. Data on the respective input/output pins (I/O) is then written into the memory location specified on the address pins (A0 through A18). Asserting all the (\overline{CS}_x) LOW and (\overline{WE}) LOW will write the entire data (I/O0-23) into the memory. Output Enable (\overline{OE}) is a don't care in a write mode.

Reading a byte is accomplished when the chip select (\overline{CS}_x) controlling that byte is LOW and Write Enable (\overline{WE}) is LOW while the Output Enable (\overline{OE}) is LOW. Under these conditions the contents of the memory location specified on the address pins will all appear on the specified data input/output pins (I/O). Asserting all the (\overline{CS}_x) LOW and (\overline{WE}) LOW with Output Enable (\overline{OE}) LOW will read the entire data (I/O0-23) from the memory.

The data input/output pins (I/O0-23) are placed in a high-impedance state when the device is deselected (\overline{CE}) HIGH, the outputs are disabled (\overline{OE}) HIGH or during a Write operation (\overline{CE} LOW, and \overline{WE} LOW).

For further details on Read and Write conditions, please see the truth table on page 7 of this data sheet.



Selection Guide

		CYM8301BV33-10	CYM8301BV33-12	CYM8301BV33-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial	300	270	255	mA
	Industrial	330	300	285	
Maximum Standby Current	Commercial/Industrial	30	30	30	mA

Pin Configurations
**119 BGA
Top View**

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	$\overline{CE0}$	A	A	NC
C	I/O12	NC	$\overline{CE1}$	NC	$\overline{CE2}$	NC	I/O0
D	I/O13	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O1
E	I/O14	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O2
F	I/O15	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O3
G	I/O16	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O4
H	I/O17	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O5
J	NC	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	NC
K	I/O18	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O6
L	I/O19	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O7
M	I/O20	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O8
N	I/O21	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	I/O9
P	I/O22	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	I/O10
R	I/O23	A	NC	NC	NC	A	I/O11
T	NC	A	A	\overline{WE}	A	A	NC
U	NC	A	A	\overline{OE}	A	A	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to 4.6V
 DC Voltage Applied to Outputs in High-Z State^[1]..... -0.5V to $V_{CC} + 0.5V$
 DC Input Voltage^[1]..... -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%

Electrical Characteristics Over the Operating Range

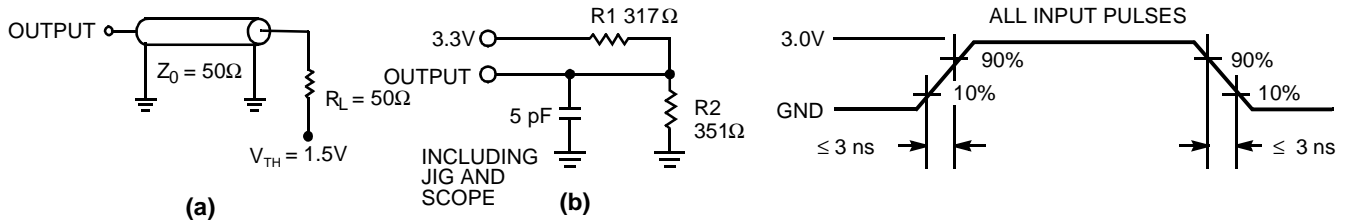
Parameter	Description	Test Conditions ^[2]	CYM8301BV33-10		CYM8301BV33-12/15		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	$V_{CC} + 0.3$	2.2	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage ^[1]		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-10	+10	-10	+10	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-10	+10	-10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$		300		300	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V_{CC} , $CE \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$		150		150	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC} , $CE \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$		30		30	mA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 3.3V$	8	pF
C_{OUT}	Output Capacitance		8	pF

Notes:

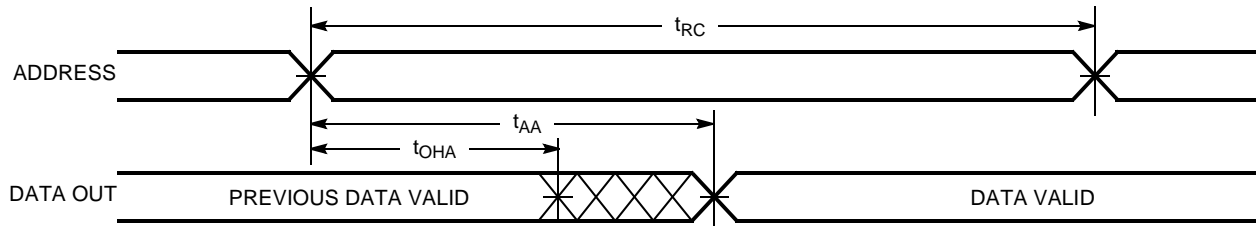
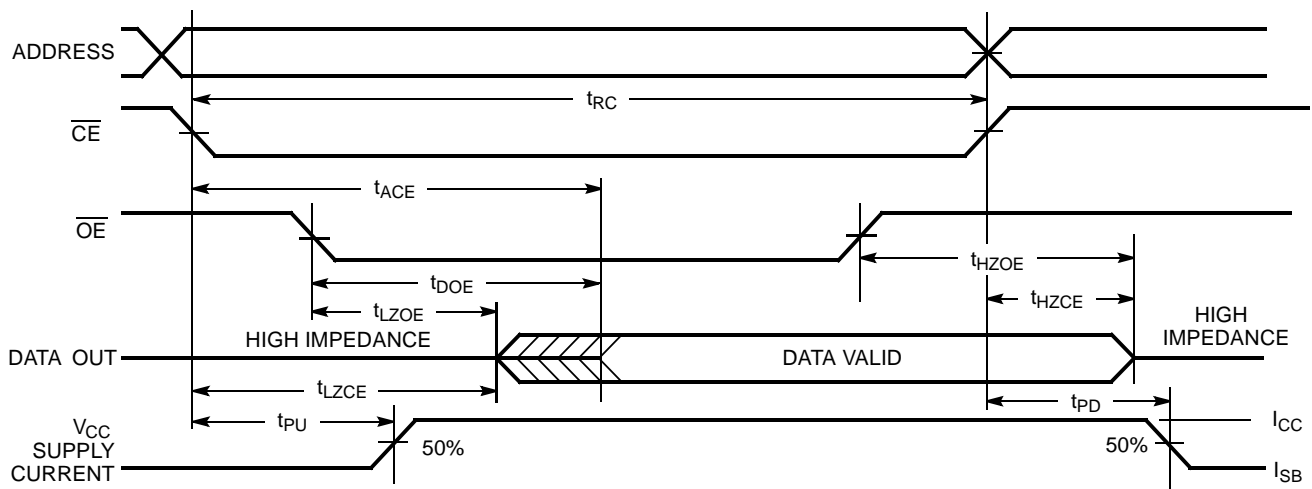
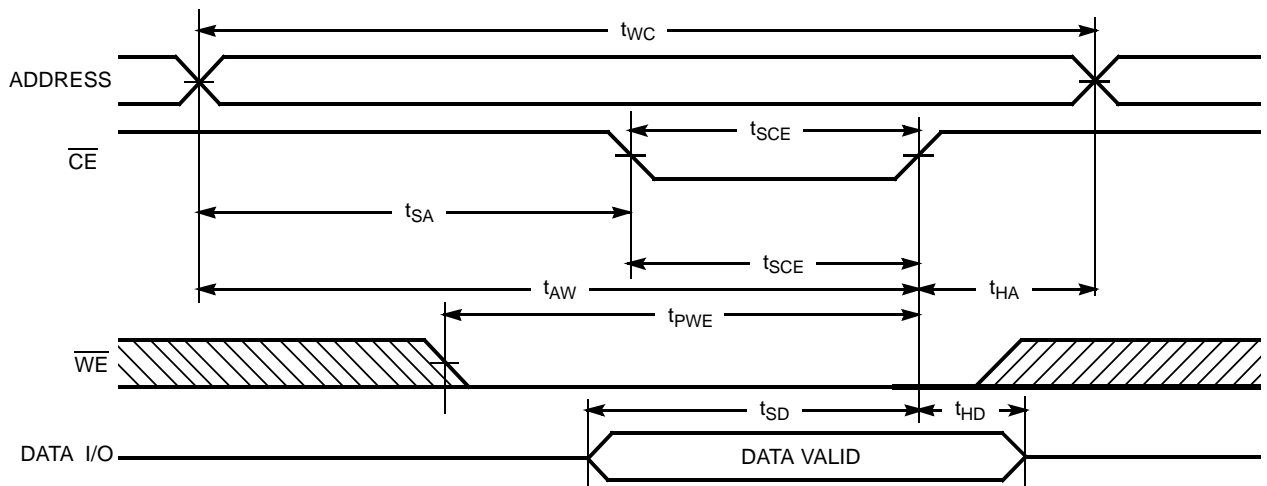
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- CE is a combination of CE1, CE2 and CE3.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Switching Characteristics^[4] Over the Operating Range

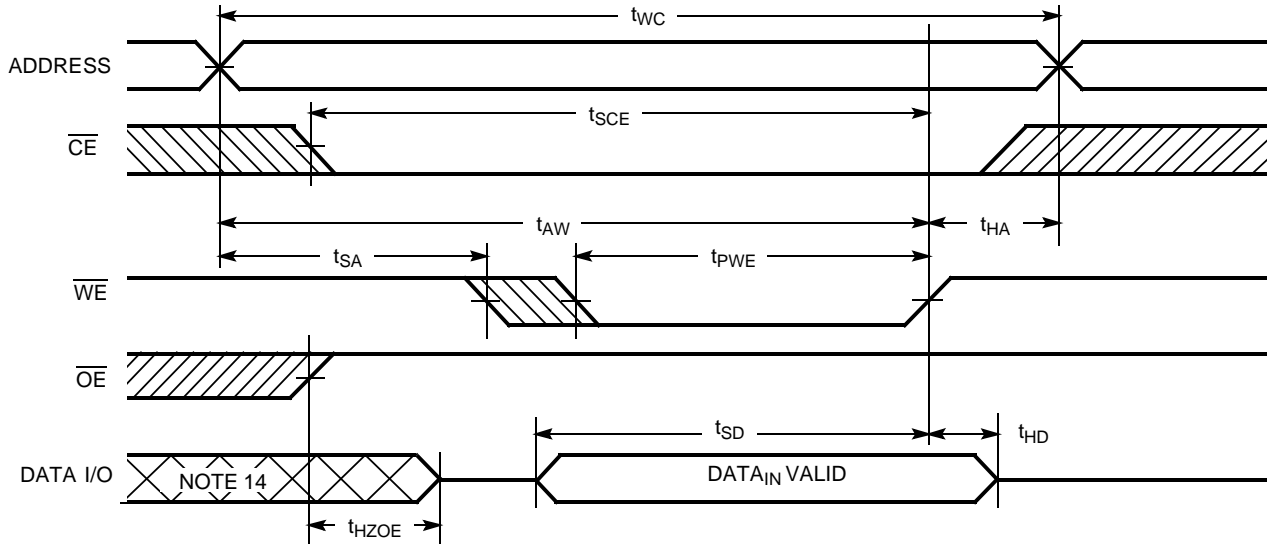
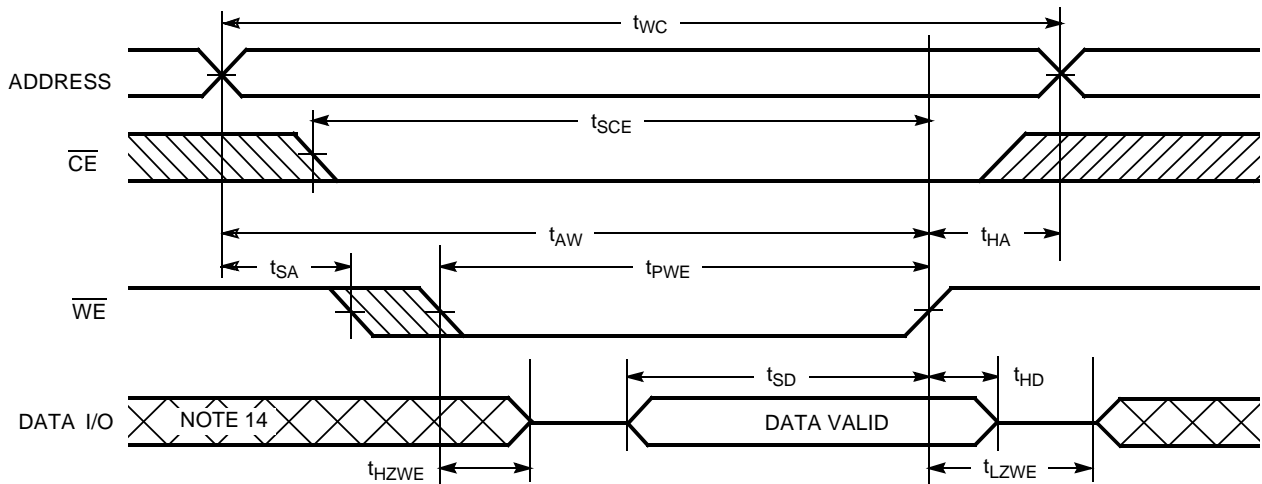
Parameter	Description ^[2]	CYM8301BV-10		CYM8301BV-12		CYM8301BV-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	\overline{CE} active to Data Valid		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		7		7.5		8.5	ns
t_{LZOE}	\overline{OE} LOW to Low-Z	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High-Z ^[5, 6]		5		6		7	ns
t_{LZCE}	\overline{CE} Active to Low-Z ^[6]	3		3		3		ns
t_{HZCE}	\overline{CE} Inactive to High-Z ^[5, 6]		5		6		7	ns
t_{PU}	\overline{CE} Active to Power-up	0		0		0		ns
t_{PD}	\overline{CE} Inactive to Power-down		10		12		15	ns
Write Cycle^[7, 8]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	\overline{CE} active to Write End	9		9		9		ns
t_{AW}	Address Set-up to Write End	9		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	8		10		11		ns
t_{SD}	Data Set-up to Write End	6		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[6]	3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[5, 6]		5		6		7	ns

Notes:

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} .
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal Write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms
Read Cycle No. 1^[9, 10]

Read Cycle No. 2 (\overline{OE} Controlled)^[2, 10, 11]

Write Cycle No. 1 (\overline{CE} Controlled)^[2, 12, 13]

Notes:

9. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
10. \overline{WE} is HIGH for Read cycle.
11. Address valid prior to or coincident with \overline{CE} transition LOW.
12. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
13. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During Write)^[12, 13]

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[2, 13]

Note:

14. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

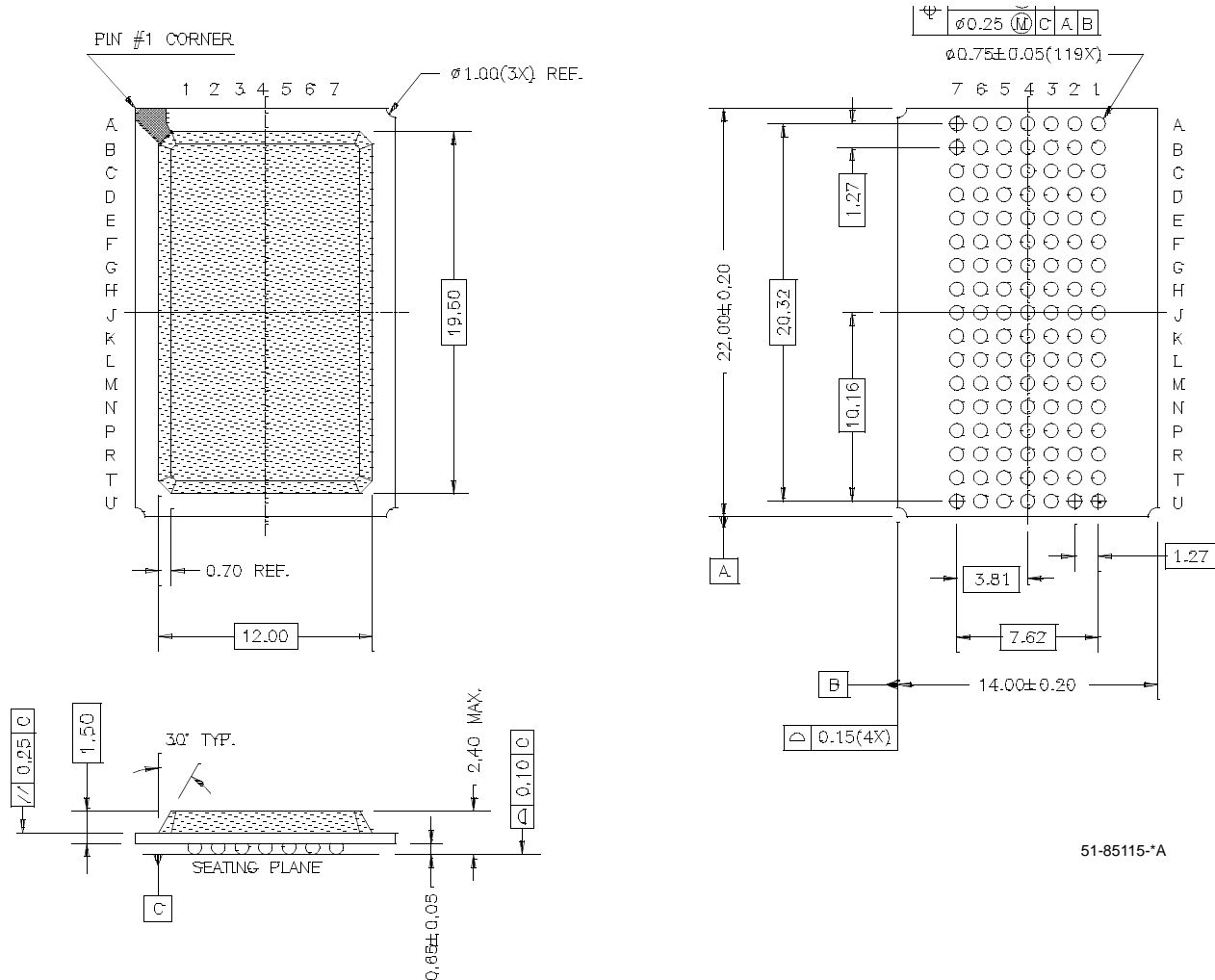
CE1	CE2	CE3	WE	OE	I/O₀-I/O₂₃	Mode
H	H	H	X	X	High-Z	Deselect/Power-down
L	L	L	H	L	Data Out (I/O0-23)	Read
L	L	L	H	H	I/O High-Z	Power-down
L	H	H	H	L	Data Out (I/O0-7) I/O8-23 in High-Z	Read
H	L	H	H	L	Data Out (I/O8-15) I/O0-7 in High-Z I/O16-23 in High-Z	Read
H	H	L	H	L	Data Out (I/O16-23) I/O0-15 in High-Z	Read
L	L	L	L	X	Data In (I/O0-23)	Write
L	H	H	L	X	Data In (I/O0-7)	Write
H	L	H	L	X	Data In (I/O8-15)	Write
H	H	L	L	X	Data In (I/O16-23)	Write

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CYM8301BV33 - 10BGC	BG119	119-ball BGA	Commercial
	CYM8301BV33 - 10BGI	BG119	119-ball BGA	Industrial
12	CYM8301BV33 - 12BGC	BG119	119-ball BGA	Commercial
	CYM8301BV33 - 12BGI	BG119	119-ball BGA	Industrial
15	CYM8301BV33 - 15BGC	BG119	119-ball BGA	Commercial
	CYM8301BV33 - 15BGI	BG119	119-ball BGA	Industrial

Package Diagram

119-ball PBGA (14 x 22 x 2.4 mm) BG119



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**	114945	05/20/02	DFP	New Data Sheet