CYM1841B

256K x 32 Static RAM Module

Features

- **High-density 8-megabit SRAM module**
- **32-bit standard footprint supports densities from 16K x 32 through 1M x 32**
- **High-speed CMOS SRAMs**
  - **Access time of 12 ns**
- **Low active power**
  - **5.3W (max.) at 25 ns**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.58 in.**
- **Available in ZIP, SIMM, and angled SIMM footprint**
- **72-pin SIMM version compatible with 1M x 32 (CYM1851)**

Functional Description

The CYM1841B is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from two 256K x 16 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs are both LOW. Data on the Input/Output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the Chip Select ($\overline{CS}$) LOW while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data Input/Output pins (I/O).

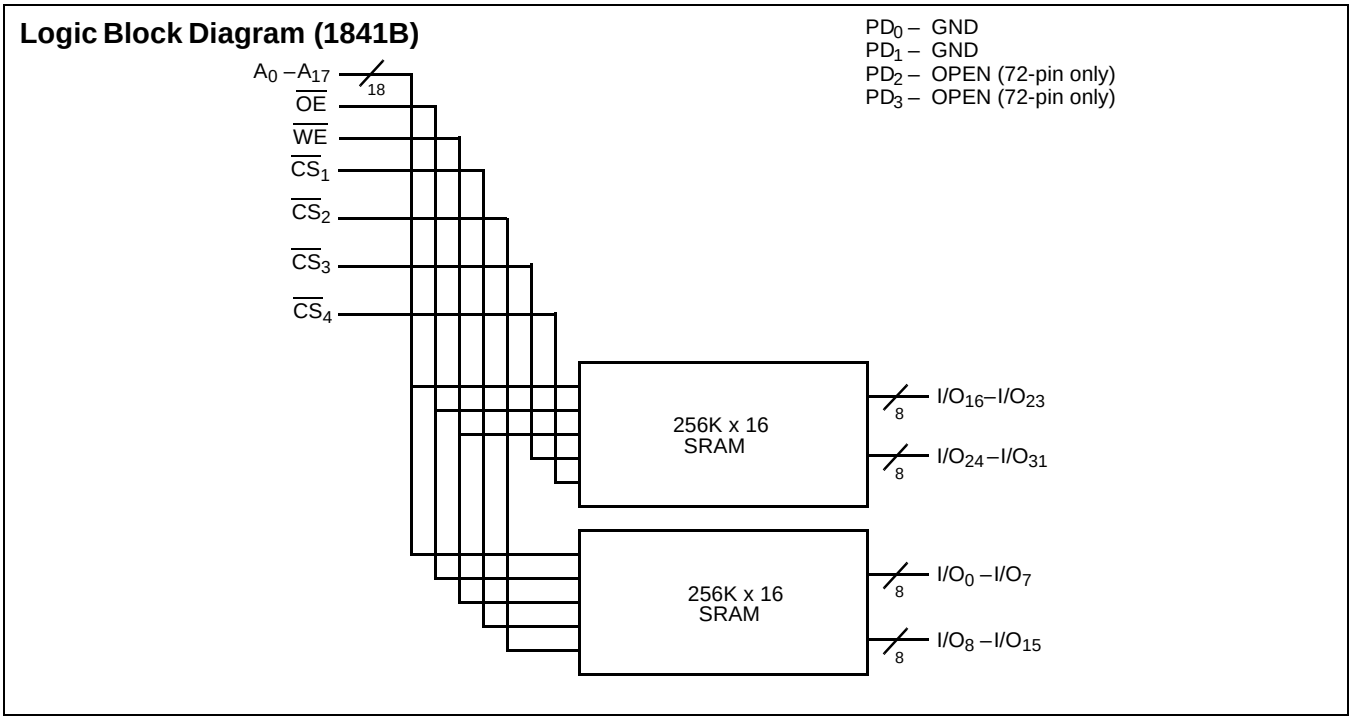
The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

A 72-pin SIMM is offered for compatibility with the 1M x 32 CYM1851. This version is socket upgradable to the CYM1851.

Both the 64-pin and 72-pin SIMM modules are available with either tin-lead or 10 micro-inches of gold flash on the edge contacts.

Logic Block Diagram (1841B)

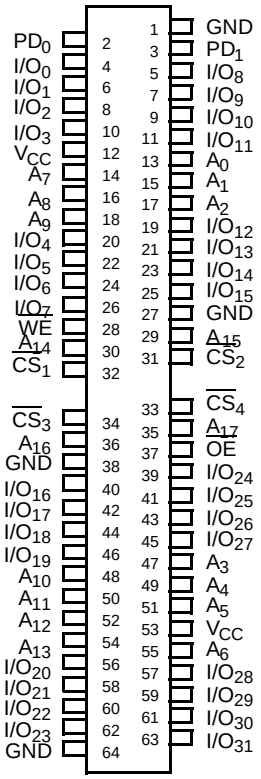


Selection Guide

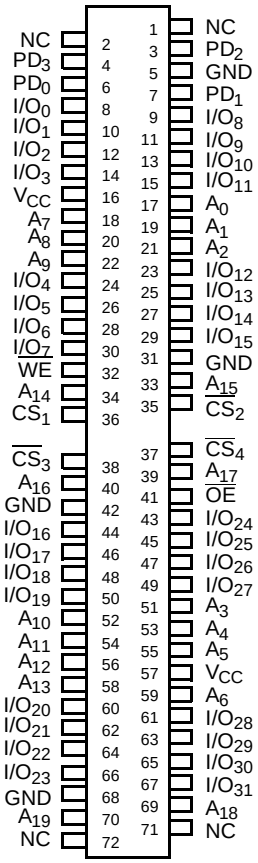
	1841B-15	1841B-20	1841B-25	1841B-35	1841B-45	Unit
Maximum Access Time	15	20	25	35	45	ns
Maximum Operating Current	400	380	380	340	340	mA
Maximum Standby Current	80	80	80	80	80	mA

Pin Configurations

64-Pin ZIP/SIMM Top View



72-Pin SIMM Top View



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –55°C to +125°C

Ambient Temperature with Power Applied ..... –10°C to +85°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

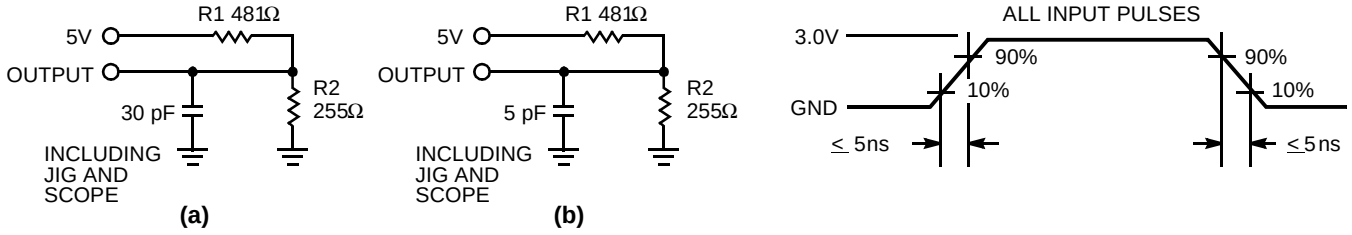
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1841B-15		1841B-20		1841B -25, 35, 45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–3	+3	–3	+3	–3	+3	uA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–2	+2	–2	+2	–2	+2	uA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		400		380		340	mA
I_{SB1}	Automatic $\overline{CS}$ Power-down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		80		80		80	mA
I_{SB2}	Automatic $\overline{CS}$ Power-down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V		6		6		6	mA

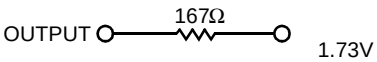
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[3]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	16	pF
C_{OUT}	Output Capacitance		16	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.
3. 20 pF on $\overline{CS}$, 70 pF all others.

Switching Characteristics Over the Operating Range[4]

Parameter	Description	1841B-15		1841B-20		1841B-25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	15		20		25		ns
t_{AA}	Address to Data Valid		15		20		25	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		7		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		4		4		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		7		8		8	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		15		18		18	
Write Cycle[7]								
t_{WC}	Write Cycle Time	15		20		25		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		15		20		ns
t_{AW}	Address Set-up to Write End	10		18		20		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		ns
t_{SD}	Data Set-up to Write End	7		8		8		ns
t_{HD}	Data Hold from Write End	1		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	6	0	8	0	8	ns

Switching Characteristics Over the Operating Range [4]

Parameter	Description	1841B-35		1841B-45		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	35		45		ns
t_{AA}	Address to Data Valid		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ LOW to High Z		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45	ns
Write Cycle[7]						
t_{WC}	Write Cycle Time	35		45		ns

Notes:

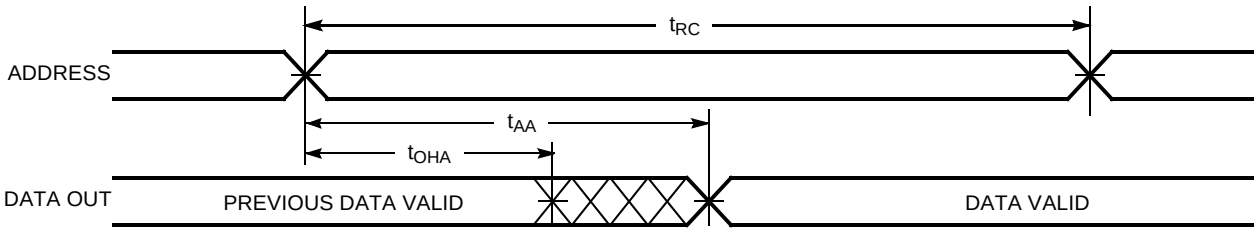
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[4]

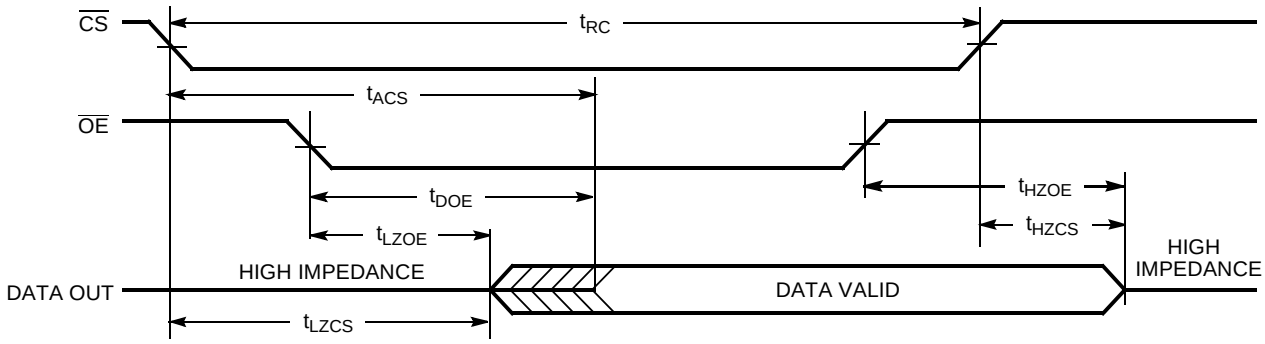
Parameter	Description	1841B-35		1841B-45		Unit
		Min.	Max.	Min.	Max.	
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		ns
t_{AW}	Address Set-Up to Write End	30		40		ns
t_{HA}	Address Hold from Write End	2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		ns
t_{SD}	Data Set-Up to Write End	20		25		ns
t_{HD}	Data Hold from Write End	2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	15	0	15	ns

Switching Waveforms

Read Cycle No. 1[8, 9]



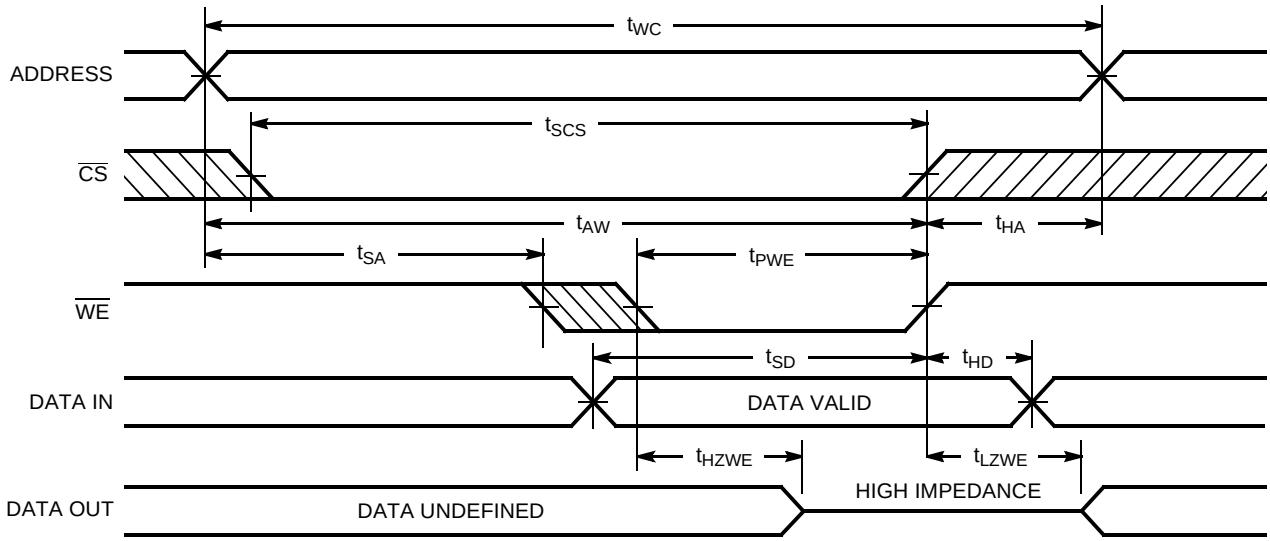
Read Cycle No. 2[8, 10]



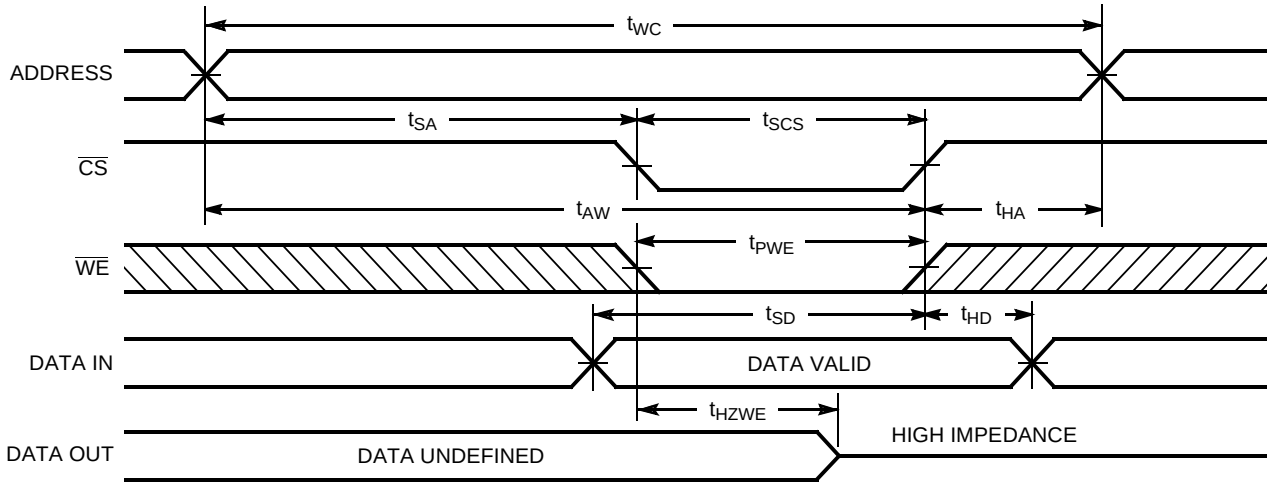
Notes:
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11]



Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

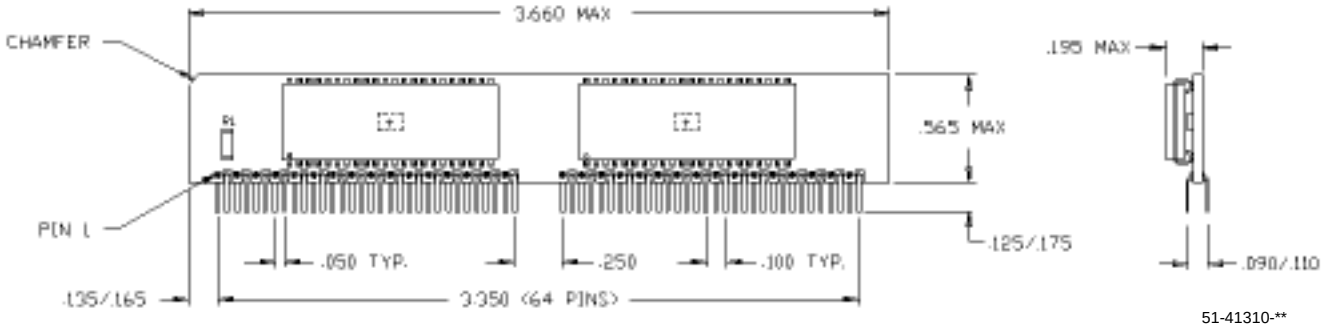
Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1841BPM-15C	PM03	64-Pin Plastic SIMM Module	Commercial
	CYM1841BPZ-15C	PZ08	64-Pin Plastic ZIP Module	
	CYM1841BP7-15C	PM50	72-Pin Plastic SIMM Module	
20	CYM1841BPM-20C	PM03	64-Pin Plastic SIMM Module	Commercial
	CYM1841BPZ-20C	PZ08	64-Pin Plastic ZIP Module	
	CYM1841BP7-20C	PM50	72-Pin Plastic SIMM Module	
25	CYM1841BPM-25C	PM03	64-Pin Plastic SIMM Module	Commercial
	CYM1841BPZ-25C	PZ08	64-Pin Plastic ZIP Module	
	CYM1841BP7-25C	PM50	72-Pin Plastic SIMM Module	
35	CYM1841BPM-35C	PM03	64-Pin Plastic SIMM Module	Commercial
	CYM1841BPZ-35C	PZ08	64-Pin Plastic ZIP Module	
	CYM1841BP7-35C	PM50	72-Pin Plastic SIMM Module	
45	CYM1841BPM-45C	PM03	64-Pin Plastic SIMM Module	Commercial
	CYM1841BPZ-45C	PZ08	64-Pin Plastic ZIP Module	
	CYM1841BP7-45C	PM50	72-Pin Plastic SIMM Module	

Package Diagrams

64-Pin ZIP Module – PZ08



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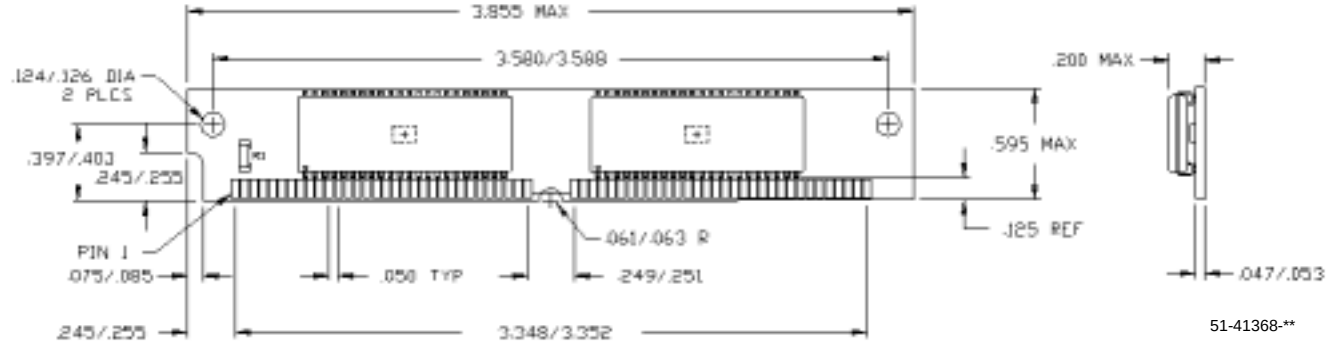
64-Pin Plastic SIMM Module – PM03



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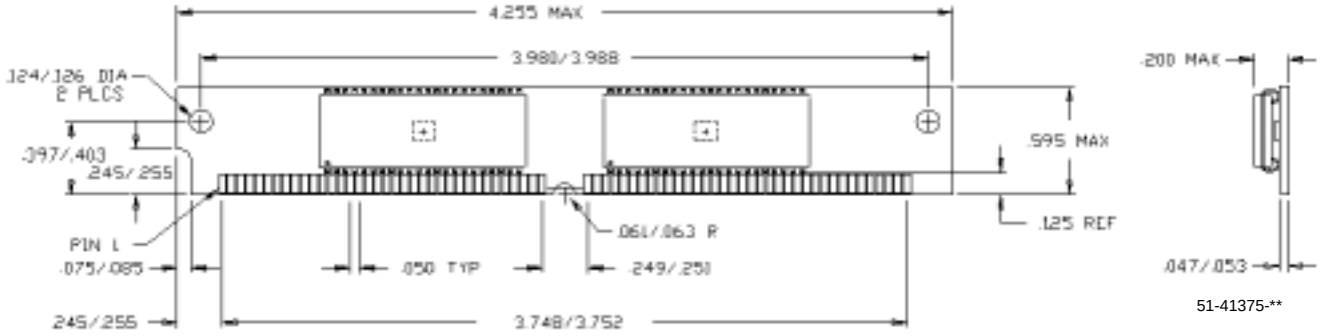
72-Pin Plastic SIMM Module – PM50



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Document History Page

Document Title: CYM1841B 256K x 32 Static RAM Module Document Number: 38-05261				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114352	3/22/02	DSG	Change from Spec number: 38-M-00031 to 38-05261
*A	125739	04/28/03	CS	Changed Iix and Ioz unit to uA from mA and amended incorrected values shown on pages 2, 3 and 4.