# 16M (1M x 16) SRAM

## Features

- **Very high speed: 85 ns**
- **Advanced low-power MoBL® architecture**
- **Wide voltage range:**
  - **— $V_{CC}$ range: 1.7V – 2.25V**
  - **— $V_{CCQ}$ (I/O) range: 1.7V – $V_{CC}$**
- **Ultra-low active, standby power**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **1T SRAM memory cell**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

## Functional Description[1]

The CY81U016X16B7A MoBL3™ is a high-performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL) in portable applications such as cellular telephones. The device can be put into standby mode when deselected ($\overline{CE}$ HIGH, or both $\overline{BLE}$ and $\overline{BHE}$ HIGH). The input/output pins ($I/O_0$ through $I/O_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH, or both $\overline{BLE}$ and $\overline{BHE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

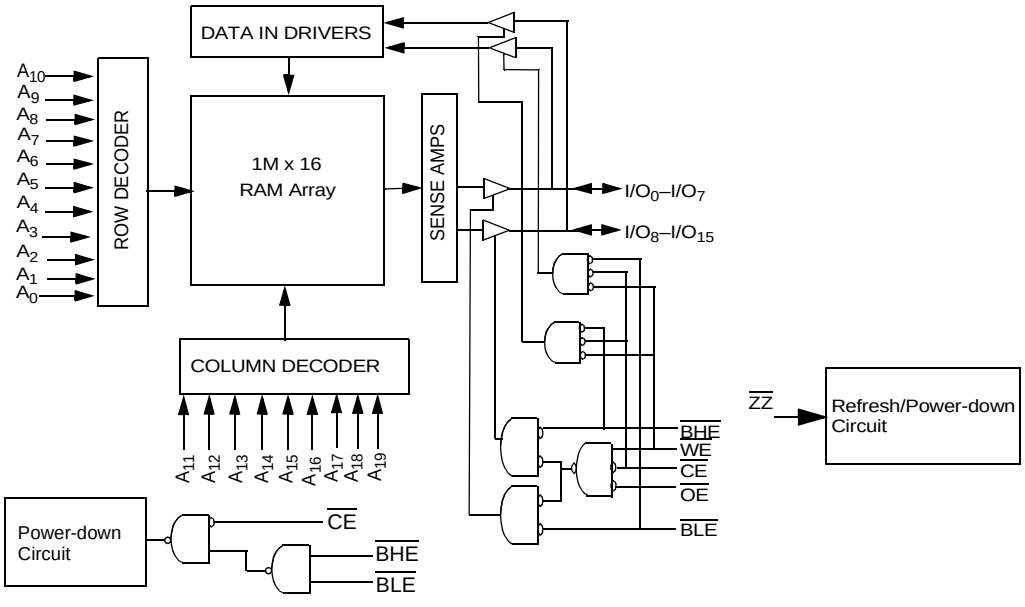
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) LOW and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_0$ through $I/O_7$), is written into the location specified on the address pins ($A_0$ through $A_{19}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_8$ through $I/O_{15}$) is written into the location specified on the address pins ($A_0$ through $A_{19}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) LOW and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on $I/O_8$ to $I/O_{15}$. See the truth table at the back of this datasheet for a complete description of read and write modes.

This SRAM has multiple power down functions. The $\overline{ZZ}$ pin will put the SRAM into a deep sleep mode, where the data is not retained in the SRAM. The Variable Address Mode allows the user to retain data in a section of the SRAM and reduce the standby current. The CY81U016X16B7A has the deep sleep mode enabled on Power up. The VAR register can be used to disable the deep sleep mode.

The CY81U016X16B7A MoBL3 is available in a 48-ball FBGA package.

## Logic Block Diagram



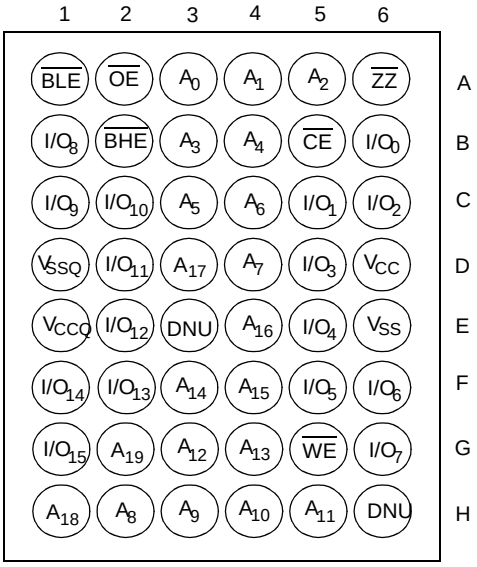

**Note:**

1. For best practice recommendations, please refer to the CY application note “System Design Guidelines” on http://www.cypress.com.

## Pin Configuration[2, 3]

**FBGA**

**Top View**




**Notes:**
2. DNU pins are to be connected to Vss or left open.
3. $V_{SSQ}$ is the Ground pin for the I/O drivers. It should be connected to $V_{SS}$.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential-V25 ..... –0.2V to +3.3V

DC Voltage Applied to Output in High-Z State[4, 5, 6].....–0.2V to $V_{CC}$ + 0.3V

DC Input Voltage[4, 5, 6] .....–0.2V to $V_{CC}$ + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

## Operating Range

| Ambient Temperature | $V_{CC}$ | $V_{CCQ}$ |
|---|---|---|
| –25°C to +85°C | 1.7 to 2.25V | 1.7V to $V_{CC}$ |

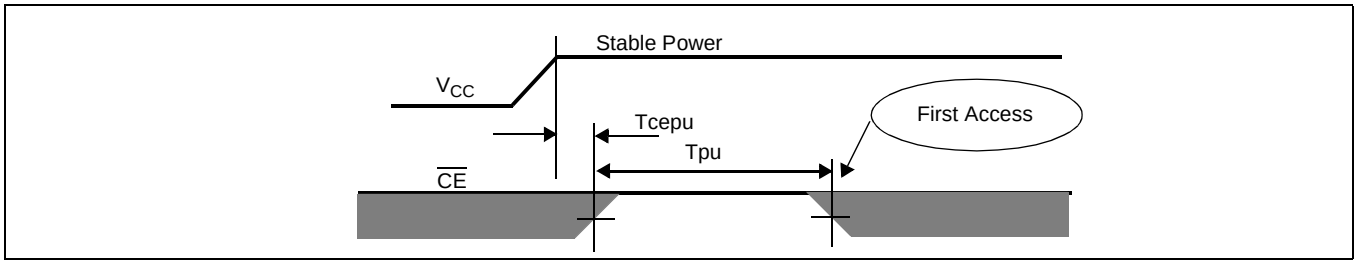
## Product Portfolio

| Product | $V_{CC}$ Range | | | Cycle Time | $t_{AA}$ | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating ($I_{CC}$) | | | | Standby ($I_{SB2}$) | |
| | | | | | | f = 1 MHz | | f = $f_{max}$ | | | |
| | Min. | $V_{CC(typ.)}$ | $V_{CC(max.)}$ | | | Typ.[7] | Max. | Typ.[7] | Max. | Typ.[7] | Max. |
| CY81U016X16B7A | 1.7V | 1.8V | 2.25V | 85 ns | 85 ns | | TBD | | 15 mA | | 60µA |

## Power-up Characteristics

The 16M needs to have a initialization time before accesses can be started on the device.

The initialization sequence is shown in the figure below. Chip Select(CE) should be HIGH within 100us of Vcc getting to the stable value. CE should be maintained at a HIGH state for a minimum of 3 ms after power-up.




| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Tcepu | Chip Enable High After Stable Vcc | | | 100 | µs |
| Tpu | Chip Enable Low After Stable Vcc | 3 | | | ms |

**Notes:**

4. Overshoot: $V_{CC}$ + 0.2V, pulse width < 20 ns.
5. Undershoot: –0.2V, pulse width < 20 ns.
6. Overshoot and undershoot specifications are characterized and are not 100% tested.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ.)}$, $T_A$ = 25°C

## Variable Address Refresh

### Description

The variable address mode allows customers to turn off sections of the die to save standby current. The 16M MoBL3 is divided into four 4M sections allowing certain sections to be active (i.e., refreshed). The variable address mode also allows a customer to go into a low-power mode with $\overline{ZZ}$ tied low and keep the data in a certain section of memory.

### Function

At power up, all four sections of the die are activated and the SRAM enters into its default state of full memory size and refresh space.

MoBL3 provides three distinct operation modes for reducing standby power:

a. Reduced Memory Size Operation

b. Partial Array Refresh

c. Deep Sleep Mode.

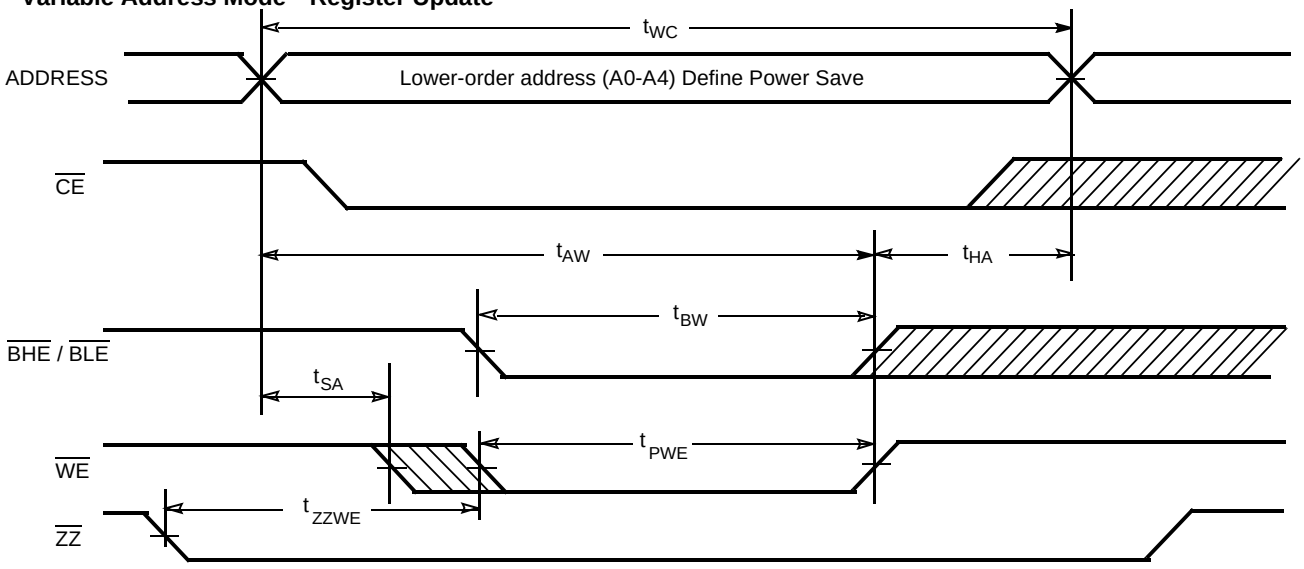
In the Reduced Memory Size (RMS) operation, the SRAM can be operated as a reduced size SRAM. For example, one could operate the 16M SRAM as an 4M, 8M, or a 12M memory block. The protocol to turn on/off the sections of the memory is given in the following pages. The RMS mode is enabled after $\overline{ZZ}$ goes high and remains in RMS mode after $\overline{ZZ}$ goes high. To revert back to a complete 16M SRAM, the protocol outlined on the the next page will have to be followed, along with the bit pattern definitions shown on page 6.

In the Partial Array Refresh (PAR), the SRAM will only refresh certain portions of the memory, as configured by the user. This mode is only for standby and is applicable as long as $\overline{ZZ}$ remains low. Once $\overline{ZZ}$ returns high in this mode, the SRAM goes back to operating in full address refresh. The protocol shown in next figure will have to be followed to turn on/off this mode of operation. Once the Variable Address (VA) register is updated, all future PAR accesses will use the contents of the VA register when $\overline{ZZ}$ returns low. If the customer wants to change the PAR space, the VA register must be updated per next figure.

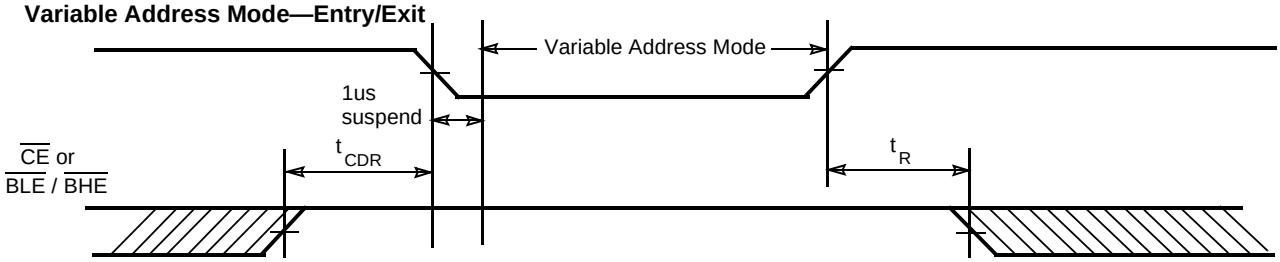
If the Variable Address (VA) register is not updated after power up, the SRAM will be in its default state. In the default state the whole memory array will be refreshed and driving $\overline{ZZ}$ low places the SRAM into a deep sleep mode after 1us. Once in the deep sleep mode, data integrity in the SRAM is not guaranteed. If the customer updates the VA register, then address bit 4 (A4) must be set to 1, indicating to the SRAM that the deep sleep mode is disabled. At any point of time, one could drive $\overline{ZZ}$ low and change the VA register's A4 bit back to 0. Then the SRAM enters deep sleep when $\overline{ZZ}$ is driven low and remains in deep sleep mode until $\overline{ZZ}$ is driven high. Once the SRAM enters into Deep Sleep Mode the content of the VA register is destroyed and the part returns to its default state.

## Variable Address Refresh Switching Diagrams

**Variable Address Mode—Register Update**[8]




**Variable Address Mode—Entry/Exit**



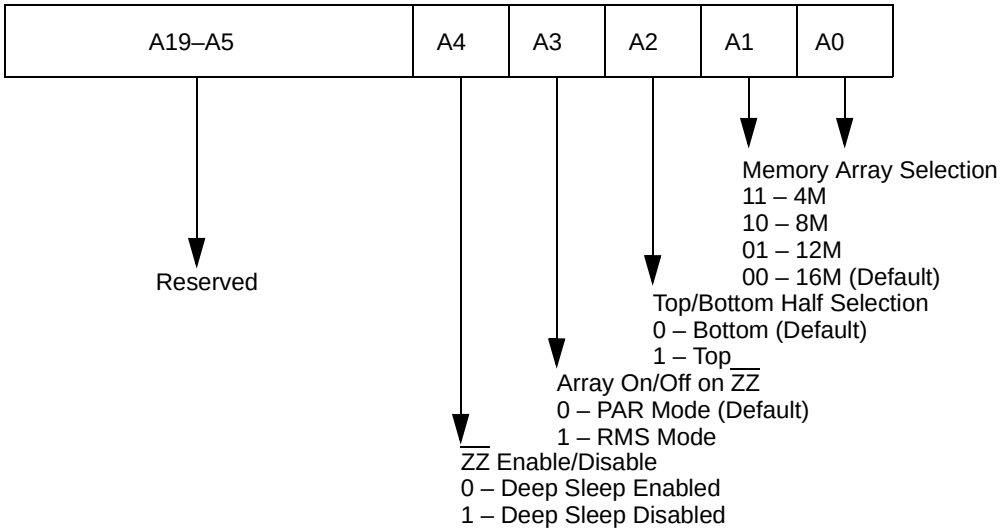

**Note:**

8. $\overline{OE}$ and the data pins are in a don't care state while the device is in variable address mode.

## Variable Address Space Timings[9]

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{ZZWE}$ | $\overline{ZZ}$ LOW to $\overline{WE}$ LOW | | 1000 | ns |
| $t_{CDR}$ | Chip deselect to $\overline{ZZ}$ LOW | 0 | | ns |
| $t_R$[10] | Operation Recovery Time (Deep Sleep Mode only) | 200 | | µs |
| $t_{ZZMIN}$ | Deep Sleep Mode Time | 10 | | µs |

## Variable Address Space—Register



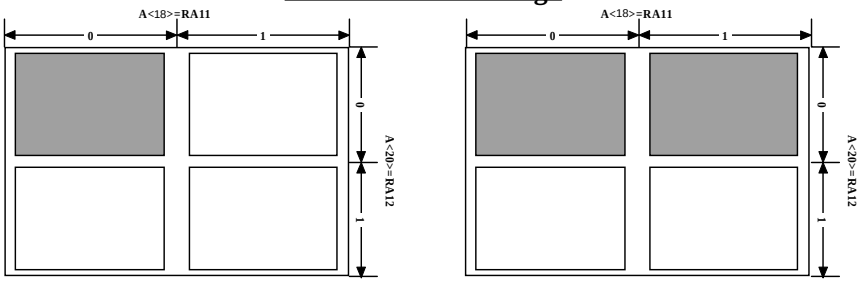

## Variable Address Space—Address Patterns

| Partial Array Refresh Mode (A3=0, A4=1) | | | | | |
|---|---|---|---|---|---|
| **A2** | **A1, A0** | **Refresh Section** | **Address** | **Size** | **Density** |
| 0 | 11 | One Fourth of the Die | 00000h - 3FFFFh (A19=A18=0) | 256K x 16 | 4M |
| 0 | 10 | Half of the Die | 00000h - 7FFFFh (A19=0) | 512M x 16 | 8M |
| 0 | 01 | Three-Fourths of the Die | 00000h - BFFFFh (A19:A18 != 11) | 768K x 16 | 12M |
| 1 | 11 | One Fourth of the Die | C0000h - FFFFFh (A19=A18=1) | 256K x 16 | 4M |
| 1 | 10 | Half of the Die | 80000h - FFFFFh (A19=1) | 512M x 16 | 8M |
| 1 | 01 | Three-Fourths of the Die | 40000h - FFFFFh (A19:A18 != 00) | 768K x 16 | 12M |
| **Reduced Memory Size Mode (A3=1, A4=1)** | | | | | |
| 0 | 11 | One Fourth of the Die | 00000h - 3FFFFh (A19=A18=0) | 256K x 16 | 4M |
| 0 | 10 | Half of the Die | 00000h - 7FFFFh (A19=0) | 512M x 16 | 8M |
| 0 | 01 | Three-Fourths of the Die | 00000h - BFFFFh (A19:A18 != 11) | 768K x 16 | 12M |
| 0 | 00 | Full Die | 00000h - FFFFFh | 1M x 16 | 16M |
| 1 | 11 | One Fourth of the Die | C0000h - FFFFFh (A19=A18=1) | 256K x 16 | 4M |
| 1 | 10 | Half of the Die | 80000h - FFFFFh (A19=1) | 512M x 16 | 8M |
| 1 | 01 | Three-Fourths of the Die | 40000h - FFFFFh (A19:A18 != 00) | 768K x 16 | 12M |
| 1 | 00 | Full Die | 00000h - FFFFFh | 1M x 16 | 16M |

**Notes:**
9. All other timing parameters are as shown in the datasheets.
10. $t_R$ applies only in the deep sleep mode.

## Memory Block Split

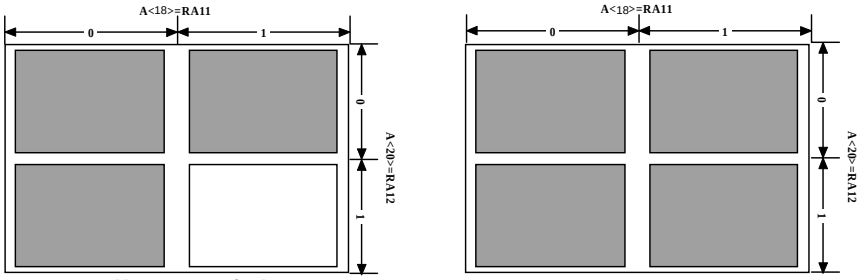
### Bottom Address Range




**1/4 Address Space Refresh**
Active Address Space:
A0-A17
A<18,19> = <0,0>




**1/2 Address Space Refresh**
Active Address Space:
A0-A18
A<19>=<0>

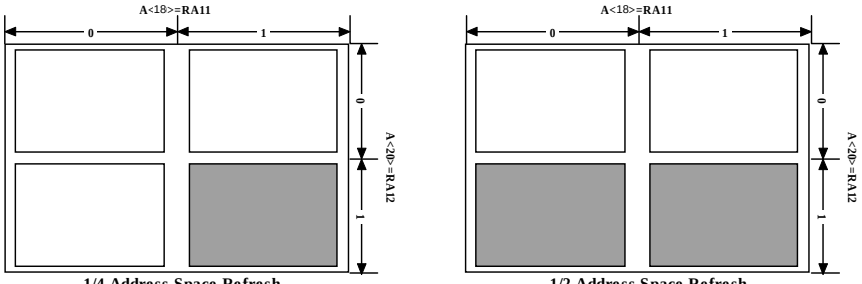



**3/4 Address Space Refresh**
Active Address Space:
A0-A19
A<18,19> = <0,0>,<1,0>,<0,1>




**Full Address Space Refresh**
Active Address Space:
A0-A19
A<1819> = <X,X>

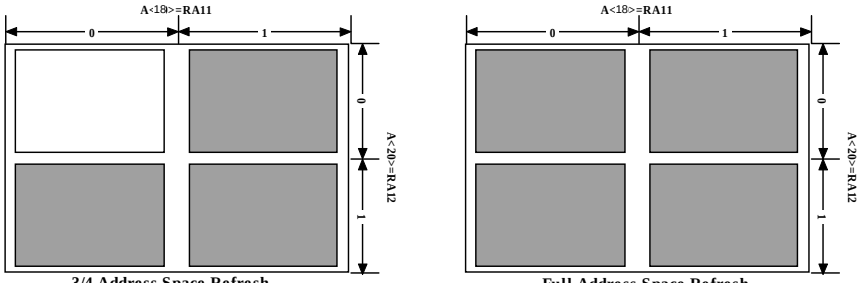
### Top Address Range




**1/4 Address Space Refresh**
Active Address Space:
A0-A17
A<18,19> = <1,1>




**1/2 Address Space Refresh**
Active Address Space:
A0-A18
A<19>=<1>




**3/4 Address Space Refresh**
Active Address Space:
A0-A19
A<18,19> = <1,0>,<0,1>,<1,1>




**Full Address Space Refresh**
Active Address Space:
A0-A19
A<18,19> = <X,X>

## Electrical Characteristics Over the Operating Range[4, 5, 6]

| Parameter | Description | Test Conditions | CY81U016X16B7A | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ.[7] | Max. | |
| $V_{OH}$[11] | Output HIGH Voltage | $I_{OH}$ = –0.1 mA | $V_{CCQ}$ – 0.2 | | | V |
| $V_{OL}$[11] | Output LOW Voltage | $I_{OL}$ = 0.1 mA | | | 0.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | 1.4 | | $V_{CC}$ + 0.2V | V |
| $V_{IL}$ | Input LOW Voltage | | –0.2 | | 0.4 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | –1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = 1/$t_{RC}$, CMOS Levels, $V_{CC}$ = Max | | | 15 | mA |
| | | $I_{OUT}$ = 0 mA, f=1MHz, CMOS Levels, $V_{CC}$ = Max | | | TBD | mA |
| $I_{SB1}$ | Automatic CE Power-down Current—CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.3V or CE ≤ 0.3V $V_{IN}$ ≥ $V_{CC}$ – 0.3V or $V_{IN}$ ≤ 0.3V, f = $f_{MAX}$ (Address and Data Only), f=0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, $\overline{BLE}$) $V_{CC}$ = Max | | | 100 | µA |
| $I_{SB2}$ | Automatic CE Power-down Current—CMOS Inputs | $\overline{CE}$ ≥ $V_{CC}$ – 0.3V or CE ≤ 0.3V $V_{IN}$ ≥ $V_{CC}$ – 0.3V or $V_{IN}$ ≤ 0.3V, f=0, $V_{CC}$ = Max | | | 60 | µA |

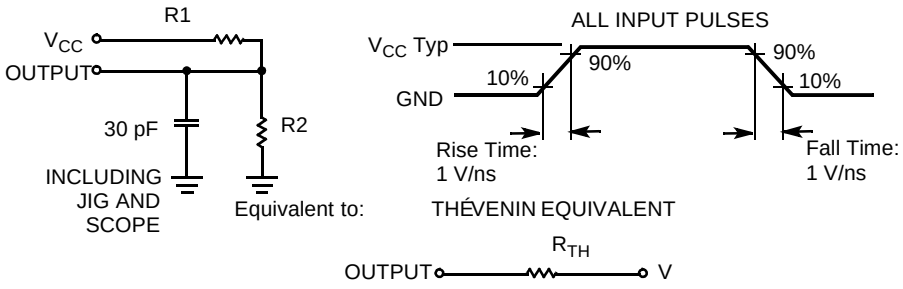
## Capacitance[12]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC(typ)}$ | 6 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

## Thermal Resistance

| Parameter | Description | Test Conditions | BGA | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient)[12] | Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board | 55 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case)[12] | | 16 | °C/W |

## AC Test Loads and Waveforms




| Parameters | 1.8V I/O | Unit |
|---|---|---|
| R1 | 14K | Ohms |
| R2 | 14K | Ohms |
| $R_{TH}$ | 7K | Ohms |
| $V_{TH}$ | 0.9 | Volts |

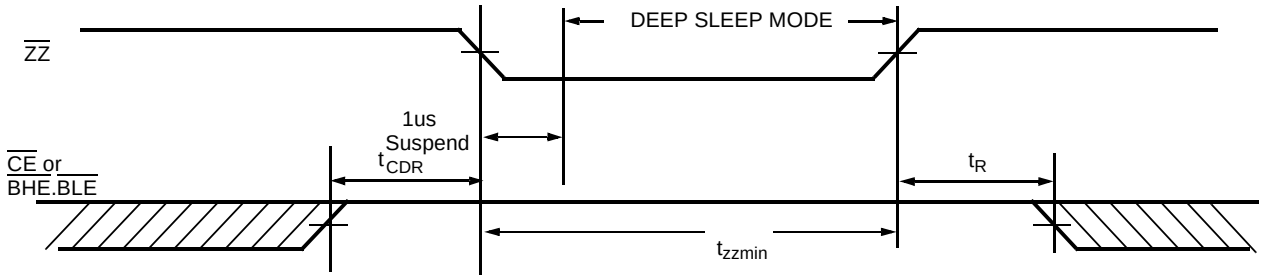
**Notes:**

11. For $I_{OH}$ = –0.4 mA, $V_{OH}$ = 0.8 x $V_{CCQ}$; for $I_{OL}$ = 0.4 mA, $V_{OL}$ = 0.2 x $V_{CCQ}$.
12. Tested initially and after any design or process changes that may affect these parameters.

## Deep Sleep Mode[13]

| Parameter | Description | Conditions | Min. | Typ.[7] | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CCDS}$ | Deep Sleep Current | $\overline{CE} \geq V_{CC} - 0.2V$, $\overline{ZZ} \leq V_{IL}$<br>$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$<br>No input may exceed $V_{CC} + 0.2V$ | | 7 | 10 | µA |
| $t_{CDR}$[13] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$ | Operation Recovery Time | | 200 | | | µs |
| $t_{zzmin}$ | Deep Sleep mode Time | | 10 | | | µs |

## Deep Sleep Waveform[14]




## Switching Characteristics Over the Operating Range[15]

| Parameter | Description | 85 ns | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **Read Cycle** | | | | |
| $t_{RC}$ | Read Cycle Time | 85 | | ns |
| $t_{AA}$ | Address to Data Valid | | 85 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 85 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 35 | ns |
| $t_{LZOE}$[19] | $\overline{OE}$ LOW to Low-Z[16] | 5 | | ns |
| $t_{HZOE}$[19] | $\overline{OE}$ HIGH to High-Z[16, 17] | | 25 | ns |
| $t_{LZCE}$[19] | $\overline{CE}$ LOW to Low-Z[16] | 10 | | ns |
| $t_{HZCE}$[19] | $\overline{CE}$ HIGH to High-Z[16, 17] | | 25 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power-up | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power-down | | 85 | ns |
| $t_{DBE}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid | | 85 | ns |
| $t_{LZBE}$[19] | $\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z[16] | 5 | | ns |
| $t_{HZBE}$[19] | $\overline{BLE}$ / $\overline{BHE}$ HIGH to HIGH Z[16,17] | | 25 | ns |

**Notes:**

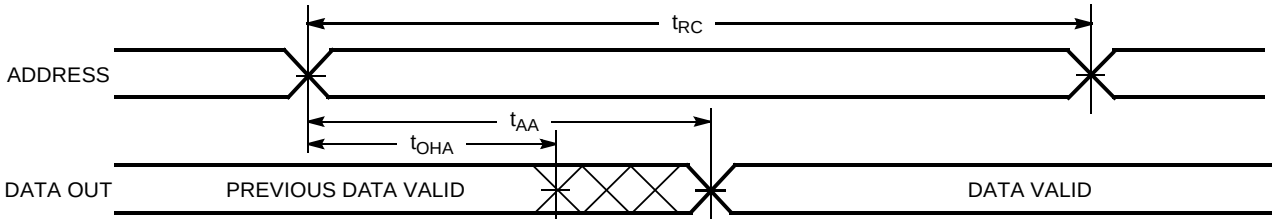
13. This mode does not retain the data in the SRAM. All data will be lost in the mode of operation. This is the default mode of operation on the CY81U016X16B7A device.
14. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signal (CE HIGH) or by disabling both $\overline{BHE}$ and $\overline{BLE}$ (both HIGH).
15. Test conditions assume signal transition time of 3ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
16. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, $t_{HZBE}$ is less than $t_{LZBE}$ and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
17. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedence state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
19. High-Z and Low-Z parameters are guaranteed by design and are not tested.

**Switching Characteristics** Over the Operating Range[15] (continued)

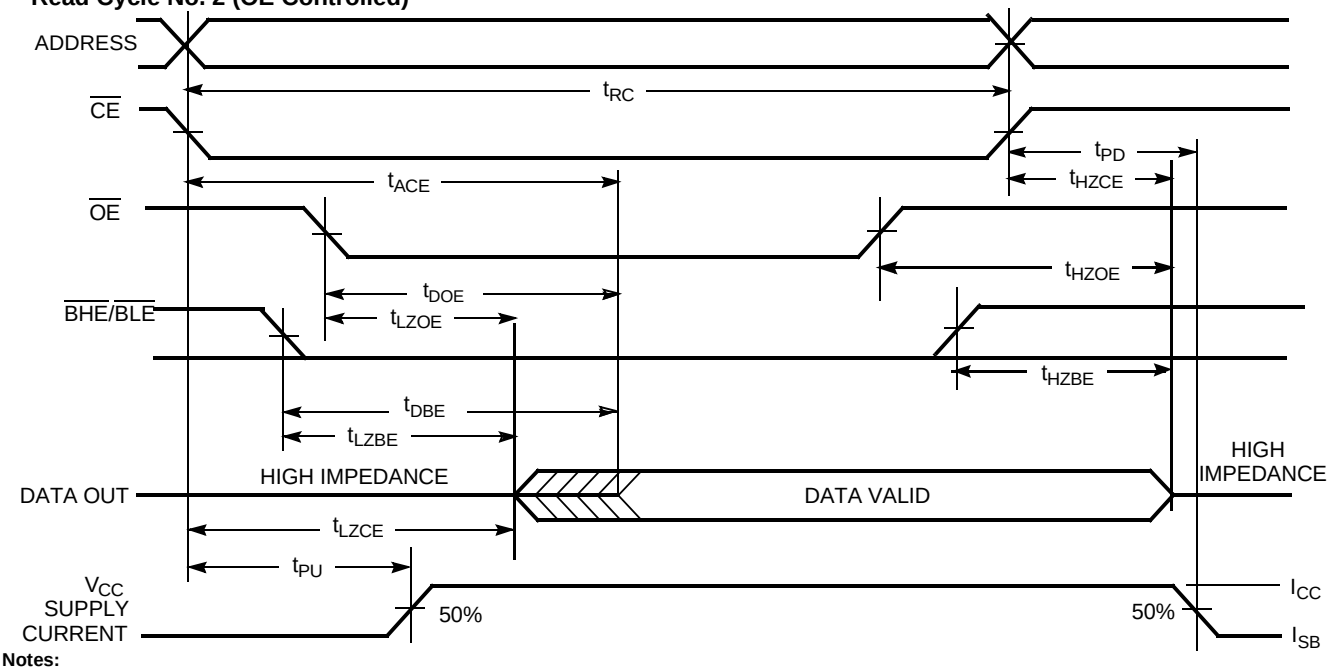
| Parameter | Description | 85 ns | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **Write Cycle**[18] | | | | |
| $t_{WC}$ | Write Cycle Time | 85 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 75 | | ns |
| $t_{AW}$ | Address Set-up to Write End | 75 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 65 | 1000 | ns |
| $t_{BW}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to Write End | 75 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 30 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | ns |
| $t_{HZWE}$[19] | $\overline{WE}$ LOW to High-Z[16, 17] | | 25 | ns |
| $t_{LZWE}$[19] | $\overline{WE}$ HIGH to Low-Z[16] | 10 | | ns |

## Switching Waveforms

**Read Cycle No. 1(Address Transition Controlled)** [20, 21]



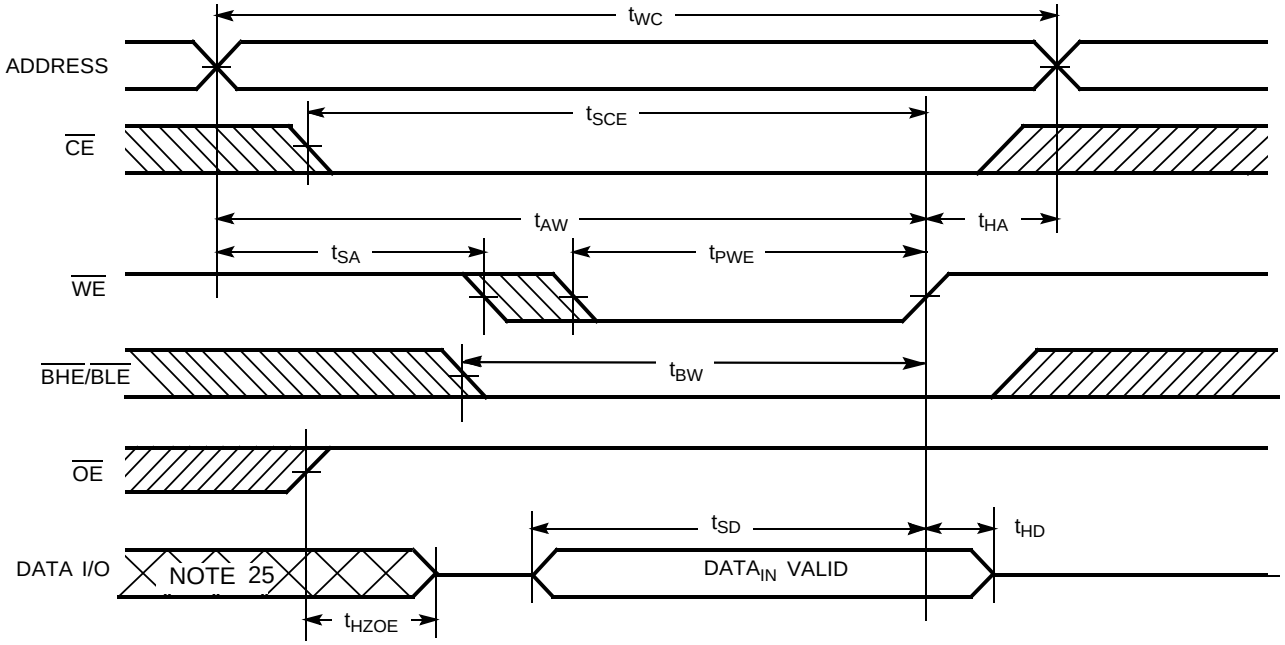

**Read Cycle No. 2 ($\overline{OE}$ Controlled)** [21, 22]



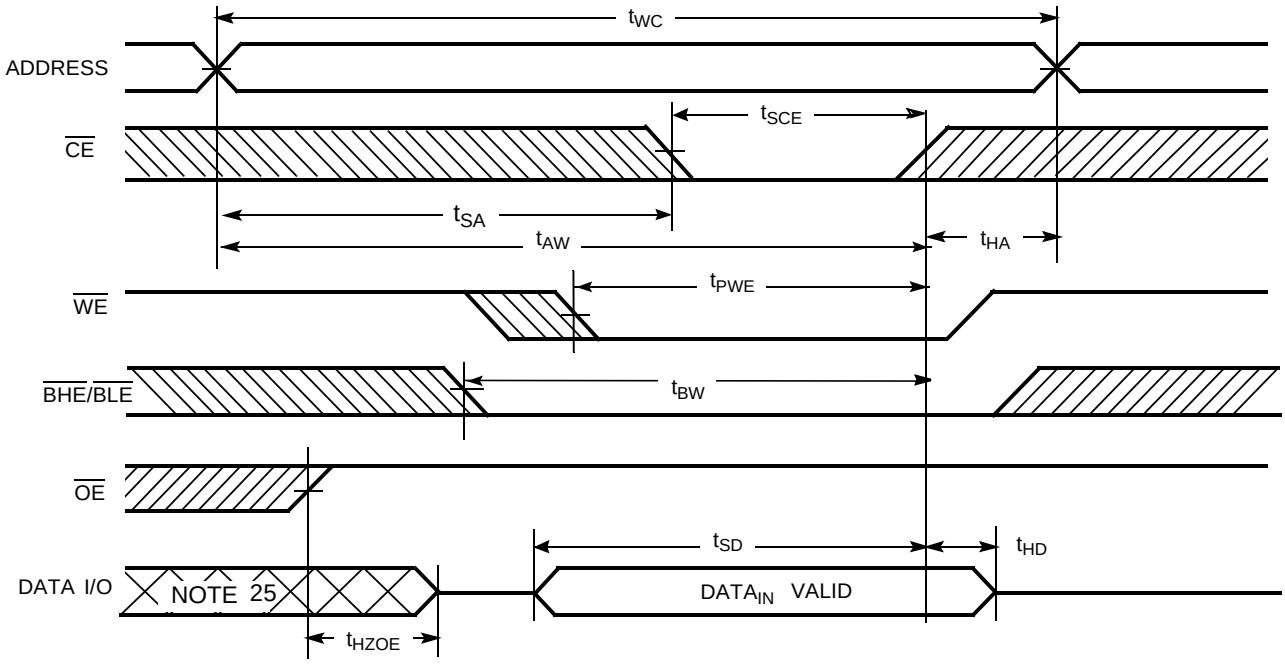

**Notes:**
20. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1(WE Controlled) [18, 23, 24]




### Write Cycle No. 2 (CE Controlled) [18, 23, 24]

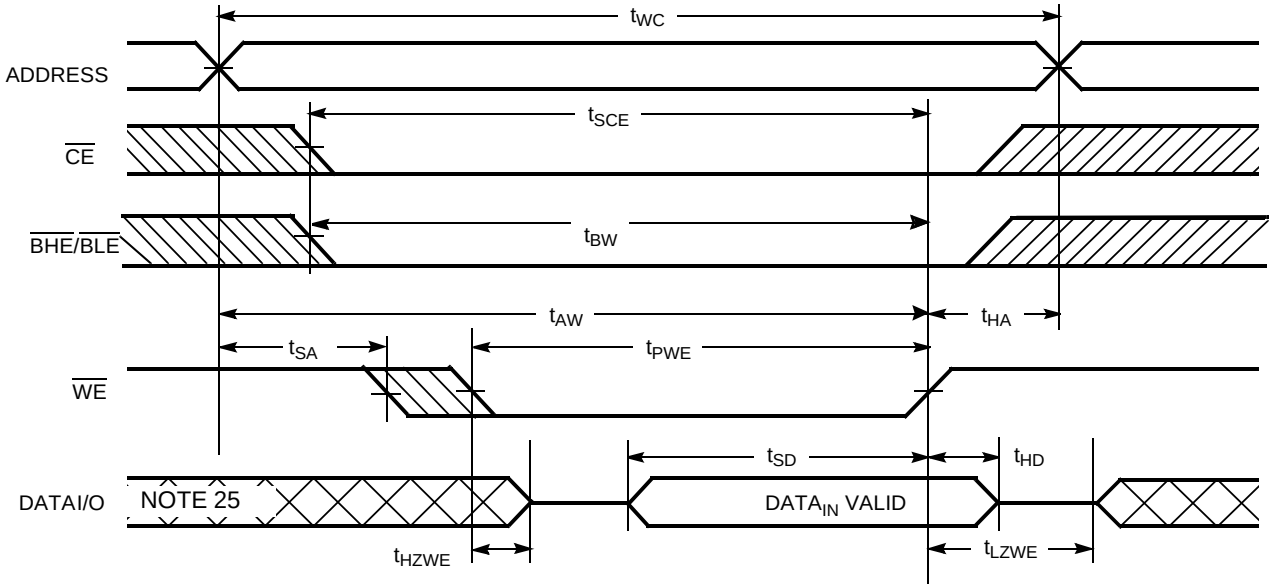



**Notes:**

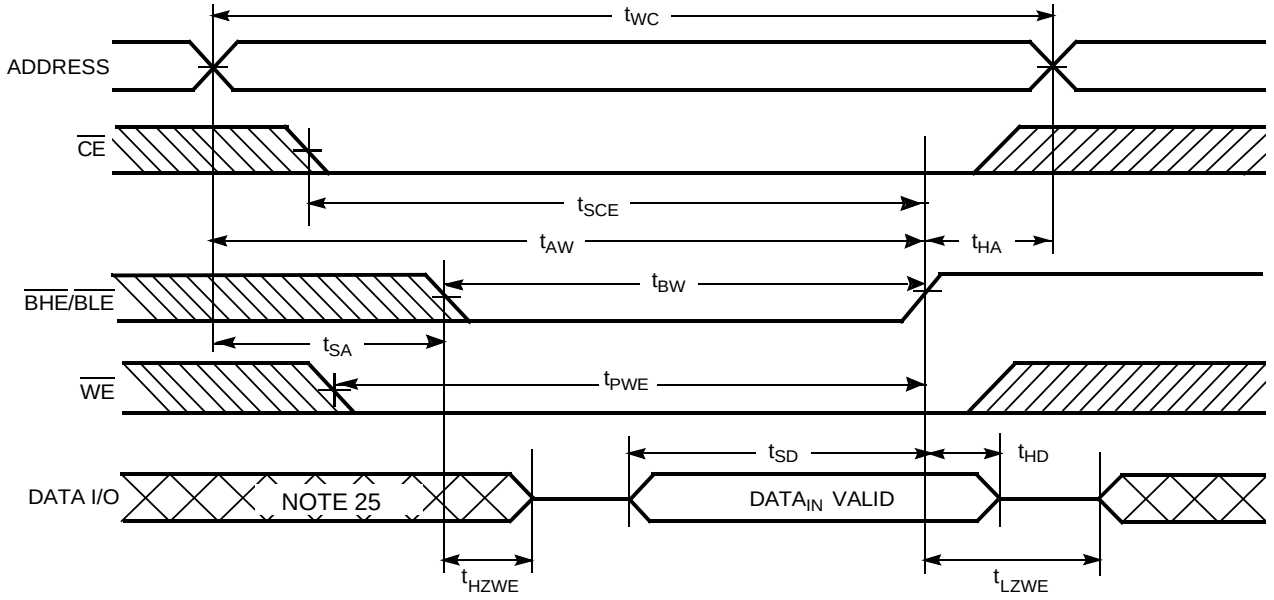
23. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
25. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

**Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)** [24]




**Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)** [24]




## Truth Table

| $\overline{CE}$ | $\overline{ZZ}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| X | H | X | X | H | H | High-Z | Deselect/Power-down | Standby ($I_{SB}$) |
| H | H | X | X | X | X | High-Z | Deselect/Power-down | Standby ($I_{SB}$) |
| X | L | X | X | X | X | High-Z | Deep Sleep Mode | Deep Sleep Current(Iccds)[26.] |
| L | H | H | L | L | L | Data Out (I/O0–I/O15) | Read | Active ($I_{CC}$) |
| L | H | H | L | H | L | Data Out (I/O0–I/O7); High-Z (I/O8–I/O15) | Read | Active ($I_{CC}$) |

## Truth Table (continued)

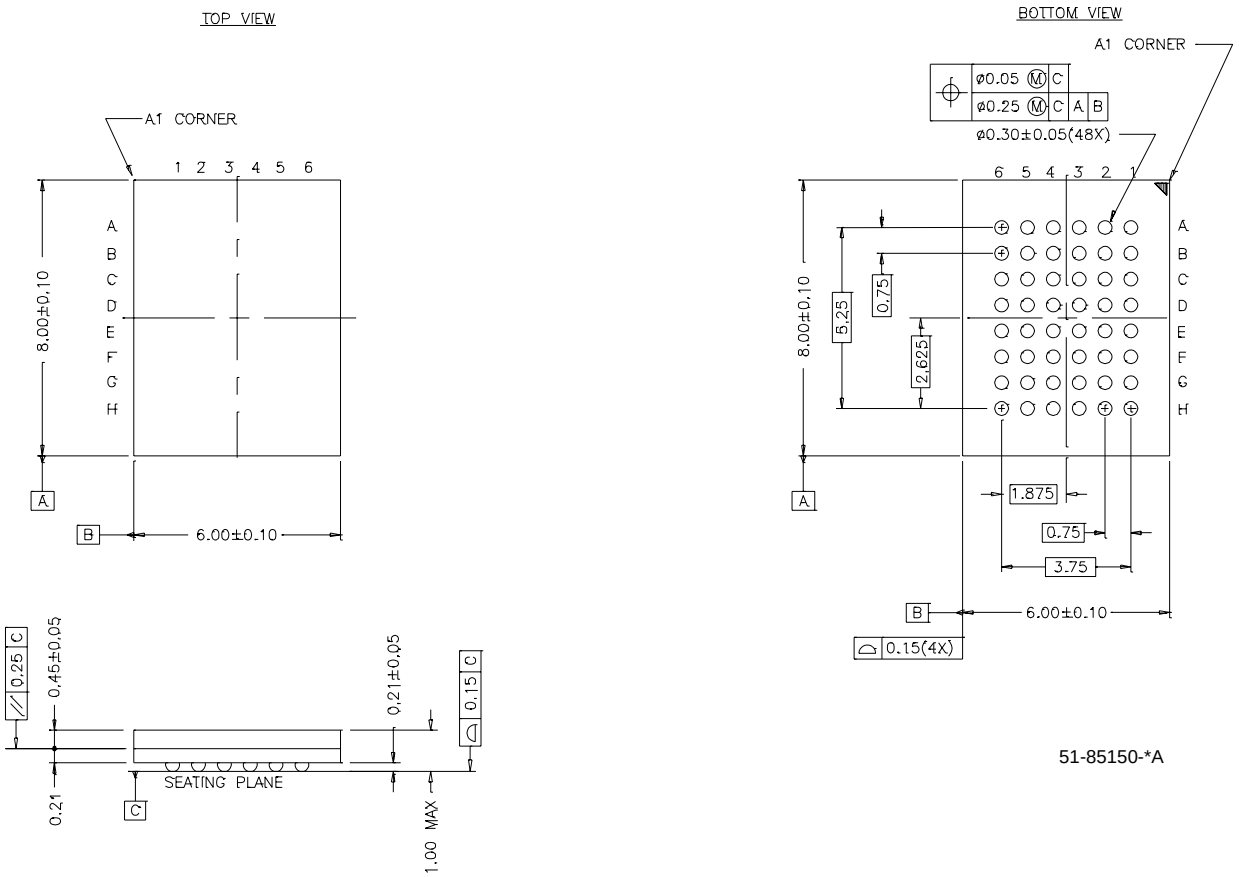
| $\overline{CE}$ | $\overline{ZZ}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| L | H | H | L | L | H | Data Out (I/O8–I/O15); High-Z (I/O0–I/O7) | Read | Active ($I_{CC}$) |
| L | H | X | H | L | L | High-Z | Output Disabled | Active ($I_{CC}$) |
| L | H | L | X | L | L | Data In (I/O0–I/O15) | Write | Active ($I_{CC}$) |
| L | H | L | X | H | L | Data In (I/O0–I/O7); High-Z (I/O8–I/O15) | Write | Active ($I_{CC}$) |
| L | H | L | X | L | H | Data In (I/O8–I/O15); High-Z (I/O0–I/O7) | Write | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 85 | CY81U016X16B7A-8N4FII | BV48A | 48-ball Fine Pitch BGA | Industrial |

## Package Diagram

**48-ball VFBGA (6 x 8 x 1 mm) BV48A**




**Note:**

26. This assumes that the deep sleep mode is enabled in the VAR register.

## Document History Page

| Document Title : CY81U016X16B7A MoBL3™ 16M (1M x 16) SRAM<br>Document Number : 38-05309 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 117415 | 09/12/02 | CDY | New Data Sheet |