



# CY74FCT16952T CY74FCT162952T CY74FCT162H952T

## 16-Bit Registered Transceivers

### Features

- Low power, pin-compatible replacement for ABT functions
- FCT-C speed at 6.3 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000 V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Extended commercial range of 40°C to 185°C
- $V_{CC} = 5V \pm 10\%$

### CY74FCT16952T Features:

- 64 mA sink current (Com'1), 32 mA source current (Com'1)
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5V, T_A = 25^\circ C$

### CY74FCT162952T Features:

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5V, T_A = 25^\circ C$
- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

### Functional Description

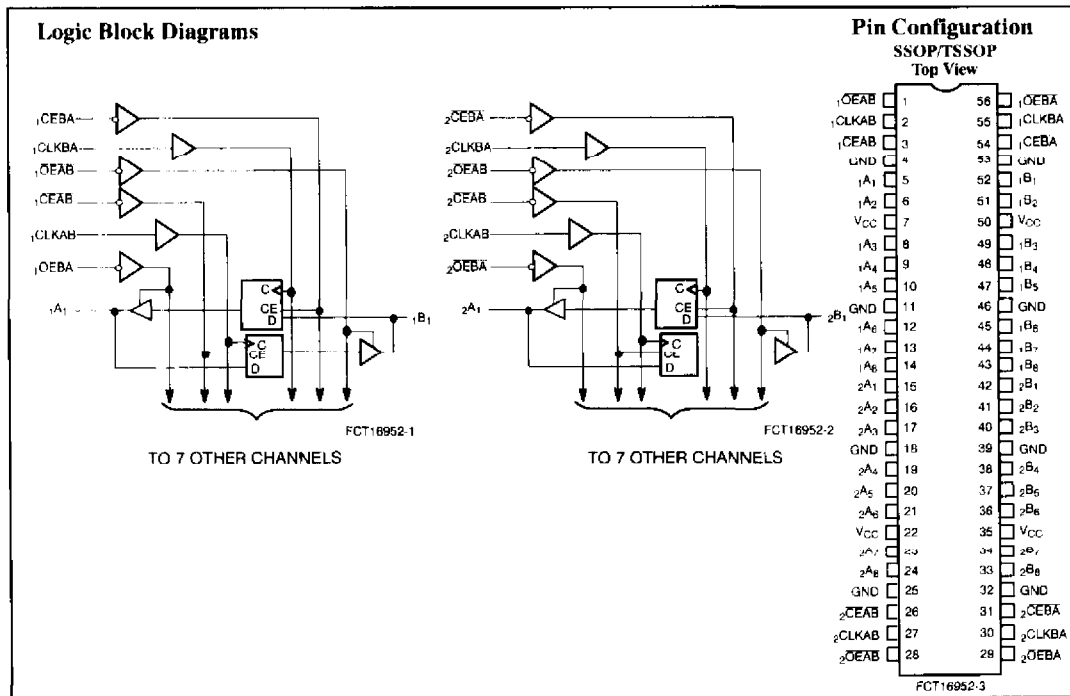
These 16-bit registered transceivers are high-speed, low-power devices. 16-bit operation is achieved by connecting the control lines of the two 8-bit registered transceivers together. For data flow from bus A-to-B,  $\overline{CEAB}$  must be LOW to allow data to be stored when CLKAB transitions from LOW-to-HIGH. The stored data will be present on the output when  $\overline{OEAB}$  is LOW. Control of data from B-to-A is similar and is controlled by

using the  $\overline{CEBA}$ , CLKBA, and  $\overline{OEBA}$  inputs. The output buffers are designed with a power-off disable feature to allow for live insertion of boards.

The CY74FCT16952T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162952T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162952T is ideal for driving transmission lines.

The CY74FCT162H952T is a 24-mA balanced output part that has "bus hold" on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.





Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[10]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>II</sub>	Input Hysteresis <sup>[7]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	Standard	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>		±1	μA
		Bus Hold			±100	
I <sub>IL</sub>	Input LOW Current	Standard	V <sub>CC</sub> =Max., V <sub>I</sub> =GND		±1	μA
		Bus Hold			±100	μA
I <sub>BBH</sub> I <sub>BBL</sub>	Bus Hold Sustain Current on Bus Hold Input <sup>[8]</sup>	V <sub>CC</sub> =Min.	V <sub>I</sub> =2.0V	-50		μA
			V <sub>I</sub> =0.8V	+50		
I <sub>BBHO</sub> I <sub>BHLO</sub>	Bus Hold Overdrive Current on Bus Hold Input <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>I</sub> =1.5V			TBD	mA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	μA
I <sub>OZI</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	μA
I <sub>OS</sub>	Short Circuit Current <sup>[9]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[9]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V			±1	μA

Output Drive Characteristics for CY74FCT16952T

Parameter	Description	Test Conditions	Min.	Typ. <sup>[10]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162952T, CY74FCT162H952T

Parameter	Description	Test Conditions	Min.	Typ. <sup>[10]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[9]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[9]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

Capacitance<sup>[7]</sup> (T<sub>A</sub> = +25 °C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ. <sup>[10]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

Notes:

7. This parameter is guaranteed but not tested.
8. Pins with bus hold are described in the Pin Description.
9. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect

operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

10. Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25 °C ambient.



**Power Supply Characteristics**

Parameter	Description	Test Conditions <sup>[11]</sup>	Typ. <sup>[10]</sup>	Max.	Unit	
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$	5	500	$\mu A$
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}$	$V_{IN} = 3.4V$ <sup>[12]</sup>	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>[13]</sup>	$V_{CC} = \text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEAB}$ or $\overline{OEBA} = \text{GND}$	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	75	120	$\mu A/$ MHz
$I_C$	Total Power Supply Current <sup>[14]</sup>	$V_{CC} = \text{Max.}$ , $F_1 = 5 \text{ MHz}$ , $F_0 = 10 \text{ MHz (CLKAB)}$ $\overline{OEAB} = \overline{CEAB} = \text{GND}$ $\overline{OEBA} = V_{CC}$ , 50% Duty Cycle, Outputs Open, One Bit Toggling	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	0.8	1.7	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	1.3	3.2	
		$V_{CC} = \text{Max.}$ , $F_0 = 10 \text{ MHz (CLKAB)}$ $f_1 = 2.5 \text{ MHz}$ , $\overline{OEAB} = \overline{CEAB} = \text{GND}$ $\overline{OEBA} = V_{CC}$ , 50% Duty Cycle, Outputs Open, Sixteen Bit Toggling	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	3.8	6.5 <sup>[15]</sup>	
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	8.3	20.0 <sup>[15]</sup>	

**Notes:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} (D_H N_T) + I_{CCD} (f_0/2 + f_1 N_T)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN} = 3.4V$ )

- $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_T$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
15. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.



**CY74FCT16952T**  
**CY74FCT162952T**  
**CY74FCT162H952T**

**Ordering Information CY74FCT16952**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.3	CY74FCT16952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT16952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT16952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT16952ATPVC	O56	56-Lead (300-Mil) SSOP	

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	CY74FCT162952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162952ATPVC	O56	56-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT162H952**

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6.3	CY74FCT162H952CTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952CTPVC	O56	56-Lead (300-Mil) SSOP	
7.5	CY74FCT162H952BTPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952BTPVC	O56	56-Lead (300-Mil) SSOP	
10.0	CY74FCT162H952ATPAC	Z56	56-Lead (240-Mil) TSSOP	Commercial
	CY74FCT162H952ATPVC	O56	56-Lead (300-Mil) SSOP	

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