

Features

- Very high speed
 - 55 ns
- Wide voltage range
 - 2.2 V to 3.7 V
- Ultra low standby power
 - Typical standby current: 8 μ A
 - Maximum standby current: 48 μ A
- Ultra low active power
 - Typical active current: 7.5 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 48-ball FBGA package

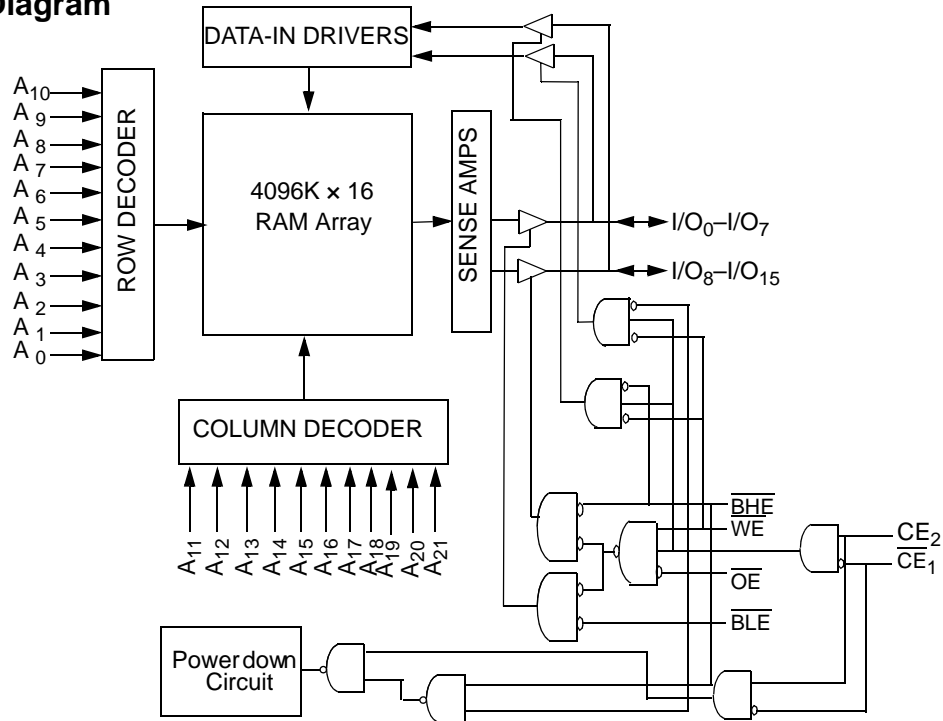
Functional Description

The CY62187EV30 is a high performance CMOS static RAM organized as 4 M words by 16-bits. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both \overline{BHE} and \overline{BLE} are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when: deselected (\overline{CE}_1 HIGH or CE_2 LOW), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH and \overline{WE} LOW).

To write to the device, take Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{21}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{21}).

To read from the device, take Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the [Truth Table](#) on page 9 for a complete description of read and write modes.

Logic Block Diagram

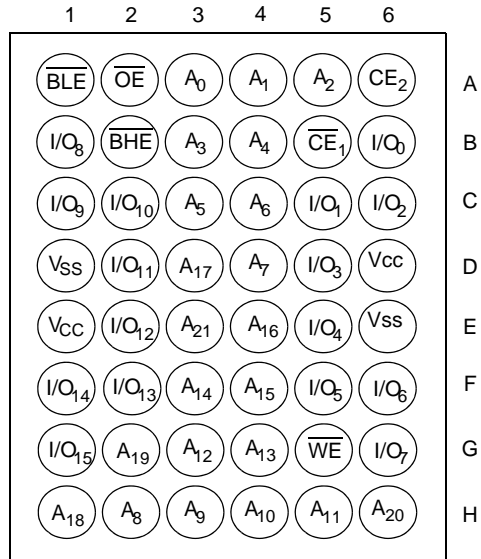


Contents

| | | | |
|---|-----------|--|-----------|
| Pin Configuration | 4 | Ordering Information | 12 |
| Product Portfolio | 4 | Ordering Code Definitions | 12 |
| Maximum Ratings | 5 | Package Diagram | 13 |
| Operating Range | 5 | Acronyms | 13 |
| Electrical Characteristics | 5 | Document Conventions | 13 |
| Capacitance | 5 | Units of Measure | 13 |
| Thermal Resistance | 6 | Document History Page | 14 |
| Data Retention Characteristics | 6 | Sales, Solutions, and Legal Information | 15 |
| Switching Characteristics | 7 | Worldwide Sales and Design Support | 15 |
| Switching Waveforms | 8 | Products | 15 |
| Truth Table | 11 | PSoC Solutions | 15 |

Pin Configuration

Figure 1. 48-ball FBGA



Product Portfolio

| Product | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---------------|---------------------------|-----|--------------------|------------|--------------------------------|-----|----------------------|-----|-------------------------------|----|
| | | | | | Operating I _{CC} (mA) | | | | Standby I _{SB2} (μA) | |
| | | | | | f = 1 MHz | | f = f _{Max} | | | |
| Min | Typ ^[1] | Max | Typ ^[1] | Max | Typ ^[1] | Max | Typ ^[1] | Max | | |
| CY62187EV30LL | 2.2 | 3.0 | 3.7 | 55 | 7.5 | 9 | 45 | 55 | 8 | 48 |

Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| | |
|---|---------------------------------|
| Storage Temperature | -65 °C to +150 °C |
| Ambient Temperature with Power Applied | -55 °C to +125 °C |
| Supply Voltage to Ground Potential..... | -0.3 V to $V_{CC(max)}$ + 0.3 V |
| DC Voltage Applied to Outputs in High Z State ^[2, 3] | -0.3 V to $V_{CC(max)}$ + 0.3 V |

| | |
|--|---|
| DC Input Voltage ^[2, 3] | -0.3 V to $V_{CC(max)}$ + 0.3 V |
| Output Current into Outputs (LOW) | 20 mA |
| Static Discharge Voltage..... | > 2001 V (per MIL-STD-883, Method 3015) |
| Latch Up Current | > 200 mA |

Operating Range

| Device | Range | Ambient Temperature | V_{CC} ^[4] |
|---------------|------------|---------------------|-------------------------|
| CY62187EV30LL | Industrial | -40 °C to +85 °C | 2.2 V to 3.7 V |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 55 ns | | | Unit |
|--------------------------|---|---|-------|--------------------|--------------------|---------|
| | | | Min | Typ ^[5] | Max | |
| V_{OH} | Output HIGH voltage | $2.2 V \leq V_{CC} \leq 2.7 V$ $I_{OH} = -0.1 mA$ | 2.0 | - | - | V |
| | | $2.7 V \leq V_{CC} \leq 3.7 V$ $I_{OH} = -1.0 mA$ | 2.4 | - | - | V |
| V_{OL} | Output LOW voltage | $2.2 V \leq V_{CC} \leq 2.7 V$ $I_{OL} = 0.1 mA$ | - | - | 0.4 | V |
| | | $2.7 V \leq V_{CC} \leq 3.7 V$ $I_{OL} = 2.1 mA$ | - | - | 0.4 | V |
| V_{IH} | Input HIGH voltage | $2.2 V \leq V_{CC} \leq 2.7 V$ | 1.8 | - | $V_{CC} + 0.3 V$ | V |
| | | $2.7 V \leq V_{CC} \leq 3.7 V$ | 2.2 | - | $V_{CC} + 0.3 V$ | V |
| V_{IL} | Input LOW voltage | $2.2 V \leq V_{CC} \leq 2.7 V$ | -0.3 | - | 0.6 | V |
| | | $2.7 V \leq V_{CC} \leq 3.7 V$ | -0.3 | - | 0.8 ^[6] | V |
| I_{IX} | Input leakage current | $GND \leq V_I \leq V_{CC}$ | -1 | - | +1 | μA |
| I_{OZ} | Output leakage current | $GND \leq V_O \leq V_{CC}$, output disabled | -1 | - | +1 | μA |
| I_{CC} | V_{CC} operating supply current | $f = f_{Max} = 1/t_{RC}$ $V_{CC} = V_{CC(max)}$ | - | 45 | 55 | mA |
| | | $f = 1 MHz$ $I_{OUT} = 0 mA$ CMOS levels | - | 7.5 | 9 | mA |
| I_{SB2} ^[7] | Automatic CE power down current—CMOS inputs | $CE_1 \geq V_{CC} - 0.2 V$ or $CE_2 \leq 0.2 V$ or (BHE and BLE) $\geq V_{CC} - 0.2 V$, $V_{IN} \geq V_{CC} - 0.2 V$ or $V_{IN} \leq 0.2 V$, $f = 0$, $V_{CC} = 3.7 V$ | - | 8 | 48 | μA |

Capacitance

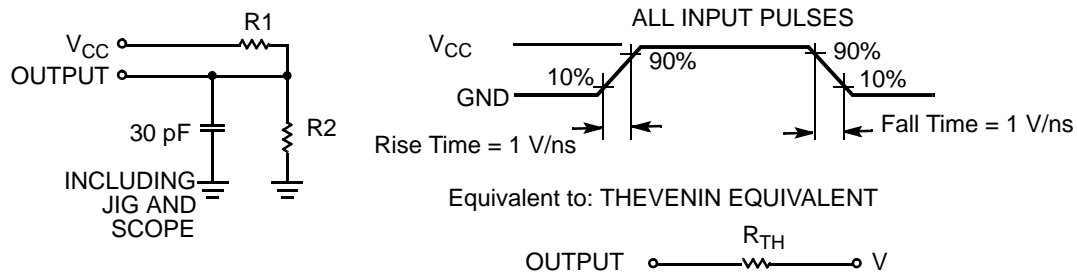
| Parameter ^[8] | Description | Test Conditions | Max | Unit |
|--------------------------|--------------------|--|-----|------|
| C_{IN} | Input capacitance | $T_A = 25 °C$, $f = 1 MHz$, $V_{CC} = V_{CC(typ)}$ | 25 | pF |
| C_{OUT} | Output capacitance | | 35 | pF |

Notes

- $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75V$ for pulse durations less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to V_{CC} (min) and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25 °C$.
- Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions input LOW Voltage applied to the device must not be higher than 0.7 V.
- Chip enables (CE_1 and CE_2) and Byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance

| Parameter ^[9] | Description | Test Conditions | FBGA | Unit |
|--------------------------|--|--|-------|------|
| θ_{JA} | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 x 4.5 inch, 2-layer printed circuit board | 59.06 | °C/W |
| θ_{JC} | Thermal resistance (junction to case) | | 14.08 | °C/W |

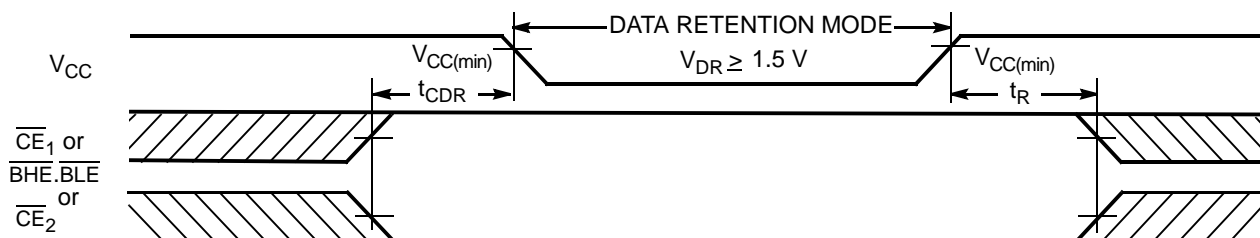
Figure 2. AC Test Loads and Waveforms

Table 1. AC Test Loads

| Parameter | 2.5 V | 3.3 V | Unit |
|-----------|-------|-------|----------|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| R_{TH} | 8000 | 645 | Ω |
| V_{TH} | 1.20 | 1.75 | V |

Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[10] | Max | Unit |
|----------------------------|--------------------------------------|---|-----|---------------------|-----|---------|
| V_{DR} | V_{CC} for data retention | | 1.5 | – | – | V |
| I_{CCDR} ^[11] | Data retention current | $V_{CC} = 1.5$ V, $CE_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or (BHE and BLE) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | – | 48 | μ A |
| t_{CDR} ^[9] | Chip deselect to data retention time | | 0 | – | – | ns |
| t_R ^[12] | Operation recovery time | | 55 | – | – | ns |

Figure 3. Data Retention Waveform^[13]


Notes

9. Tested initially and after any design or process changes that may affect these parameters.
10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
11. Chip enables (CE_1 and CE_2) and Byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ μ s or stable at $V_{CC(min)} \geq 100$ μ s.
13. BHE.BLE is the AND of both BHE and BLE. Chip is deselected by either disabling the chip enable signals or by disabling both BHE and BLE.

Switching Characteristics

Over the Operating Range

| Parameter ^[14] | Description | 55 ns | | Unit |
|-----------------------------------|---|-------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t_{RC} | Read cycle time | 55 | – | ns |
| t_{AA} | Address to data valid | – | 55 | ns |
| t_{OHA} | Data hold from address change | 6 | – | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to data valid | – | 55 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 25 | ns |
| t_{LZOE} | \overline{OE} LOW to LOW Z ^[15] | 5 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to high Z ^[15, 16] | – | 20 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to low Z ^[15] | 10 | – | ns |
| t_{HZCE} | \overline{CE}_1 HIGH and CE_2 LOW to high Z ^[15, 16] | – | 20 | ns |
| t_{PU} | \overline{CE}_1 LOW and CE_2 HIGH to power up | 0 | – | ns |
| t_{PD} | CE_1 HIGH and CE_2 LOW to power down | – | 55 | ns |
| t_{DBE} | $\overline{BLE}/\overline{BHE}$ LOW to data valid | – | 55 | ns |
| t_{LZBE} | $\overline{BLE}/\overline{BHE}$ LOW to low Z ^[15] | 10 | – | ns |
| t_{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to high Z ^[15, 16] | – | 20 | ns |
| Write Cycle^[17] | | | | |
| t_{WC} | Write cycle time | 55 | – | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to write end | 45 | – | ns |
| t_{AW} | Address setup to write end | 45 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 40 | – | ns |
| t_{BW} | $\overline{BLE}/\overline{BHE}$ LOW to write end | 45 | – | ns |
| t_{SD} | Data setup to write end | 25 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to high Z ^[15, 16] | – | 20 | ns |
| t_{LZWE} | \overline{WE} HIGH to low Z ^[15] | 10 | – | ns |

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V_{TH} , input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Table 1 on page 6.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal Write time of the memory is defined by the overlap of \overline{WE} , $CE_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled)^[18, 19]

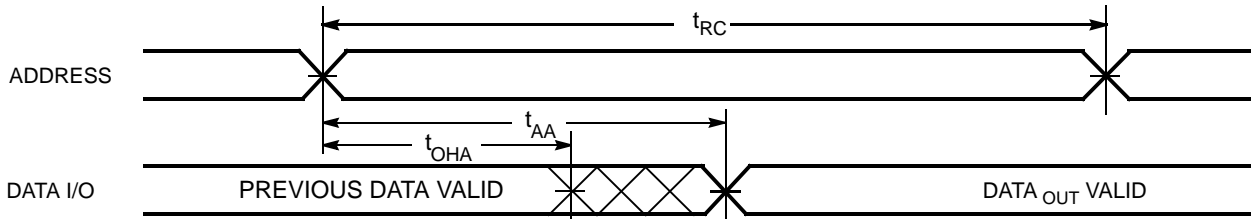
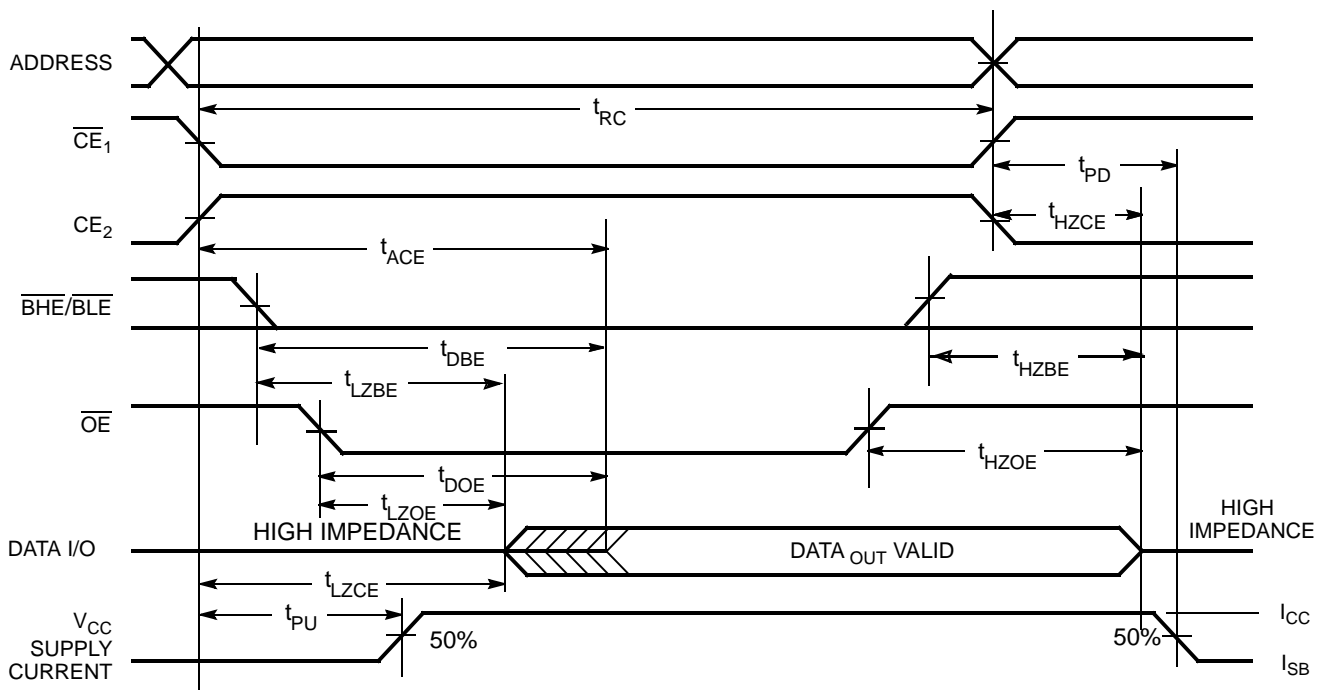


Figure 5. Read Cycle 2 (\overline{OE} Controlled)^[19, 20]



Notes

18. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.

19. WE is HIGH for read cycle.

20. Address valid prior to or coincident with \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle 1 (\overline{WE} Controlled) [21, 22, 23, 24]

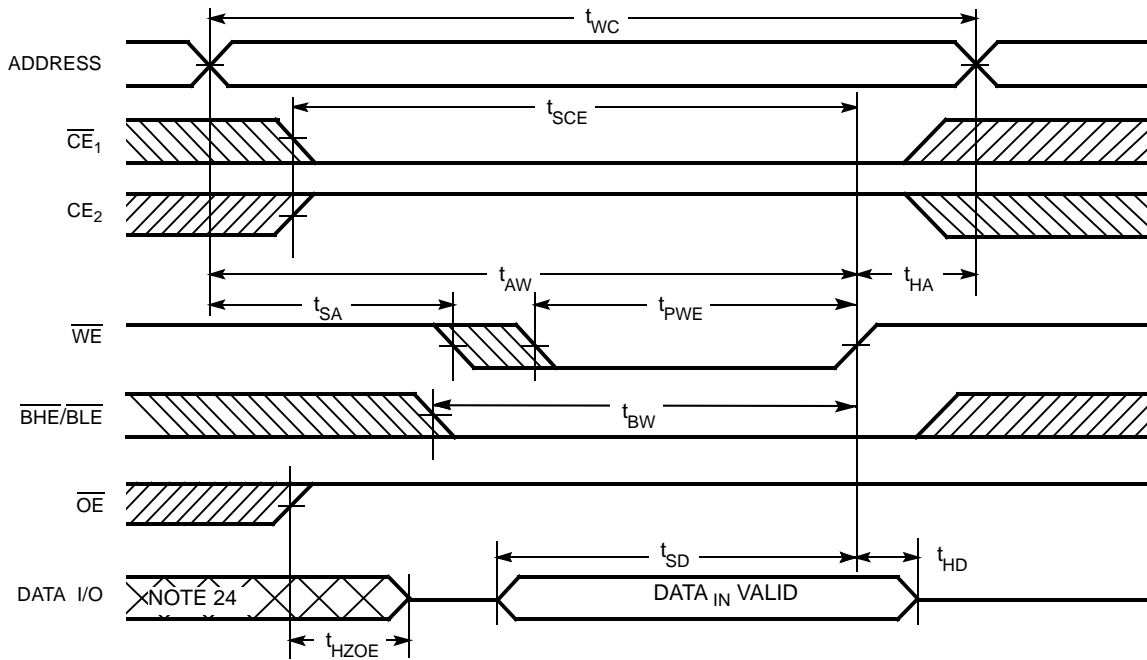
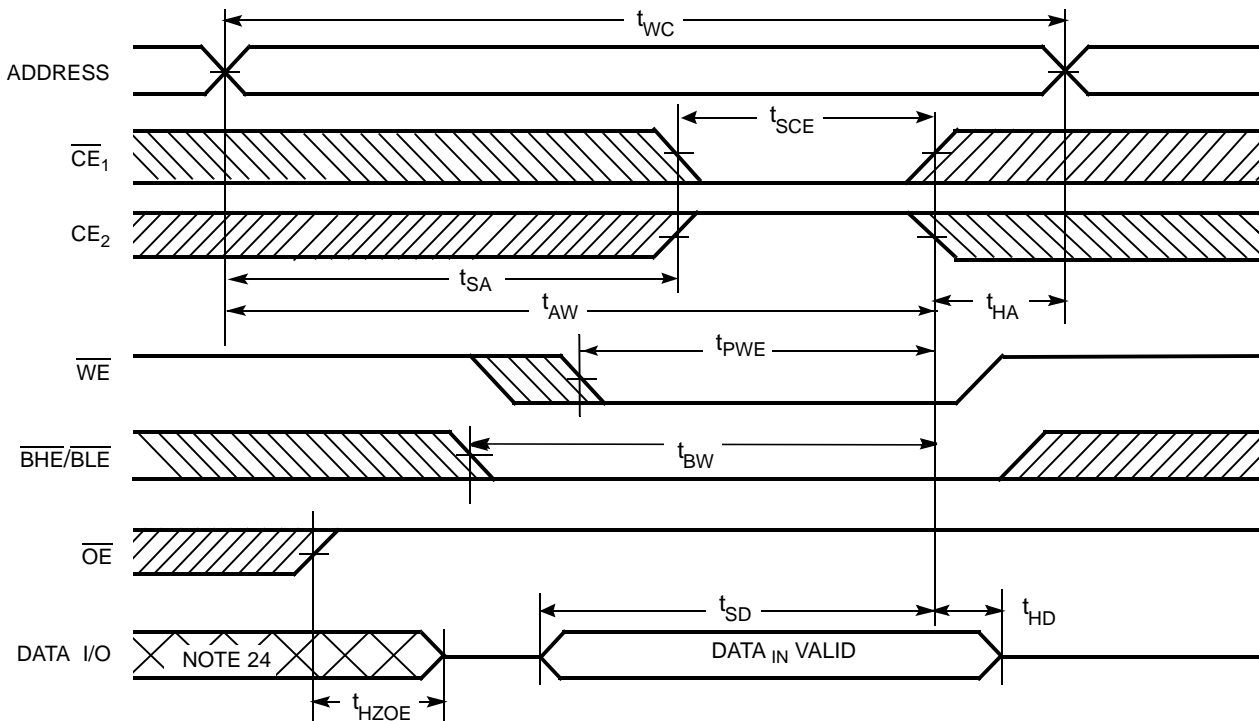


Figure 7. Write Cycle 2 (\overline{CE}_1 or \overline{CE}_2 Controlled) [21, 22, 23, 24]



Notes

- 21. The internal Write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$, and $\overline{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 23. If \overline{CE}_1 goes HIGH and \overline{CE}_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 24. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[25, 26]

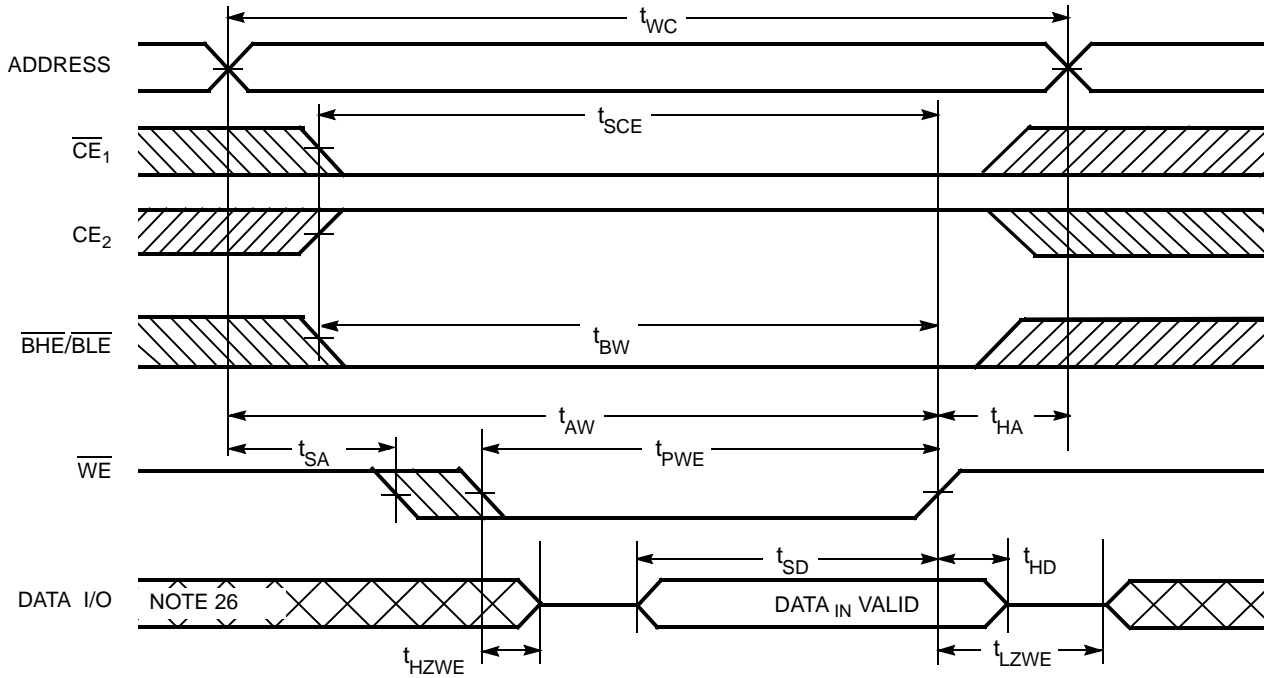
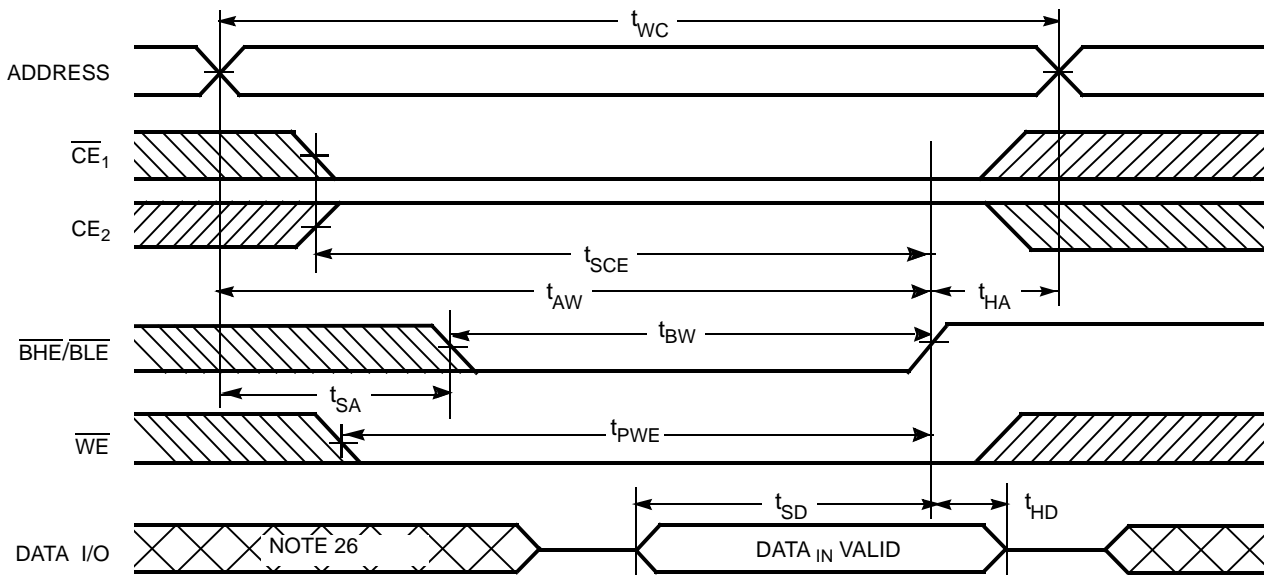


Figure 9. Write Cycle 4 ($\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[25,26]



Notes

- 25. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
- 26. During this period the I/Os are in output state and input signals should not be applied.

Truth Table

| \overline{CE}_1 | \overline{CE}_2 | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs Outputs | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|-------------------|-------------------|--|---------------------|----------------------------|
| H | X ^[27] | X | X | X ^[27] | X ^[27] | High Z | Deselect/Power Down | Standby (I _{SB}) |
| X ^[27] | L | X | X | X ^[27] | X ^[27] | High Z | Deselect/Power Down | Standby (I _{SB}) |
| X ^[27] | X ^[27] | X | X | H | H | High Z | Deselect/Power Down | Standby (I _{SB}) |
| L | H | H | L | L | L | Data Out (I/O ₀ –I/O ₁₅) | Read | Active (I _{CC}) |
| L | H | H | L | H | L | High Z (I/O ₈ –I/O ₁₅); Data Out (I/O ₀ –I/O ₇) | Read | Active (I _{CC}) |
| L | H | H | L | L | H | Data Out (I/O ₈ –I/O ₁₅); High Z (I/O ₀ –I/O ₇) | Read | Active (I _{CC}) |
| L | H | L | X | L | L | Data In (I/O ₀ –I/O ₁₅) | Write | Active (I _{CC}) |
| L | H | L | X | H | L | High Z (I/O ₈ –I/O ₁₅); Data In (I/O ₀ –I/O ₇) | Write | Active (I _{CC}) |
| L | H | L | X | L | H | Data In (I/O ₈ –I/O ₁₅); High Z (I/O ₀ –I/O ₇) | Write | Active (I _{CC}) |
| L | H | H | H | L | H | High Z | Output Disabled | Active (I _{CC}) |
| L | H | H | H | H | L | High Z | Output Disabled | Active (I _{CC}) |
| L | H | H | H | L | L | High Z | Output Disabled | Active (I _{CC}) |

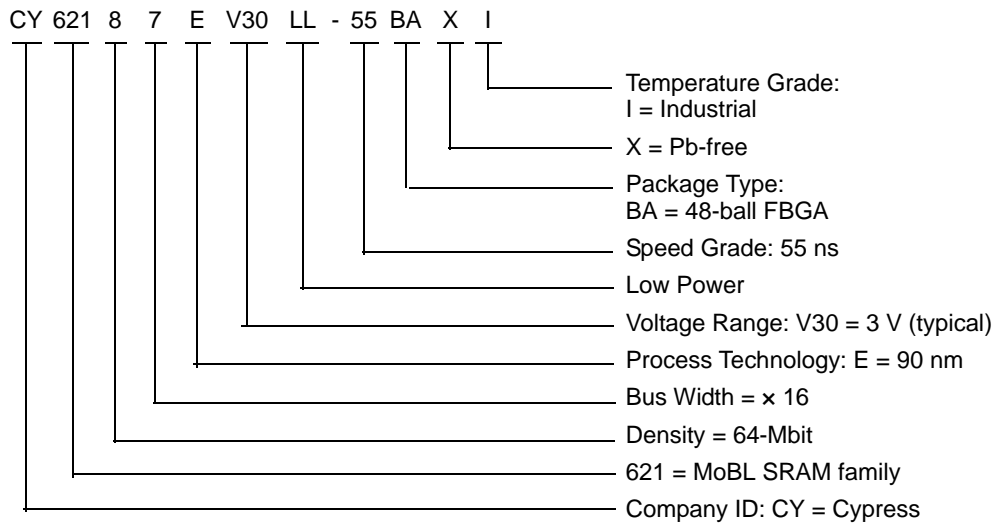
Note

27. The 'X' (Don't care) state for the chip enables and byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

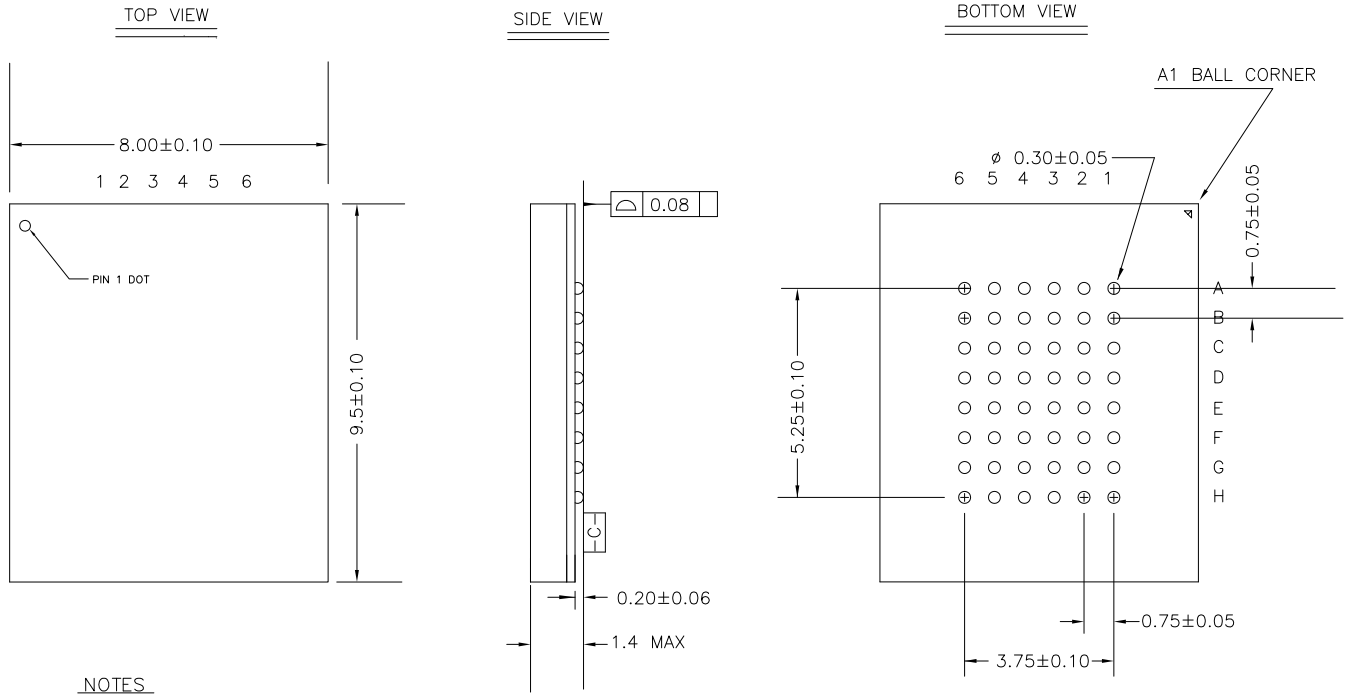
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|----------------------|-----------------|---|-----------------|
| 55 | CY62187EV30LL-55BAXI | 001-50044 | 48-ball fine pitch ball grid array (8 x 9.5 x 1.4 mm) Pb-free | Industrial |

Ordering Code Definitions



Package Diagram

Figure 10. 48-ball FBGA (8 × 9.5 × 1.4 mm)



NOTES

1. REFERENCE JEDEC # MO-205
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-50044 *D

Acronyms

| Acronym | Description |
|-------------------------|---|
| $\overline{\text{BHE}}$ | byte high enable |
| $\overline{\text{BLE}}$ | byte low enable |
| CMOS | complementary metal oxide semiconductor |
| $\overline{\text{CE}}$ | chip enable |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SRAM | static random access memory |
| FBGA | fine-pitch ball grid array |
| $\overline{\text{WE}}$ | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | mega hertz |
| μA | microampere |
| mA | milliampere |
| ms | millisecond |
| ns | nanosecond |
| Ω | ohms |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY62187EV30 MoBL [®] 64-Mbit (4 M x 16) Static RAM | | | | |
|---|---------|-----------------|-----------------|--|
| Document Number: 001-48998 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 2595932 | VKN/PYRS | 10/24/08 | New Datasheet |
| *A | 2644442 | VKN/PYRS | 01/23/09 | Updated the Package diagram on page 10 |
| *B | 2672650 | VKN/PYRS | 03/12/09 | Extended the V_{CC} range to 3.7V Added 55 ns speed bin and it's related information Changed $I_{CC(typ)}$ from 2.5 mA to 3.5 mA at $f = 1$ MHz Changed $I_{CC(max)}$ from 4 mA to 6 mA at $f = 1$ MHz For 70 ns speed, changed $I_{CC(typ)}$ form 33 mA to 28 mA at $f = f_{MAX}$ For 70 ns speed, changed $I_{CC(max)}$ from 40 mA to 45 mA at $f = f_{MAX}$ For 70 ns speed, changed t_{PWE} from 45 to 50 ns, t_{SD} from 30 to 35 ns Modified footnote #6 Changed 48-Ball FBGA package dimensions from 8 x 9.5 x 1.6 mm to 8 x 9.5 x 1.4 mm and updated package diagram on page 10 |
| *C | 2737164 | VKN/AESA | 07/13/09 | Converted from preliminary to final Changed $I_{CC(typ)}$ from 3.5 mA to 4 mA at $f = 1$ MHz Changed $I_{CC(typ)}$ from 35 mA to 45 mA and from 28 mA to 35 mA for the speeds 50 ns and 70 ns respectively at $f = f_{max}$ Included V_{CC} range in the test condition of the "Electrical Characteristics" table for the specs V_{OH} , V_{OL} , V_{IH} , V_{IL} Changed $V_{IL(max)}$ from 0.8V to 0.7V for $V_{CC} = 2.7V$ to 3.7V Changed C_{IN} spec from 20 pF to 25 pF and C_{OUT} spec from 20 pF to 35 pF Included thermal specs for 48-FBGA Included V_{CC} range for V_{TH} spec in the AC test load table Changed t_{LZBE} spec from 5 ns to 10 ns Added footnote #20 related to chip enable |
| *D | 2765892 | VKN | 09/18/09 | Removed 70 ns speed For 55 ns speed, at $f = 1$ MHz, changed $I_{CC(max)}$ spec from 6 mA to 9 mA Changed $I_{CC(typ)}$ from 4 mA to 7.5 mA at $f = 1$ MHz |
| *E | 3177000 | AJU | 02/18/2011 | Updated Features (Corrected $I_{CC(typ)}$ from 4 mA to 7.5 mA). Updated Pin Configuration (Renamed Figure 1 as "48-ball FBGA"). Updated Product Portfolio (Corrected $I_{CC(typ)}$ from 4 mA to 7.5 mA). Updated Electrical Characteristics (Included \overline{BHE} and \overline{BLE} in I_{SB2} test conditions to reflect Byte power down feature). Updated Table 1 on page 6 (AC Test Loads). Updated Data Retention Characteristics (Included \overline{BHE} and \overline{BLE} in I_{CCDR} test conditions to reflect Byte power down feature, corrected $t_{R(min)}$ from t_{RC} to 55 ns). Added Ordering Code Definitions . Updated Package Diagram . Added Acronyms and Units of Measure . Changed all instances of IO to I/O. Updated in new template. |
| *F | 3282088 | RAME | 06/14/2011 | Updated template as per current Cypress standards. Removed reference to AN1064 SRAM system guidelines. Changed the V_{IL} parameter max value to 0.8 V for test condition $2.7 V \leq V_{CC} \leq 3.7 V$ and referenced to footnote # 6. |
| *G | 3785005 | TAVA | 10/18/2012 | Minor Text Modifications. Updated Package Diagram (from Rev *C to *D). |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at www.cypress.com/sales.

Products

| | |
|--------------------------|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2008-2012. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.