SONY

SP10T Antenna Switch Module 6TRx/2Tx/2Rx

CXM3582UR

Description

The CXM3582UR is a SP10T antenna switch module for GSM/UMTS/CDMA/LTE multi-mode handset.
The CXM3582UR has a built-in dual low pass filter and a +1.8 V CMOS compatible decoder.

The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.
The device has low BOM with no DC blocking capacitor.

(Applications: GSM/UMTS/CDMA/LTE multi-mode handsets)

Features

- Low insertion loss: 0.45 dB (Typ.) TRx (Cellular band)
  0.60 dB (Typ.) TRx (IMT Tx band)
- High linearity: IIP3 = 68 dBm
- Battery direct operation: V_{DD} = 2.5 V to 5.0 V
- No DC blocking capacitors except sourcing DC bias
- Small package size: 26-pin UQFN (2.6 mm x 3.4 mm x 0.625 mm Max.)
- Lead-free and RoHS compliant

Structure

GaAs junction gate pHEMT (JPHEMT) MMIC switch, CMOS decoder

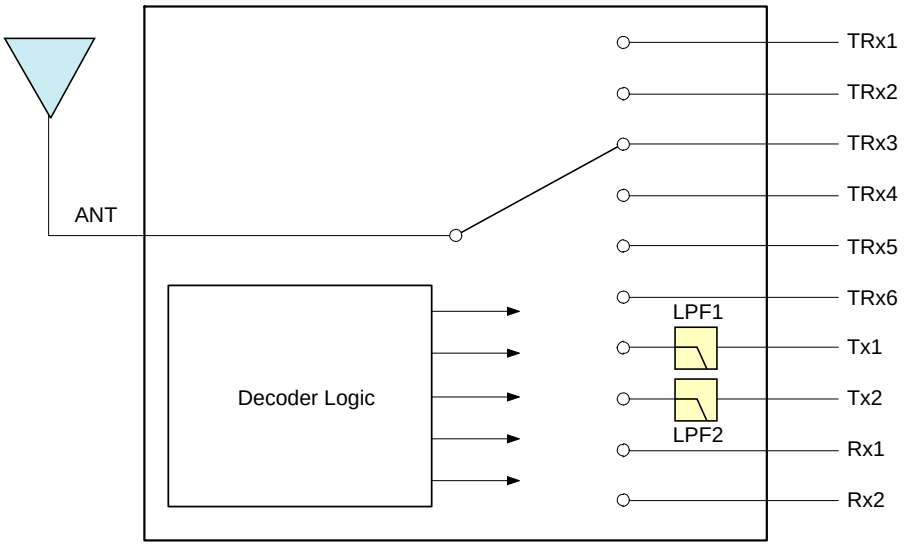
Absolute Maximum Ratings

- Bias voltage V_{DD} 6 V (Ta = 25 °C)
- Control voltage V_{CTL} 4 V (Ta = 25 °C)
- Input power max. [Tx1] 36 dBm (Duty cycle = 12.5 % to 50 %) (Ta = 25 °C)
- Input power max. [Tx2] 34 dBm (Duty cycle = 12.5 % to 50 %) (Ta = 25 °C)
- Input power max. [TRx] 32 dBm (Ta = 25 °C)
- Input power max. [Rx] 13 dBm (Ta = 25 °C)
- Operating temperature –35 to +90 °C
- Storage temperature –65 to +150 °C

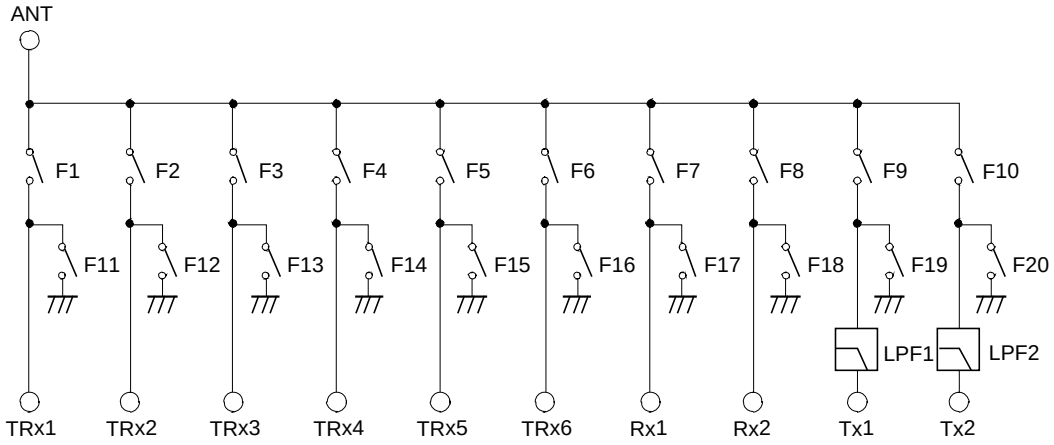
GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

E11907C26

Block Diagram of SP10T Antenna Switch Module



Block Diagram of SP10T 6TRx/2Tx/2Rx



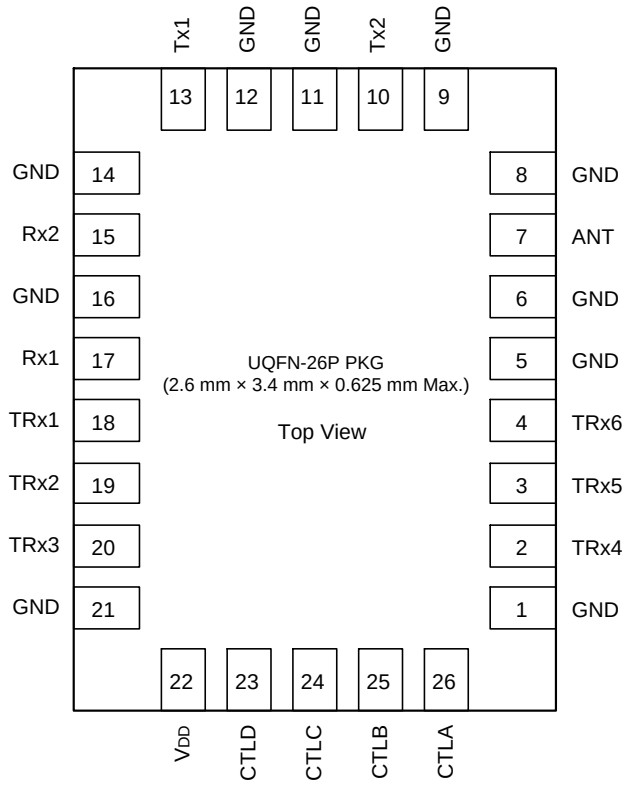
Truth Table

State	Active path	CTL state				SW state (*1)																		
		CTLA	CTLB	CTLC	CTLD	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20
1	TRx1	L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H
2	TRx2	H	L	H	L	L	H	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H
3	TRx3	H	H	H	L	L	L	H	L	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
4	TRx4	H	L	H	H	L	L	L	H	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H
5	TRx5	H	H	H	H	L	L	L	L	H	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H
6	TRx6	H	L	L	H	L	L	L	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H	H
7	Rx1	L	H	H	L	L	L	L	L	L	L	H	L	L	L	H	H	H	H	H	H	L	H	H	H
8	Rx2	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	H	H	H	H	H	H	L	H	H
9	Tx1	H	H	L	L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	L	H
10	Tx2	H	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
11	Idle (*2)	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

(*1) State “L” means a switch “OFF”, State “H” means a switch “ON”

(*2) State “Idle” means that the DC/DC converter is “OFF”, and the switch paths are in an undefined state.

Pin Configuration of SP10T



DC Bias Condition

(Ta = 25 °C)

Parameter	Min.	Typ.	Max.	Unit
V_{DD}	+2.5	+2.8	+5.0	V
VCTL(H)	+1.35	+1.8	+3.1	V
VCTL(L)	0	—	+0.45	V

Target Specification

(V_{DD} = 2.5 V, Ta = 25 °C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Ant - TRx1	*1, *2, *3, *10	—	0.48	0.58	dB
			*4, *11	—	0.65	0.80	
			*5	—	0.69	0.84	
		Ant - TRx2	*1, *2, *3, *10	—	0.46	0.56	
			*4, *11	—	0.63	0.78	
			*5	—	0.70	0.85	
		Ant - TRx3	*1, *2, *3, *10	—	0.40	0.50	
			*4, *11	—	0.54	0.69	
			*5	—	0.58	0.73	
		Ant - TRx4	*1, *2, *3, *10	—	0.39	0.49	
			*4, *11	—	0.49	0.64	
			*5	—	0.51	0.66	
		Ant - TRx5	*1, *2, *3, *10	—	0.44	0.54	
			*4, *11	—	0.60	0.75	
			*5	—	0.66	0.81	
			*6	—	0.75	0.95	
			*7	—	0.96	1.16	
		Ant - TRx6	*1, *2, *3, *10	—	0.45	0.55	
			*4, *11	—	0.69	0.84	
			*5	—	0.75	0.90	
		Ant - Tx1	*8	—	1.10	1.20	
		Ant - Tx2	*9	—	1.20	1.35	
		Ant - Rx1, 2	*10	—	0.80	0.90	
			*11	—	0.99	1.14	
VSWR	VSWR	All ports in active paths	600 to 2170 MHz	—	—	1.50	—
Harmonics	2fo	Ant - TRx1, 2, 3, 4, 5, 6	*2, *3, *4	—	—	–40	dBm
	3fo			—	—	–40	
	2fo	Ant - TRx4	*2, *12B	—	—	–78	
	2fo	Ant - Tx1	*8	—	—	–36	
	3fo			—	—	–36	
	2fo	Ant - Tx2	*9	—	—	–36	
	3fo			—	—	–36	
Attenuation	ATT	Tx1 - Ant	1648 to 1805 MHz	25	—	—	dB
			1805 to 1830 MHz	30	—	—	
			2472 to 2745 MHz	25	—	—	
			3296 to 10000 MHz	20	—	—	
			10000 to 12750 MHz	15	—	—	
		Tx2 - Ant	3420 to 3820 MHz	25	—	—	
			5130 to 5730 MHz	25	—	—	
			6840 to 12750 MHz	20	—	—	
Inter modulation product power in Rx band	IMD2	Ant - TRx1, 2, 3, 4, 5 ,6	*12A, 13, 14, 17, 18, 21, 22	—	—	–105	dBm
	IMD3		*12A, 15, 16, 19, 20, 23, 24	—	—	–105	
Input IP3	IIP3	Ant - TRx1, 2, 3, 4, 5, 6	*12A, 25, 26	—	68	—	
Switching time	Ts	Active mode	50 % Ctl to 90 % RF	—	3	5	µs
Wake up time	Tw		Wake up time from Idle mode to Active mode	—	30	50	µs
Control current	Ictl		V_{CTL} = 1.80 V	—	1	5	µA
Supply current	I_{DD}	Active mode	V_{DD} = 2.8 V	—	0.22	0.4	mA
Supply current	I_{DD}	Idle mode	V_{DD} = 2.8 V	—	—	20	µA

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO	Tx1 - TRx1, 2, 3, 4, 5, 6, Rx1, 2	*8 (Tx1 Active)	40	—	—	dB
		Tx2 - TRx1, 2, 3, 4, 5, 6	*9 (Tx2 Active)	32	—	—	
		Tx2 - Rx1, 2		40	—	—	
		TRx1, 2, 3 - TRx4, 5, 6	*1, *2, *3, *10 (TRx1, 2, 3, 4, 5, 6 Active)	40	—	—	
		TRx1, 2, 3 - TRx4, 5, 6	*4, *5, *11 (TRx1, 2, 3, 4, 5, 6 Active)	30	—	—	
		TRx5 - TRx1, 2, 3	*6, *7 (TRx5 Active)	25	—	—	
		TRx1 - TRx2	*1, *2, *3, *10 (TRx1, 2 Active)	30	—	—	
		TRx1 - TRx2	*4, *5, *11 (TRx1, 2 Active)	18	—	—	
		TRx1 - TRx3	*1, *2, *3, *10 (TRx1, 3 Active)	40	—	—	
		TRx1 - TRx3	*4, *5, *11 (TRx1, 3 Active)	20	—	—	
		TRx2 - TRx3	*1, *2, *3, *10 (TRx2, 3 Active)	25	—	—	
		TRx2 - TRx3	*4, *5, *11 (TRx2, 3 Active)	15	—	—	
		TRx4 - TRx5	*1, *2, *3, *10 (TRx4, 5 Active)	30	—	—	
		TRx4 - TRx5	*4, *5, *11 (TRx4, 5 Active)	21	—	—	
		TRx4 - TRx5	*6, *7 (TRx5 Active)	15	—	—	
		TRx4 - TRx6	*1, *2, *3, *10 (TRx4, 6 Active)	40	—	—	
		TRx4 - TRx6	*4, *5, *11 (TRx4, 6 Active)	26	—	—	
		TRx5 - TRx6	*1, *2, *3, *10 (TRx5, 6 Active)	30	—	—	
		TRx5 - TRx6	*4, *5, *11 (TRx5, 6 Active)	24	—	—	
		TRx5 - TRx6	*6, *7 (TRx5 Active)	17	—	—	
		Rx1 - Rx2	*11 (Rx1, 2 Active)	33	—	—	

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

Corresponding Band of TRx (UMTS/CDMA/GSM)

*1 Pin = 26 dBm, 452 to 468 MHz (Band Class 5)
*2 Pin = 25 dBm, 704 to 787 MHz (Band 13, Band 17)
*3 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 8)
*4 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 3 Tx, Band 4 Tx)
*5 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)
*6 Pin = 26 dBm, 2300 to 2400 MHz (Band 40)
*7 Pin = 26 dBm, 2500 to 2690 MHz (Band 7)
*8 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)
*9 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)
*10 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)
*11 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)
*12A Measured with the recommended circuit 1, 2
*12B Measured with the recommended circuit 3

IMD Condition

Band	fRx on TRx	fTx +20 dBm on TRx	fBlocker –15 dBm on Ant		IMD condition
Band I	2140 MHz	1950 MHz	IMD2 (fRx – fTx)	190 MHz	*13
			IMD2 (fRx + fTx)	4090 MHz	*14
			IMD3 (2fTx – fRx)	1760 MHz	*15
			IMD3 (2fTx + fRx)	6040 MHz	*16
Band II	1960 MHz	1880 MHz	IMD2 (fRx – fTx)	80 MHz	*17
			IMD2 (fRx + fTx)	3840 MHz	*18
			IMD3 (2fTx – fRx)	1800 MHz	*19
			IMD3 (2fTx + fRx)	5720 MHz	*20
Band V	880 MHz	835 MHz	IMD2 (fRx – fTx)	45 MHz	*21
			IMD2 (fRx + fTx)	1715 MHz	*22
			IMD3 (2fTx – fRx)	790 MHz	*23
			IMD3 (2fTx + fRx)	2550 MHz	*24

IIP3 Condition

Band	f1 +27 dBm on TRx	f2 +27 dBm on TRx	IIP3 condition IIP3 = (3 * Pout – IM3)/2
Band I	1950 MHz	1951MHz	*25
Band V	835 MHz	836MHz	*26

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit.

Target Specification of Triple Beat Ratio

(V_{DD} = 2.5V, Ta = 25 °C)

Item	Symbol	Path	Condition				Min.	Typ.	Max.	Unit
			Tx1 at TRx* 21.5dBm	Tx2 at TRx* 21.5dBm	Jammer at Ant –30 dBm	Triple beat product at TRx*				
Triple beat ratio	TBR	Ant - TRx1, 2, 3, 4, 5, 6	835.5 MHz	836.5 MHz	881.5 MHz	881.5 ± 1 MHz	81	—	—	dBc
			1880 MHz	1881 MHz	1960 MHz	1960 ± 1 MHz	81	—	—	

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit

Target Specification of Input IP2

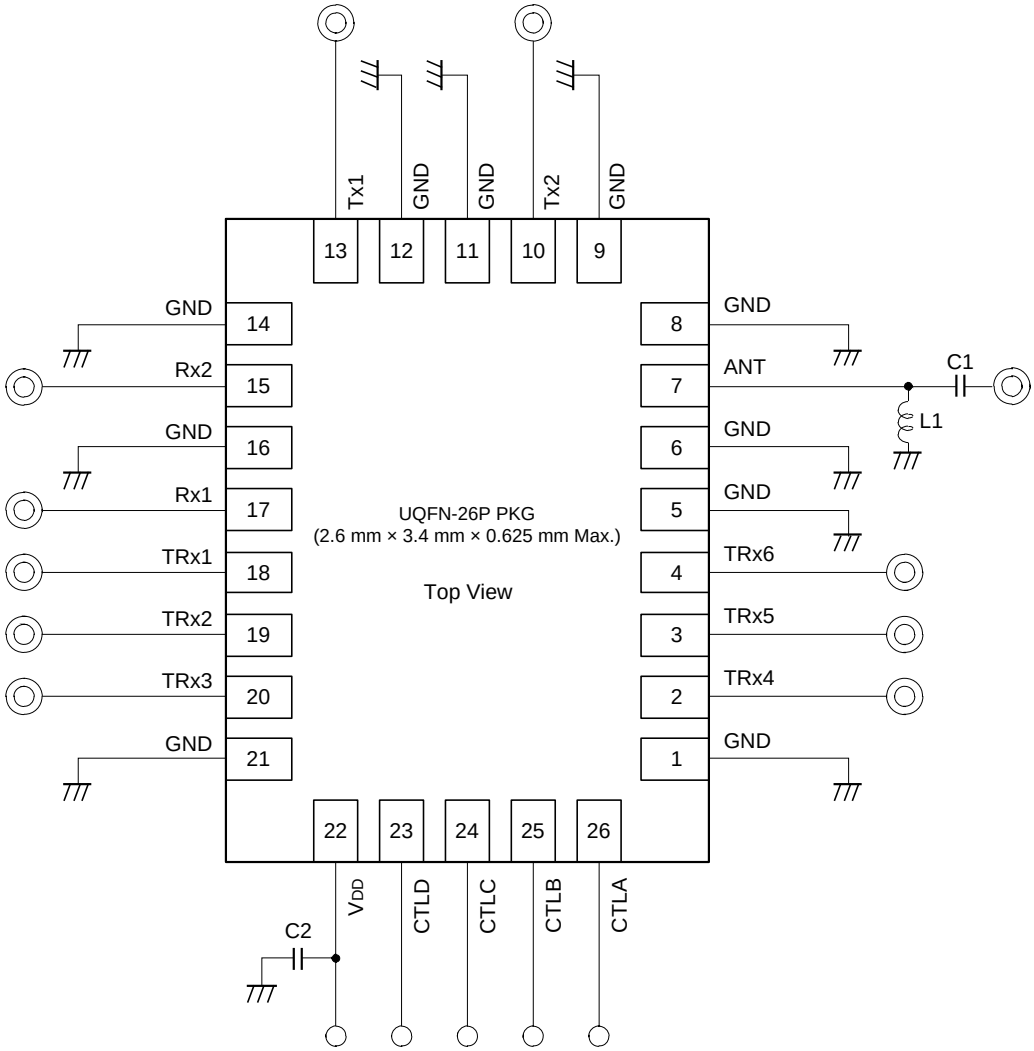
(V_{DD} = 2.5 V, Ta = 25 °C)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
			Tx at TRx* 24 dBm	Jammer at Ant –20 dBm	IM2 product at TRx*				
Input IP2	IIP2	Ant - TRx1, 2, 3, 4, 5, 6	836.61	1718.61	881.61	113.5	—	—	dBm
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit

Recommended Circuit 1

Operation frequency range: 0.7-2.7 GHz



*1: No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)

*2: DC levels of all RF ports are GND.

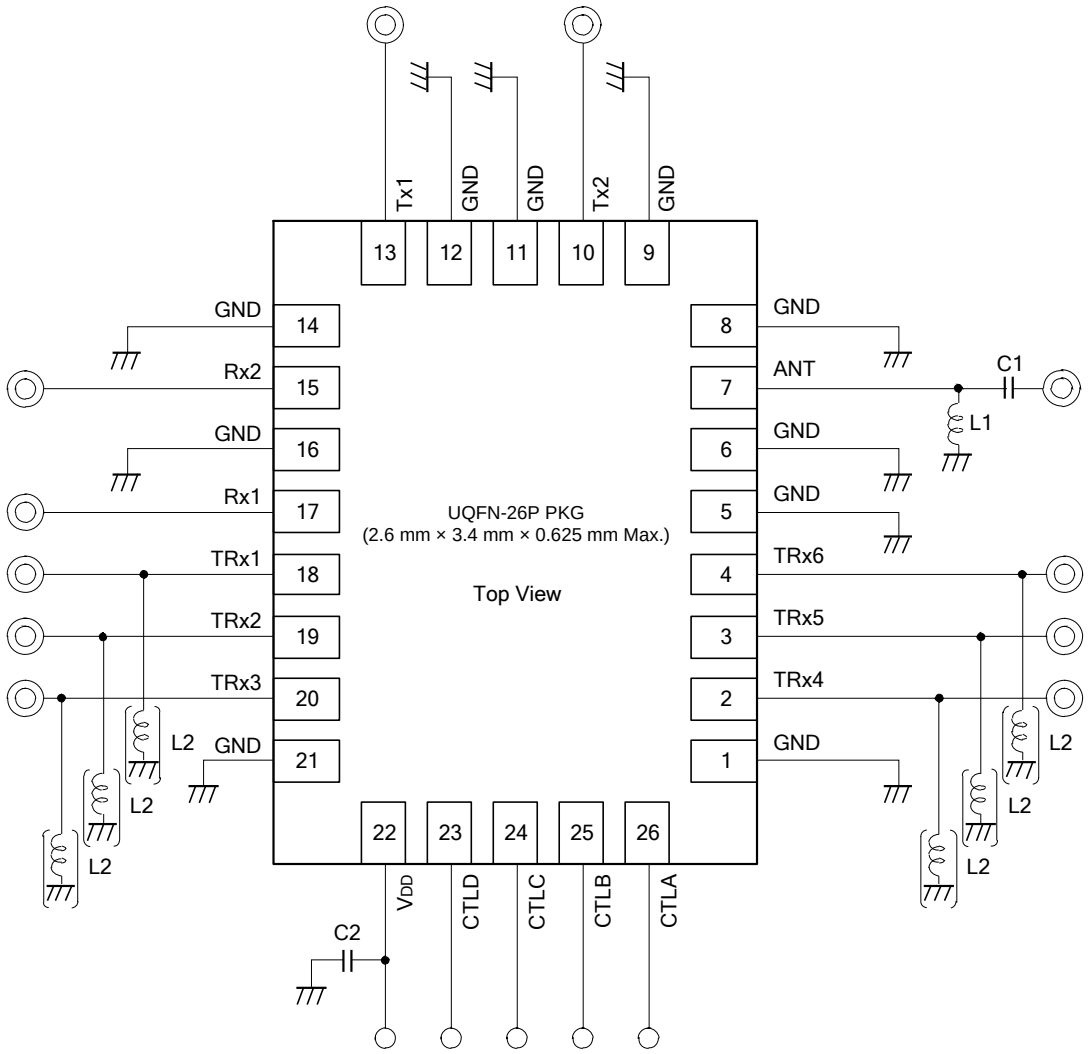
*3: L1 (22 nH) and C1 (22 pF) are recommended on Ant port for ESD protection.

*4: C2 capacitor (100 pF) is recommended.

*5: TRx5 is recommended for Band7.

Recommended Circuit 2

Operation frequency range: 0.45-2.7 GHz



*1: No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)

*2: DC levels of all RF ports are GND.

*3: L1 (47 nH) and C1 (22 pF) are recommended on Ant port for ESD protection.

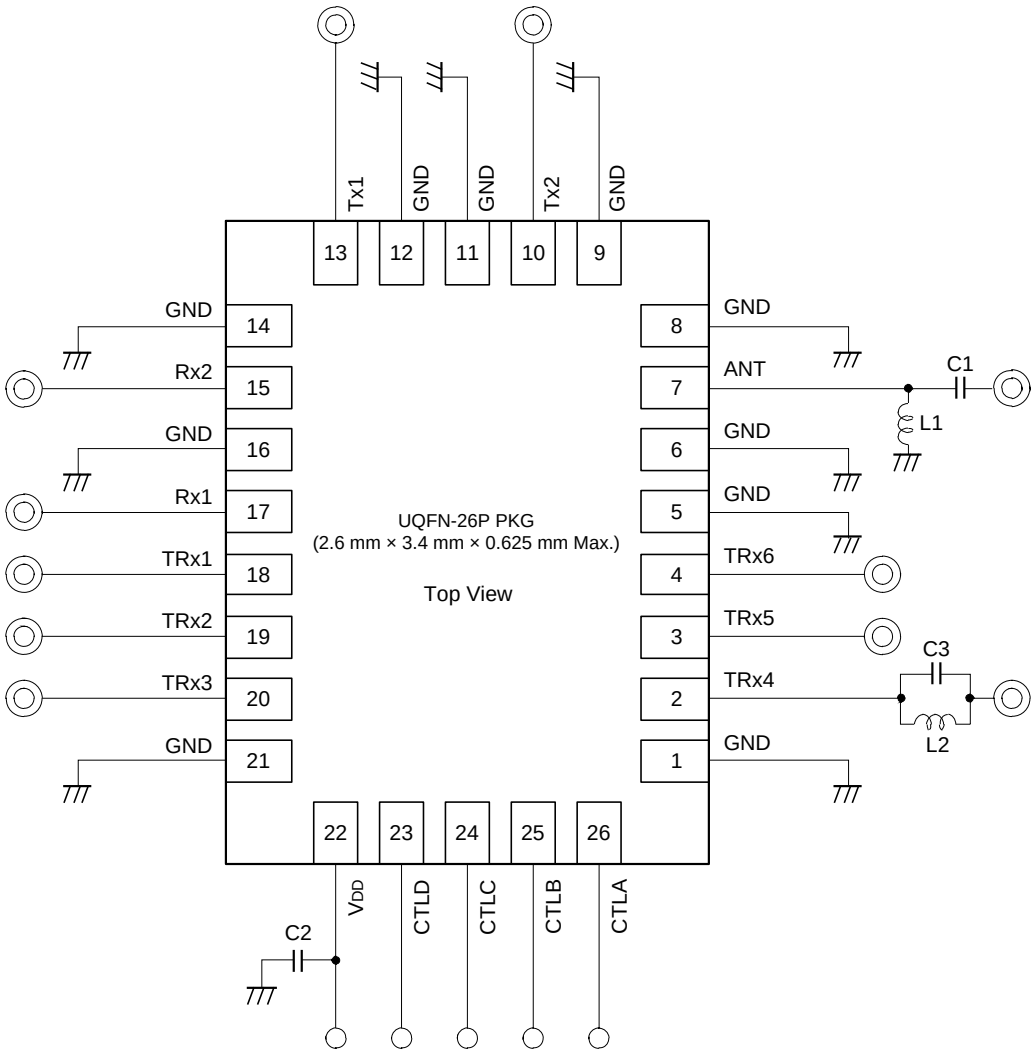
*4: C2 Capacitor (100 pF) is recommended.

*5: TRx5 is recommended for Band7.

*6: L2 (12 nH) is recommended on a TRx port assigned for Band I to improve IMD2 performance. (Rx-Tx (190 MHz))

Recommended Circuit 3

2nd Harmonics Improvement at LTE (Band13)



*1: No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)

*2: DC levels of all RF ports are GND.

*3: L1 (47 nH) and C1(22 pF) are recommended on Ant port for ESD protection.

*4: C2 Capacitor (100 pF) is recommended.

*5: TRx5 is recommended for Band7.

*6: L2 (1.8 nH) and C3 (4.0 pF) are recommended when TRx4 is assigned for Band 13.

Recommended Land Pattern

UQFN-26P-01 Macro drawing (Reference)

- PKG: 3.4 mm x 2.6 mm
- Pin pitch: 0.4 mm

* Metal mask thickness: 110 µm

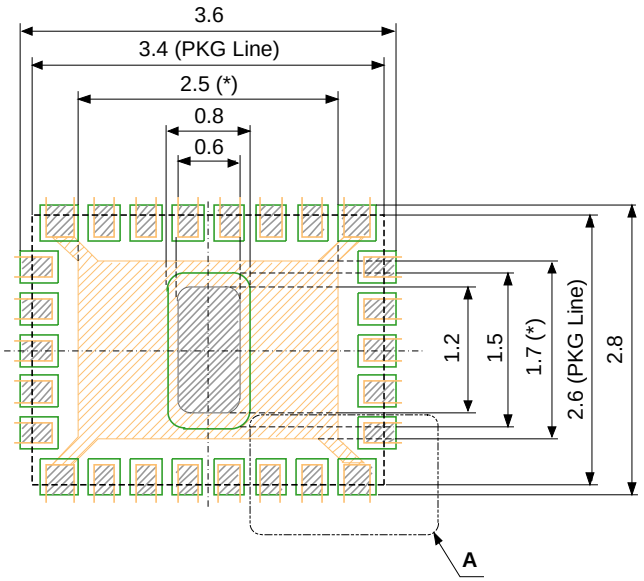
: Metal area in board (*1)

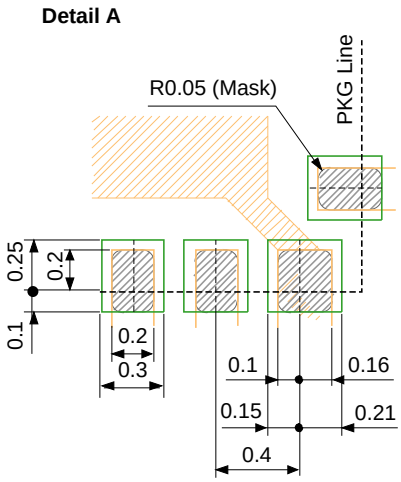
*1: GND plane is recommended.

: Land

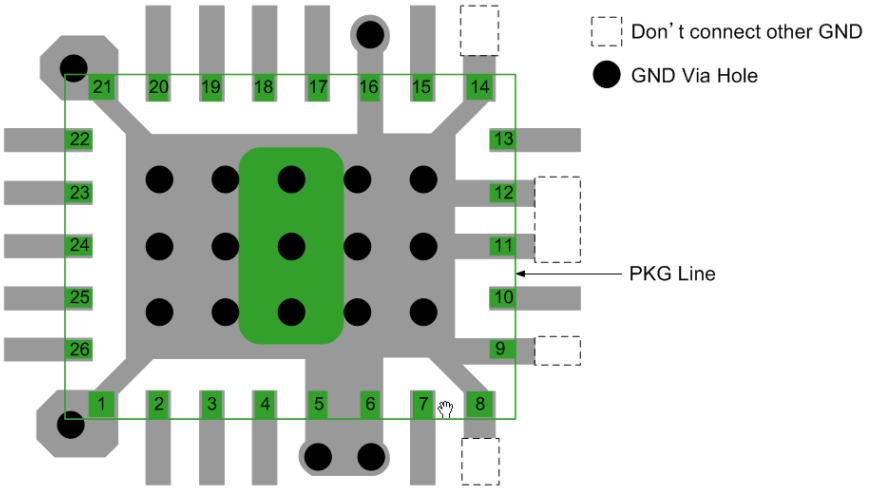
: Mask (Open area)

: Resist (Open area)





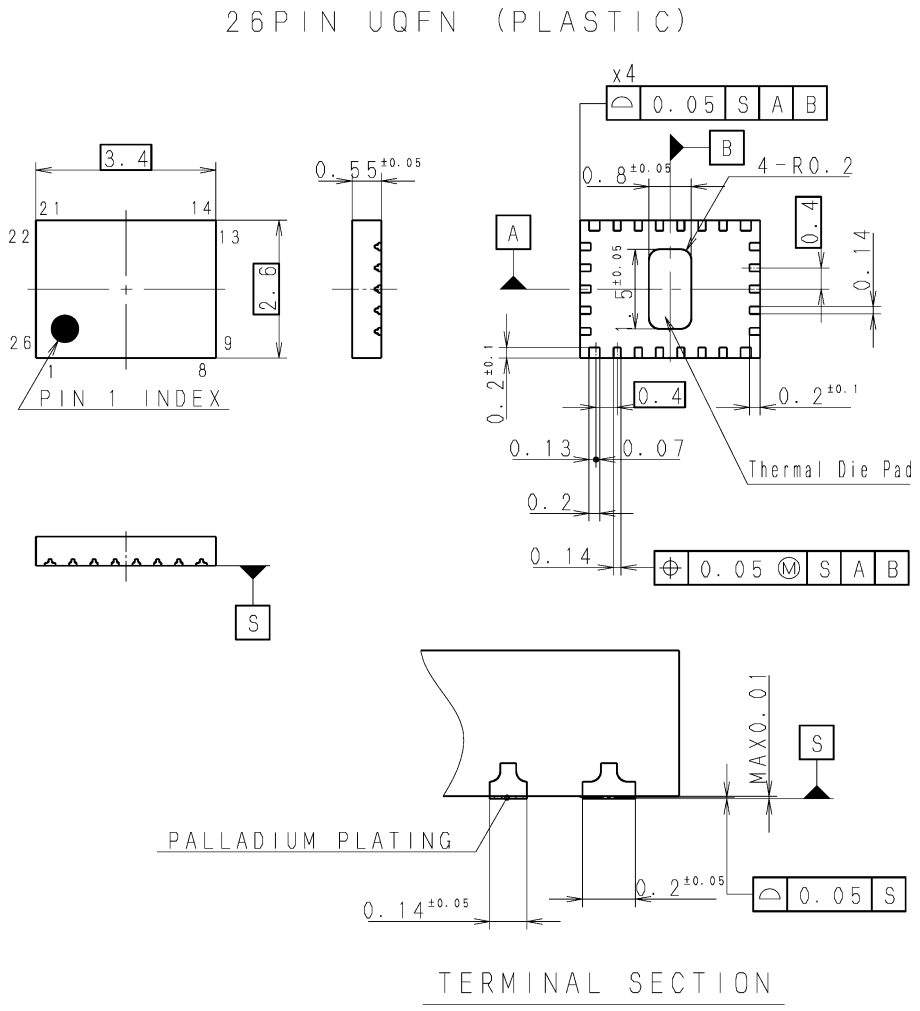
PCB Design for UQFN-26P



Package Outline

(Unit: mm)

Product Code：875342105



TERMINAL SECTION

Note:Terminal burr height 0.05mm MAX.

SONY CODE	UQFN-26P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

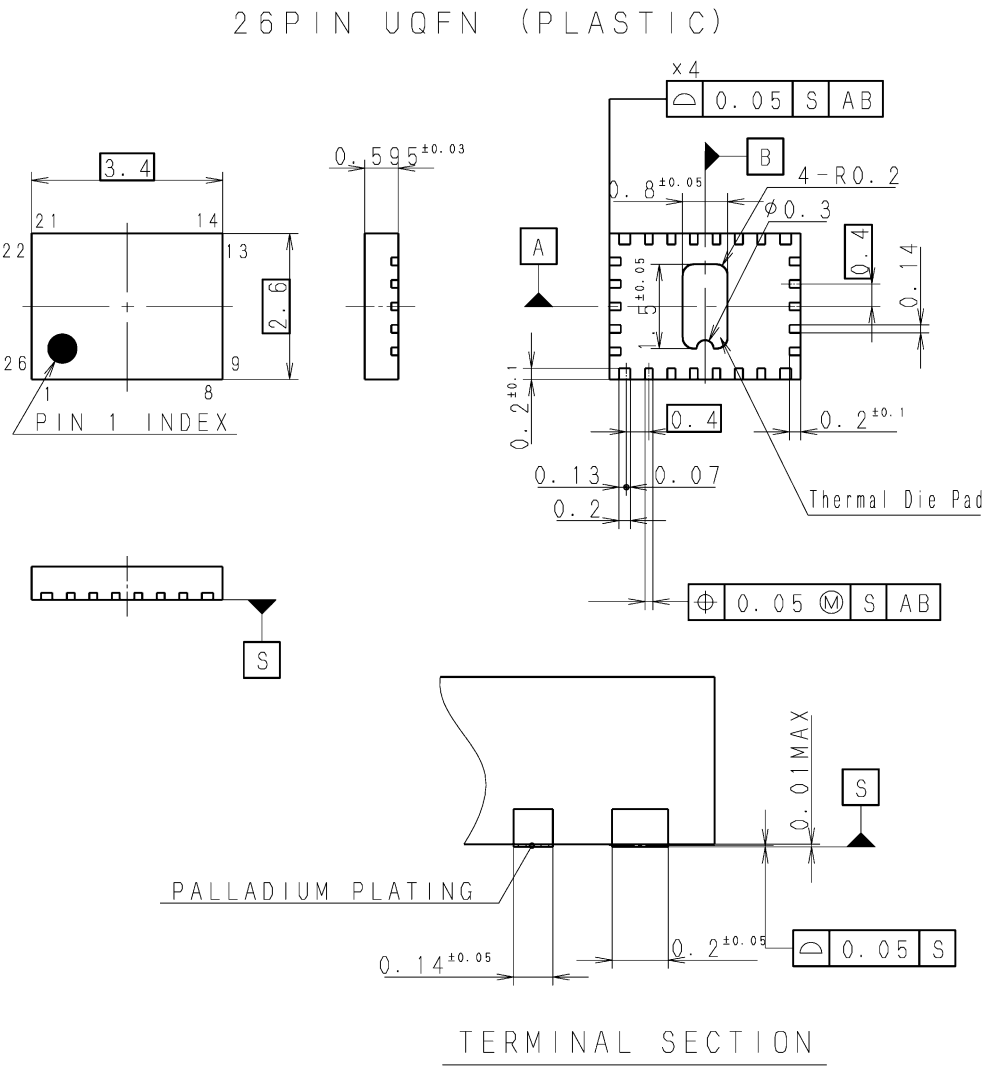
PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

PART No. AP-4000-26011S	Rev. 0
ISSUED '11.06.20	REVISED
PRODUCTION LINE	COMPILING DIV. SDT ENGINEERING DIVISION
REMARKS PKG CORD:UR-26-1	

Package Outline

(Unit: mm)

Product Code : 875340939



Note:Terminal burr height 0.05mm MAX.

SONY CODE	UQFN-26P-541
JEITA CODE	————
JEDEC CODE	————

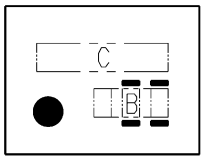
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	PALLADIUM PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

PART No. AP-2000-26QNBE3	Rev. 0
ISSUED '11.11.24	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:UR-26-CBE	

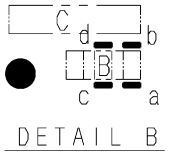
Marking

Product Code: 875342105



MARKING C: M3582

注1） B部はロット番号（Ｍａｘ３文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記２進法ビット方式により表示する。）
ａ部年コード（２進法ビット方式の１ビット目を表示）を配置する。
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ５文字）を配置する。
（５文字を超える場合は製品名省略標示規定に従う。）
注3） マーク深さは、ＭＡＸ０．０５ｍｍの事.

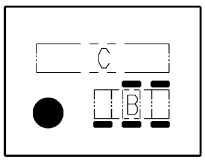


DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION d.
2) TYPE NO.(MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm

Marking

Product Code: 875340939



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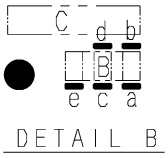
ｂ部年コード（２進法ビット方式の２ビット目を表示）を配置する。
ｃ部年コード（２進法ビット方式の３ビット目を表示）を配置する。
ｄ部年コード（２進法ビット方式の４ビット目を表示）を配置する。
注2） C部は製品名（Ｍａｘ５文字）を配置する。
（５文字を超える場合は製品名省略標示規定に従う。）
注3） ｅ部は組立場所表記を配置する。



DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION d.
2) TYPE NO.(MAX 5 CHARACTERS) IN SECTION C.
(FOR MORE THAN 5 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) ASSEMBLY PLACE IN SECTION e.

Note

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