SONY

SP10T Antenna Switch for GSM/UMTS Dual Mode Handsets

CXM3560XR

Description

The CXM3560XR is SP10T antenna switch for GSM/UMTS dual mode handsets.
The CXM3560XR has a 1.8V CMOS compatible decoder.
The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity.
(Applications: GSM (4bands) and UMTS (4bands) Dual-Mode Handsets)

Features

◆ Low Insertion Loss: 0.30dB (Typ.) Tx1 (GSM Low Band Tx)
0.45dB (Typ.) Tx2 (GSM High Band Tx)
0.60dB (Typ.) TRx1 (UMTS Band I)

◆ Low Voltage Operation: V_{DD} = 2.5V

◆ No DC Blocking Capacitors required on RF ports

◆ Small package size: XQFN-24P-02 (2.2mm × 2.9mm × 0.4mm Max.)

◆ Lead-Free and RoHS Compliant

Structure

GaAs Junction Gate pHEMT (JPHEMT) MMIC Switch, CMOS Decoder

Absolute Maximum Ratings

(Ta = 25°C)

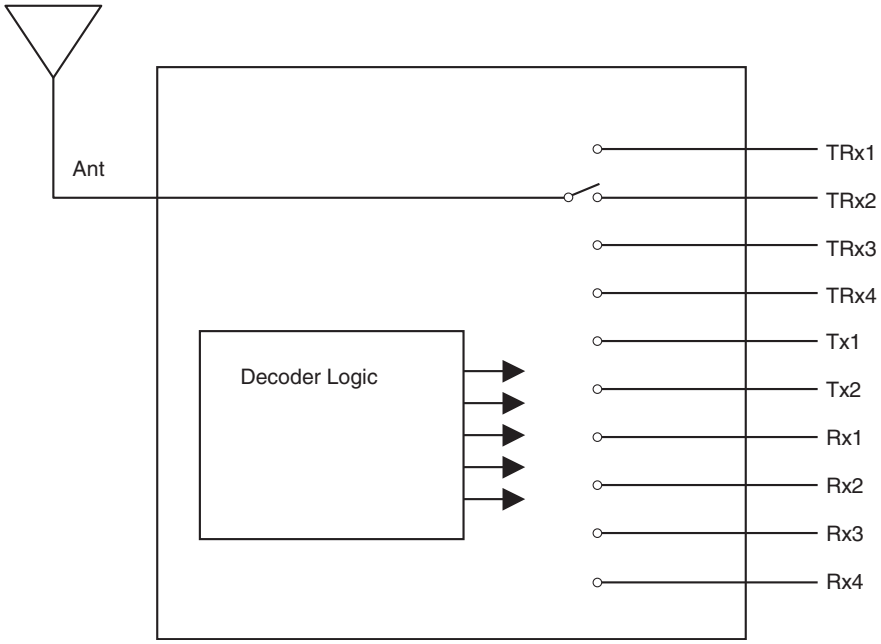
◆ Bias voltage	V_{DD}	4	V
◆ Control voltage (CTL-A/B/C/D)	Vctl	4	V
◆ Input power max. [Tx1]		36	dBm (Duty cycle = 12.5 to 50%)
◆ Input power max. [Tx2]		34	dBm (Duty cycle = 12.5 to 50%)
◆ Input power max. [TRx1, 2, 3, 4]		32	dBm
◆ Input power max. [Rx1, 2, 3, 4]		13	dBm
◆ Operating temperature range		–35 to +85	°C
◆ Storage temperature range		–65 to +150	°C

Note on Handling
GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

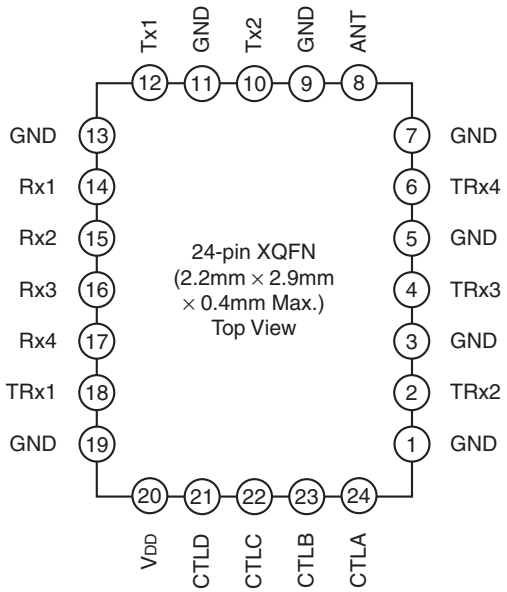
E09411A03

Block Diagram

SP10T Antenna Switch



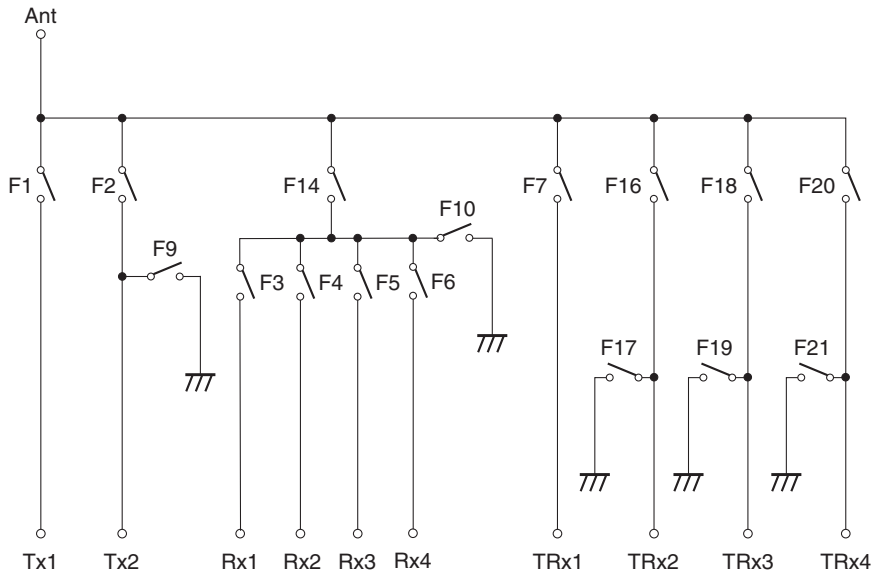
Pin Configuration



Pin Description

Pin No.	Name	Pin No.	Name
1	GND	13	GND
2	TRx2	14	Rx1
3	GND	15	Rx2
4	TRx3	16	Rx3
5	GND	17	Rx4
6	TRx4	18	TRx1
7	GND	19	GND
8	Ant	20	V_{DD}
9	GND	21	CTLD
10	Tx2 (DCS/PCS)	22	CTLC
11	GND	23	CTLB
12	Tx1 (GSM850/900M)	24	CTLA

RF Switch



Truth Table

State	Active Path	Vctl State				Switch State															
		A	B	C	D	F1	F2	F3	F4	F5	F6	F7	F9	F10	F14	F16	F17	F18	F19	F20	F21
1	Tx1	H	H	L	L	H	L	L	L	L	L	L	H	H	L	L	H	L	H	L	H
2	Tx2	H	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H	L	H	L	H
3	Rx1	L	L	L	L	L	L	H	L	L	L	L	H	L	H	L	H	L	H	L	H
4	Rx2	L	L	H	L	L	L	L	H	L	L	L	H	L	H	L	H	L	H	L	H
5	Rx3	L	H	H	L	L	L	L	L	H	L	L	H	L	H	L	H	L	H	L	H
6	Rx4	L	H	L	L	L	L	L	L	L	H	L	H	L	H	L	H	L	H	L	H
7	TRx1	H	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H	L	H	L	H
8	TRx2	H	H	H	L	L	L	L	L	L	L	L	H	H	L	H	L	L	H	L	H
9	TRx3	H	L	H	H	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H
10	TRx4	H	H	H	H	L	L	L	L	L	L	L	H	H	L	L	H	L	H	H	L
11	Sleep	L	L	L	H	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Electrical Characteristics

Supply Voltage Value

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Bias voltage (V_{DD})	+2.5	+2.65	+3.3	V

Logic Value

(Ta = 25°C)

Item	State	Min.	Typ.	Max.	Unit
Control voltage (CTL-A/B/C/D)	High	+1.5	+1.8	+3.3	V
	Low	0	—	+0.3	

Specification 1

(Ta = 25°C, V_{DD} = 2.5V, Vctl = 1.5V)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Ant-Tx1	*1	—	0.30	0.45	dB
		Ant-Tx2	*2	—	0.45	0.60	
		Ant-Rx1	*3	—	0.75	0.90	
			*4	—	1.00	1.15	
		Ant-Rx2	*3	—	0.75	0.90	
			*4	—	1.00	1.15	
		Ant-Rx3	*3	—	0.75	0.90	
			*4	—	1.00	1.15	
		Ant-Rx4	*3	—	0.75	0.90	
			*4	—	1.00	1.15	
		Ant-TRx1	*5	—	0.55	0.70	
			*6	—	0.60	0.75	
		Ant-TRx2	*5	—	0.60	0.75	
			*6	—	0.68	0.83	
			*7	—	0.45	0.60	
			*8	—	0.45	0.60	
			*9	—	0.57	0.72	
			*10	—	0.60	0.75	
		Ant-TRx3	*7	—	0.45	0.60	
			*8	—	0.45	0.60	
			*9	—	0.60	0.75	
			*10	—	0.62	0.77	
		Ant-TRx4	*7	—	0.40	0.55	
			*8	—	0.40	0.55	
			*9	—	0.65	0.80	
			*10	—	0.66	0.81	
VSWR	VSWR	All ports in Active Paths	824 to 2170MHz	—	1.20	—	—
Harmonics	2fo	Tx1-Ant	*1	—	–50	–36	dBm
	3fo			—	–40	–35	
	2fo	Tx2-Ant	*2	—	–45	–36	
	3fo			—	–40	–33	
	2fo	TRx1-Ant	*5	—	–55	–39	
	3fo			—	–54	–39	
	2fo	TRx2-Ant	*7,*9	—	–65	–39	
	3fo			—	–58	–39	
	2fo	TRx3-Ant	*7,*9	—	–65	–39	
	3fo			—	–58	–39	
	2fo	TRx4-Ant	*7	—	–65	–39	
	3fo			—	–58	–39	

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Inter modulation product power in Rx band	IMD2	TRx1-Ant	*11, *19	—	–105	–97	dBm
		TRx2-Ant	*12, *19	—	–105	–97	
			*13, *19	—	–105	–97	
			*14, *19	—	–105	–97	
		TRx3-Ant	*12, *19	—	–105	–97	
			*13, *19	—	–105	–97	
			*14, *19	—	–105	–97	
		TRx4-Ant	*14, *19	—	–105	–97	
	IMD3	TRx1-Ant	*15, *19	—	–105	–97	
		TRx2-Ant	*16, *19	—	–105	–97	
			*17, *19	—	–105	–97	
			*18, *19	—	–105	–97	
		TRx3-Ant	*16, *19	—	–105	–97	
			*17, *19	—	–105	–97	
			*18, *19	—	–105	–97	
		TRx4-Ant	*18, *19	—	–105	–97	
Switching time	Ts		50%Ctl to 90%RF	—	3	5	μS
Control current	Ictl		Vctl = 1.80V	—	1	5	μA
Supply current	Idd		V_{DD} = 2.65V	—	0.18	0.40	mA
Sleep current	Isleep		Sleep mode *state11 V_{DD} = 2.65V	—	4	10	μA

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

*1 Pin on Tx1: 34dBm, 824 to 915MHz, Tx1 enabled
*2 Pin on Tx2: 32dBm, 1710 to 1910MHz, Tx2 enabled
*3 Pin on Ant: 10dBm, 869 to 960MHz, Rx1, Rx2, Rx3 or Rx4 enabled
*4 Pin on Ant: 10dBm, 1805 to 1990MHz, Rx1, Rx2, Rx3 or Rx4 enabled
*5 Pin on TRx1 or TRx2: 26dBm, 1920 to 1980MHz, TRx1 or TRx2 enabled
*6 Pin on Ant: 10dBm, 2110 to 2170MHz, TRx1 or TRx2 enabled
*7 Pin on TRx2, TRx3 or TRx4: 26dBm, 824 to 849MHz, TRx2, TRx3 or TRx4 enabled
*8 Pin on Ant: 10dBm, 869 to 894MHz, TRx2, TRx3 or TRx4 enabled
*9 Pin on TRx2, TRx3 or TRx4: 26dBm, 1710 to 1910MHz, TRx2, TRx3 or TRx4 enabled
*10 Pin on Ant: 10dBm, 1805 to 1990MHz, TRx2, TRx3 or TRx4 enabled
*11 Pin on TRx1: 20dBm, 1950MHz, Pin on Ant: –15dBm, 190MHz, TRx1 enabled
*12 Pin on TRx2 or TRx3: 20dBm, 1745MHz, Pin on Ant: –15dBm, 95MHz, TRx2 or TRx3 enabled
*13 Pin on TRx2 or TRx3: 20dBm, 1880MHz, Pin on Ant: –15dBm, 80MHz, TRx2 or TRx3 enabled
*14 Pin on TRx2, TRx3 or TRx4: 20dBm, 835MHz, Pin on Ant: –15dBm, 45MHz, TRx2, TRx3 or TRx4 enabled
*15 Pin on TRx1: 20dBm, 1950MHz, Pin on Ant: –15dBm, 1760MHz, TRx1 enabled
*16 Pin on TRx2 or TRx3: 20dBm, 1745MHz, Pin on Ant: –15dBm, 1650MHz, TRx2 or TRx3 enabled
*17 Pin on TRx2 or TRx3: 20dBm, 1880MHz, Pin on Ant: –15dBm, 1800MHz, TRx2 or TRx3 enabled
*18 Pin on TRx2, TRx3 or TRx4: 20dBm, 835MHz, Pin on Ant: –15dBm, 790MHz, TRx2, TRx3 or TRx4 enabled
*19 Measured with the recommended circuit

Specification 1-Isolation

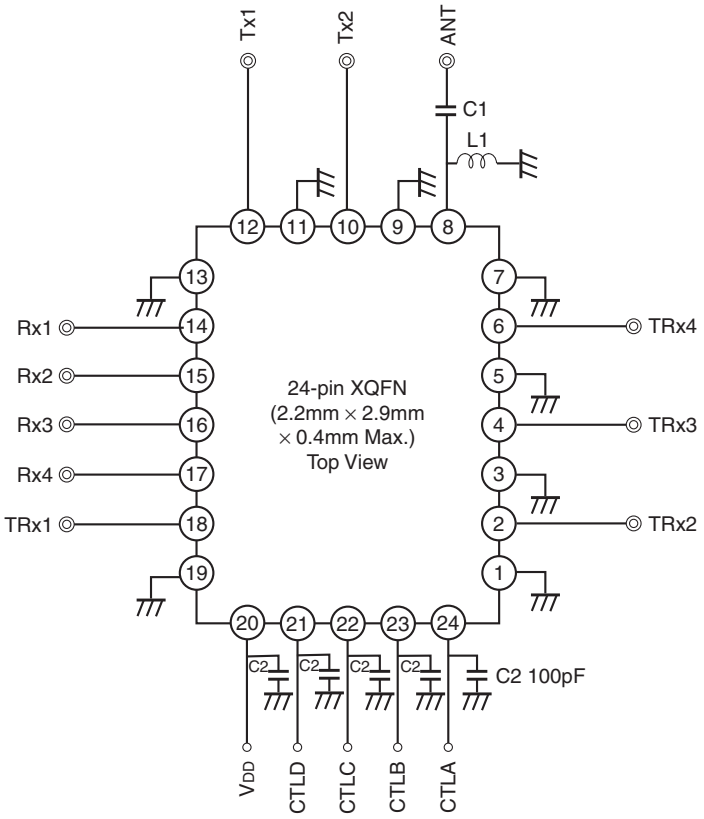
(Ta = 25°C, V_{DD} = 2.5V, Vctl = 1.5V)

Item	Symbol	Path		Condition	Min.	Typ.	Max.	Unit
		Active	Isolation					
Isolation	ISO	Tx1	Tx1-Rx1	824 to 915MHz	35	50	—	dB
			Tx1-Rx2		35	55	—	
			Tx1-Rx3		35	55	—	
			Tx1-Rx4		35	55	—	
			Tx1-TRx1		25	30	—	
			Tx1-TRx2		25	48	—	
			Tx1-TRx3		25	50	—	
			Tx1-TRx4		25	35	—	
			Tx1-Tx2		25	35	—	
			Tx1-Tx2	1648 to 1830MHz	18	25	—	
		Tx2	Tx2-Rx1	1710 to 1910MHz	35	55	—	
			Tx2-Rx2		35	55	—	
			Tx2-Rx3		35	55	—	
			Tx2-Rx4		35	45	—	
			Tx2-TRx1		20	23	—	
			Tx2-TRx2		20	38	—	
			Tx2-TRx3		20	40	—	
			Tx2-TRx4		20	30	—	
			Tx2-Tx1		16	19	—	
		TRx1	TRx1-Rx1	1920 to 1980MHz	30	53	—	
			TRx1-Rx2		30	48	—	
			TRx1-Rx3		30	40	—	
			TRx1-Rx4		20	24	—	
			TRx1-TRx2		27	35	—	
			TRx1-TRx3		23	40	—	
			TRx1-TRx4		23	30	—	
			TRx1-Tx1		17	19	—	
			TRx1-Tx2		20	33	—	

Item	Symbol	Path		Condition	Min.	Typ.	Max.	Unit
		Active	Isolation					
Isolation	ISO	TRx2	TRx2-Rx1	824 to 849MHz	30	62	—	dB
			TRx2-Rx2		30	62	—	
			TRx2-Rx3		30	62	—	
			TRx2-Rx4		30	55	—	
			TRx2-TRx1		20	30	—	
			TRx2-TRx3		20	30	—	
			TRx2-TRx4		20	35	—	
			TRx2-Tx1		20	27	—	
			TRx2-Tx2		20	45	—	
			TRx2-Rx1	1710 to 1910MHz	30	58	—	
			TRx2-Rx2		30	58	—	
			TRx2-Rx3		30	55	—	
			TRx2-Rx4		30	45	—	
			TRx2-TRx1		18	23	—	
			TRx2-TRx3		18	24	—	
			TRx2-TRx4		18	28	—	
			TRx2-Tx1		17	19	—	
			TRx2-Tx2		20	34	—	
		TRx3	TRx3-Rx1	824 to 849MHz	30	62	—	
			TRx3-Rx2		30	62	—	
			TRx3-Rx3		30	62	—	
			TRx3-Rx4		30	57	—	
			TRx3-TRx1		20	30	—	
			TRx3-TRx2		20	35	—	
			TRx3-TRx4		20	32	—	
			TRx3-Tx1		20	26	—	
			TRx3-Tx2		20	45	—	
			TRx3-Rx1	1710 to 1910MHz	30	57	—	
			TRx3-Rx2		30	58	—	
			TRx3-Rx3		30	55	—	
			TRx3-Rx4		30	45	—	
			TRx3-TRx1		18	23	—	
			TRx3-TRx2		18	29	—	
			TRx3-TRx4		18	25	—	
			TRx3-Tx1		17	19	—	
			TRx3-Tx2		20	33	—	
		TRx4	TRx4-Rx1	824 to 849MHz	35	62	—	
			TRx4-Rx2		35	62	—	
			TRx4-Rx3		35	62	—	
			TRx4-Rx4		35	57	—	
			TRx4-TRx1		20	30	—	
			TRx4-TRx2		35	42	—	
			TRx4-TRx3		30	35	—	
			TRx4-Tx1		20	27	—	
			TRx4-Tx2		30	45	—	

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

Recommended Circuit



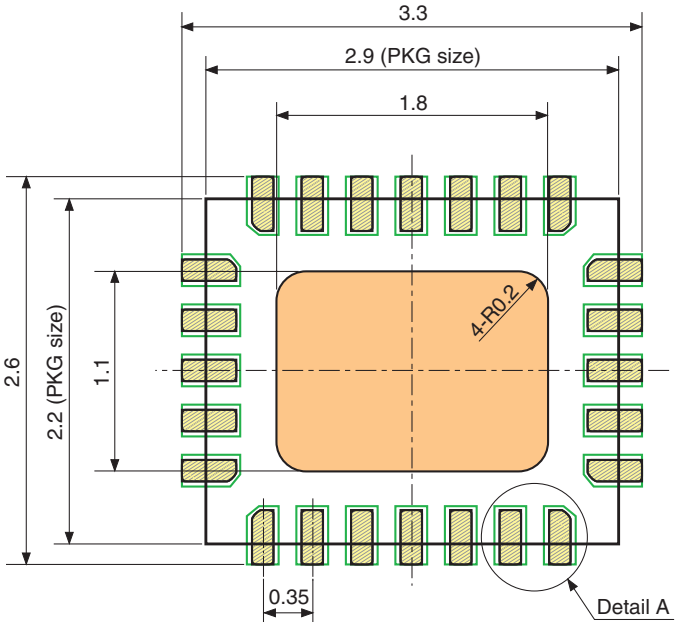
Note) 1. No DC blocking Capacitors are required on all RF ports.
2. DC levels of all RF ports are GND.
3. L1 Inductor(22nH) and C1 Capacitor(22pF) are recommended on Ant port for ESD protection.
4. C2 Capacitor (100pF) is recommended.

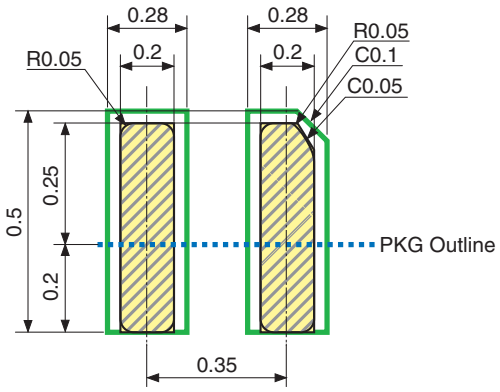
PCB Layout Template

XQFN-24P-02 Macro for MMIC (Reference)

Specification

- PKG size: 2.9mm × 2.2mm t0.35mm
- Terminal pitch: 0.35mm
- Terminal length: 0.25mm
- Mask thickness: 0.11mm





Detail A

: Land area

: Mask open area (Solder printing area)

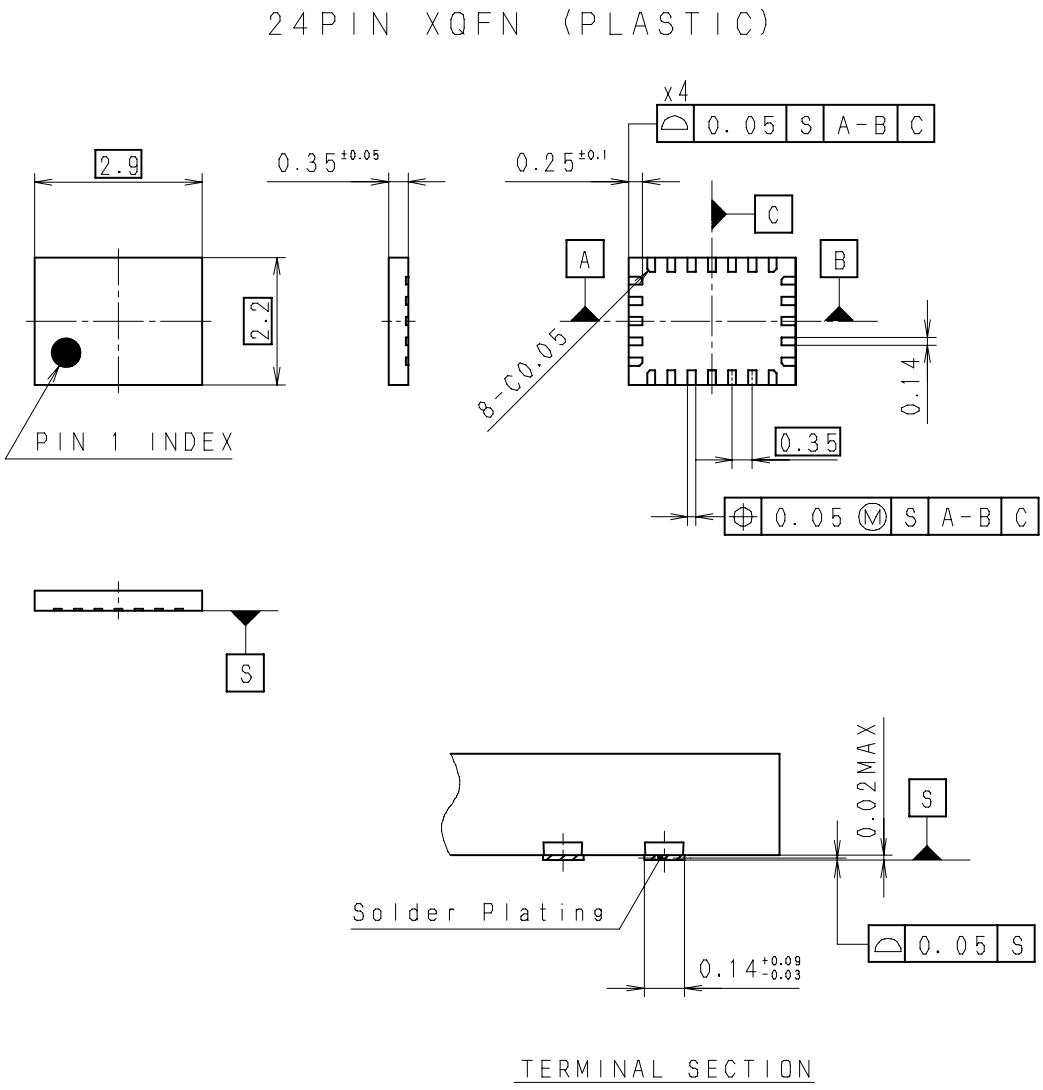
: Board resist open area

: Metal area in board (GND plane is recommended.)

: PKG outline

Package Outline

(Unit: mm)



Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	XQFN-24P-02
JEITA CODE	————
JEDEC CODE	————

AP-4000-24046S Rev. 0

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm