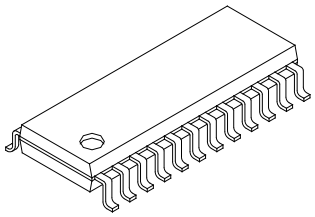
SONY

CXL1512M

CCD Delay Line for NTSC

24 pin SOP (Plastic)



Description

The CXL1512M is an IC developed for use in conjunction with Y/C signal processing ICs for NTSC. This CCD delay line provides the comb filter output for eliminating the chrominance signal cross talk and 1H delay output for luminance signals.

Features

- Single power supply (5V)
- Built-in quadruple progression PLL circuit
- Built-in comb filter
- 1H delay output
- Built-in peripheral circuits
- Positive phase signal input, positive phase signal output

Functions

- Comb filter output
- 1H delay output for luminance signal
- Clock driver
- Autobias circuit
- Input clamp circuit (for luminance signals)
- Center bias circuit (for chrominance signals)
- Sample-and-hold circuit
- Quadruple progression PLL circuit
- Clock buffer output circuit

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	+6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	500	mW

Recommended Operating Voltage (Ta = 25°C)

V_{DD} 5V ± 5%

Structure

CMOS-CCD

E94803-ST

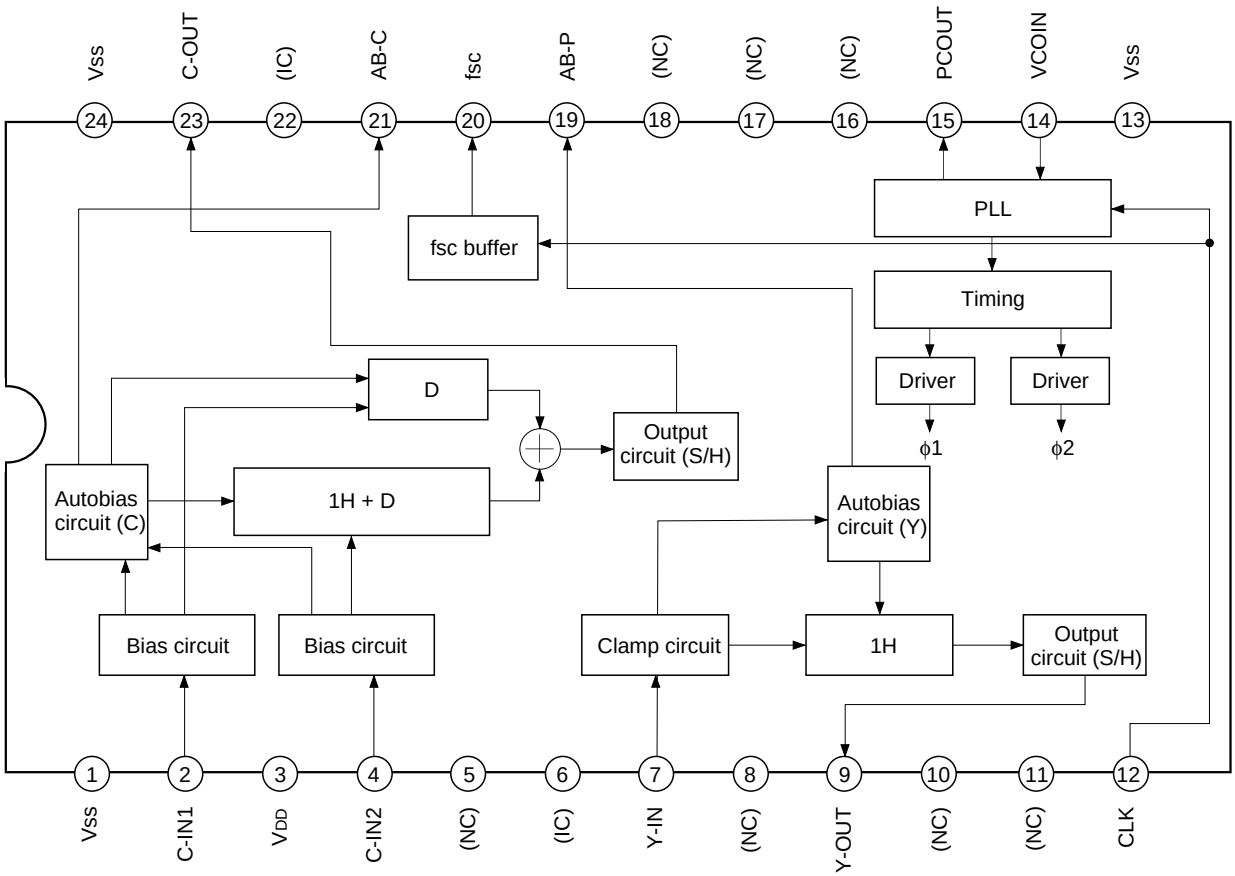
Recommended Clock Conditions (Ta = 25*C)

- Input clock amplitude V_{CLK} 0.3Vp-p to 1.0Vp-p (0.5Vp-p Typ.)
- Clock frequency f_{CLK} 3.579545MHz
- Input clock waveform sine wave

Input Signal Amplitude

Vsig 350mVp-p (Typ.), 575mVp-p (Max.)

Block Diagram and Pin Configuration (Top View)



SOP 24pin

Pin No.	Symbol	I/O	Description
1	V_{SS}	—	GND
2	C-IN1	I	Chrominance signal input 1
3	V_{DD}	—	Power supply
4	C-IN2	I	Chrominance signal input 2
5	(NC)	—	—
6 *	(IC)	—	(Connected internally)
7	Y-IN	I	Luminance signal input
8	(NC)	—	—
9	Y-OUT	O	Luminance signal output
10	(NC)	—	—
11	(NC)	—	—
12	CLK	I	Clock input
13	V_{SS}	—	GND
14	VCOIN	I	VCO input
15	PCOUT	O	Phase comparator output
16	(NC)	—	—
17	(NC)	—	—
18	(NC)	—	—
19	AB-P	O	Autobias output (P)
20	fsc	O	fsc buffer output
21	AB-C	O	Autobias output (C)
22 *	(IC)	I	(Connected internally)
23	C-OUT	O	Chrominance signal output
24	V_{SS}	—	GND

* Pins 6 and 22 are internally connected. Therefore, connect a voltage of 5V when using these pins.

Description of Functions

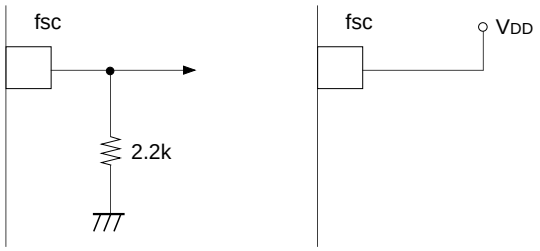
The CXL1512M provides chrominance signal comb filters and luminance signal delay outputs.

	Number of CCD bits
Chrominance comb filter output	1H (910bit)
Luminance signal delay output	1H (908bit)

- **fsc Output Pin**

  The buffer output of the clock input from the CLK pin is provided at the fsc output pin. Since a pull-up resistor is contained inside the IC, the supply voltage is produced during open, and the output is stopped. Connect a 2.2kΩ pull-down resistor when the fsc output is to be used.

<When in use> <When not in use>



Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V, f_{CLK} = 3.579545MHz, V_{CLK} = 500mVp-p sine wave)

See Electrical Characteristics Measurement Circuit

Item	Symbol	Measurement condition	SW condition						Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	6					
Supply current	IDD	—	b	b	b	a	—	—		35	50	mA	1

Chrominance signal Characteristics (No signals input to Y-IN)

Item	Symbol	Measurement condition	SW condition						Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	6					
Low frequency gain	GLC	(See Note 2)	a	a	b	—	a	b	–2	0	2	dB	2
Frequency response	FC	(See Note 3)	a	a	b	—	a	b	–2.0	–1.0	0	dB	3
Linearity	LIC	(See Note 4)	a	a	b	—	a	b	–0.3	0	0.3	dB	4
Comb depth min. gain	CCD	(See Note 5)	a	a	b	—	a	b		–40	–25	dB	5
SN ratio	SNC	50% white video signal	a	a	b	—	a	d	52	56		dB	6
Coupling level	CPC	(See Note 7)	b	b	b	—	a	b		10	50	mVrms	7
Delay time	DC	(See Note 8)	a	b	b	—	a	a	—	230	—	ns	8

<Luminance Signal Characteristics> (No signals input to C-IN1, C-IN2)

Item	Symbol	Measurement condition	SW condition						Min.	Typ.	Max.	Unit	Note
			1	2	3	4	5	6					
Low frequency gain	GLY	(See Note 2)	b	b	a	b	b	b	–2	0	2	dB	2
Frequency response	FY	(See Note 3)	b	b	a	b	b	b	–2.0	–1.0	0	dB	3
Differential gain	DGY	5-step staircase wave	b	b	a	a	b	c	0	3	5	%	9
Differential phase	DPY	5-step staircase wave	b	b	a	a	b	c	0	3	5	deg	9
Linearity	LNY	(See Note 10)	b	b	a	a	b	a	35	40	43	%	10
SN ratio	SNY	50% white video signal	b	b	a	b	b	d	52	56		dB	6
Coupling level	CPY	(See Note 7)	b	b	b	b	b	b		10	50	mVrms	7

Note

1. This is the IC's supply current value when no signals are input.

2. This is the C-OUT and Y-OUT pin output gain when 500 mVp-p sine waves are input to C-IN1, C-IN2 and Y-IN.

   (Example of calculation)

   $$GLC = 20 \log \frac{\text{C-OUT pin output voltage (mVp-p)}}{\text{500 (mVp-p)}} \text{ [dB]}$$

   Input signal frequency
   - GLC : 204.545kHz
   - GLY : 200kHz

3. This indicates the difference in the C-OUT and Y-OUT pin output gain when 200mVp-p low- and high-frequency sine waves are input to C-IN1, C-IN2 and Y-IN. Set the input bias (Vbias) to 2.0V when measuring the luminance signal characteristics (GLY, GHY).

   (Example of calculation)

   $$FC = 20 \log \frac{\text{C-OUT pin output voltage (high frequency) (mVp-p)}}{\text{C-OUT pin output voltage (low frequency) (mVp-p)}} \text{ [dB]}$$

   Input signal frequency (low frequency) → see Note 2
   Input signal frequency (high frequency)
   - Chrominance signal : 3.571678MHz
   - Luminance signal : 3.58MHz

4. Calculate with the gain applying when 200mVp-p and 500mVp-p sine waves (see Note 2 for the frequencies) are input to C-IN1 and C-IN2.

   (Example of calculation)

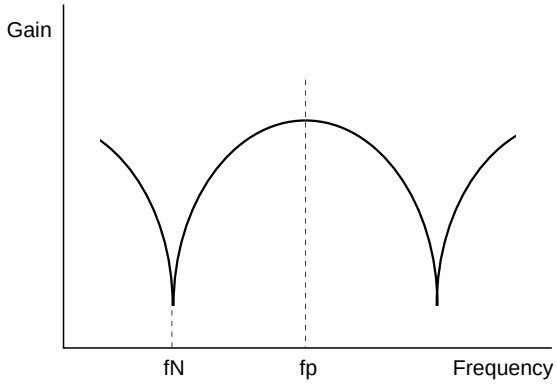
   $$LIC = 20 \log \left(\frac{\dfrac{\text{Output voltage with 500mVp-p input (mVp-p)}}{\text{500mVp-p}}}{\dfrac{\text{Output voltage with 200mVp-p input (mVp-p)}}{\text{200mVp-p}}} \right) \text{ [dB]}$$

5. Measure the difference of the C-OUT output gain when 500mVp-p sine waves have been input to C-IN1 and C-IN2 at the following frequencies shown below.

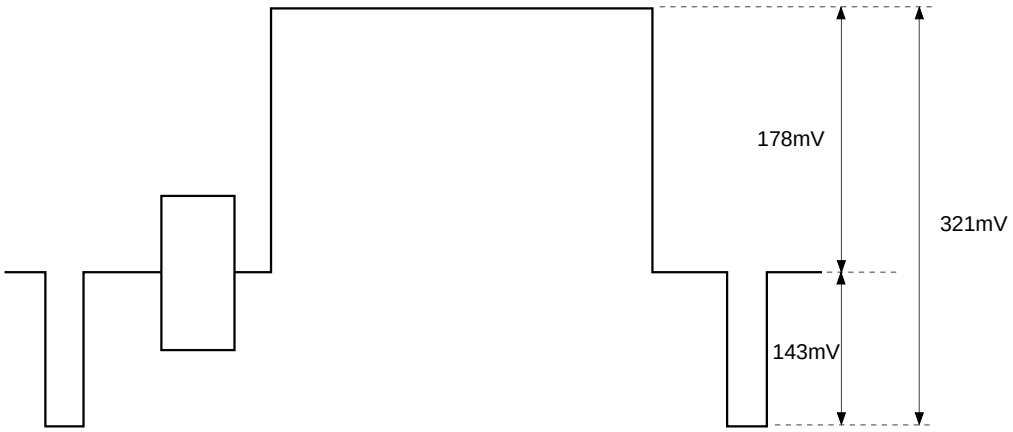
   Input signal frequency

	fp	fN
CCD	3.571678MHz	3.563811MHz

   The frequency response for the outputs at fp and fN are shown in the figure below.



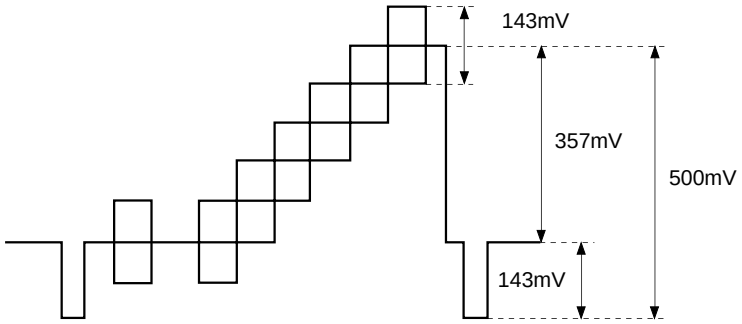
6. Using the BPF 100kHz to 4MHz in the Sub Carrier Trap mode, measure the SN ratio on the video noise meter when the 50 % white video signal shown in the figure below is input.



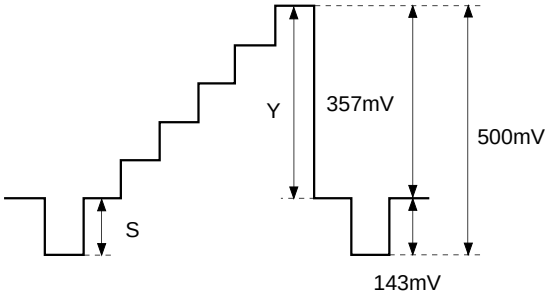
7. Measure the internal clock component (4fsc: 14.31818MHz component) when no signals are input.

8. Measure the delay time of the C-OUT output when the C-IN1 signal is input.

9. On the vector scope, measure the differential gain and differential phase when the 5-step staircase wave shown in the figure below is input.



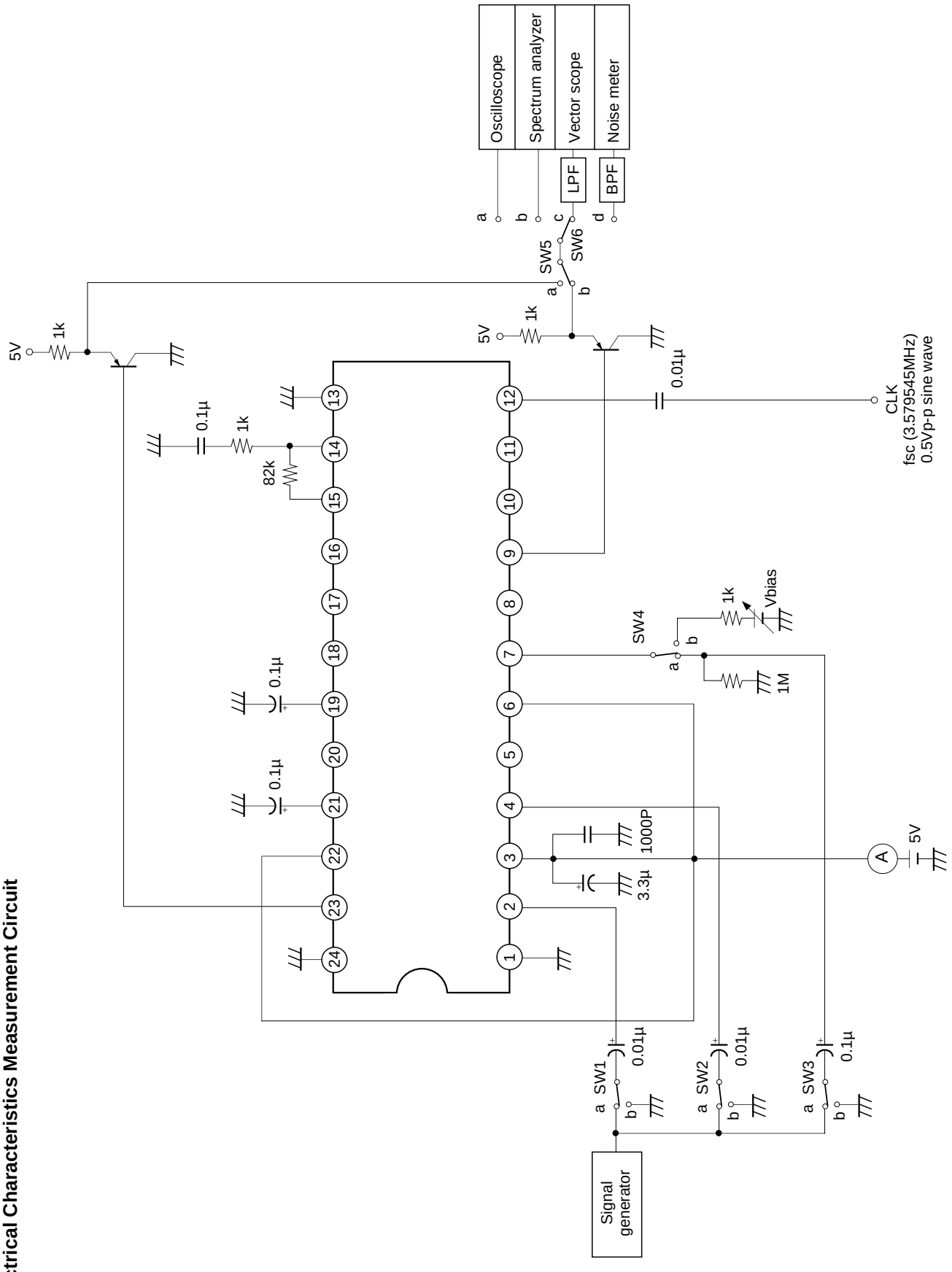
10. Input the 5-step staircase wave only for the luminance signal shown in the figure below, and measure the Y-OUT luminance level (Y) and SYNC level (S).



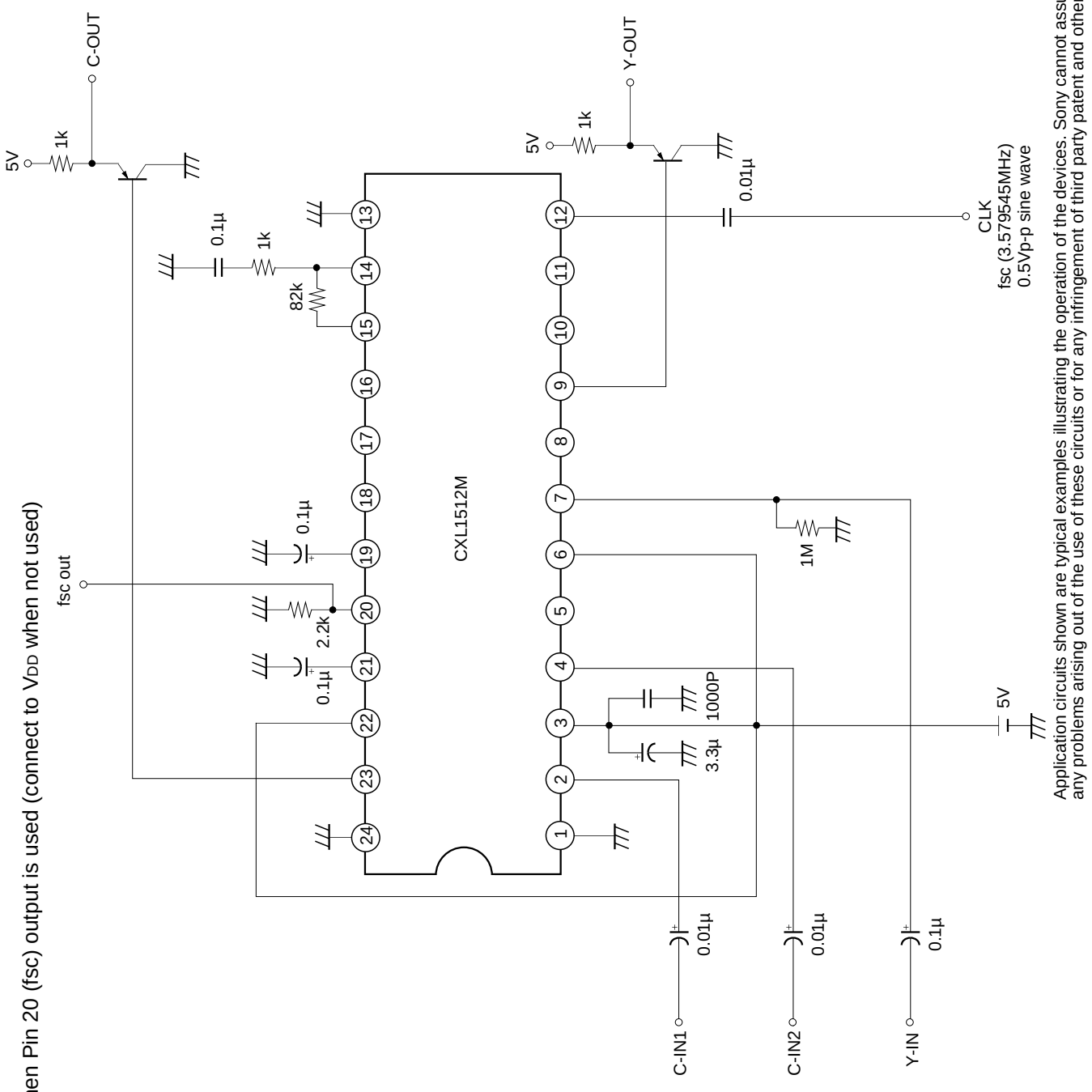
(Example of calculation)

$$LNY = \frac{S\ (mV)}{Y\ (mV)} \times 100$$

Electrical Characteristics Measurement Circuit



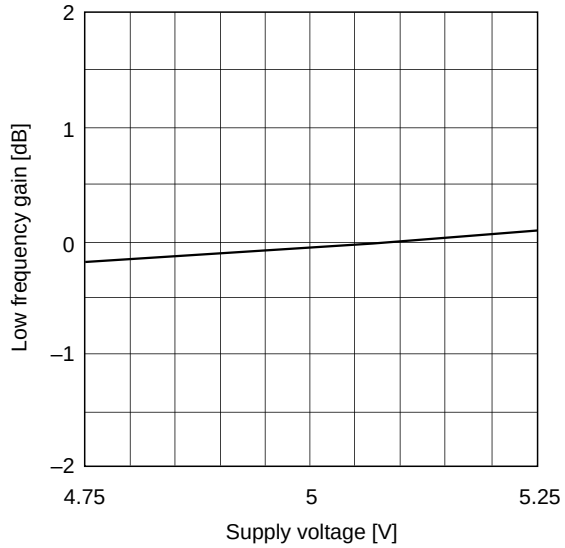
Application Circuit When Pin 20 (fsc) output is used (connect to V_{DD} when not used)



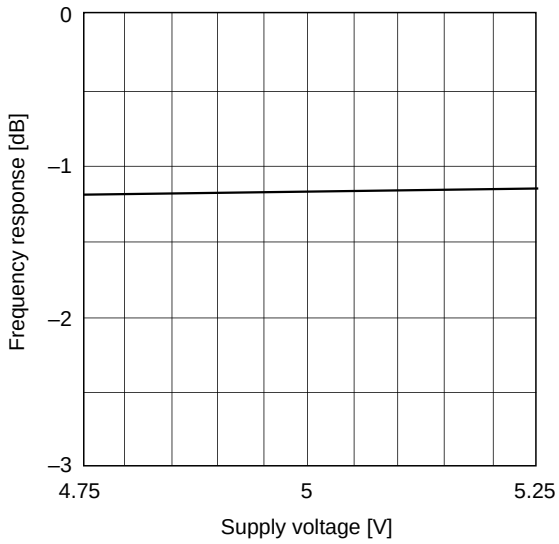
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

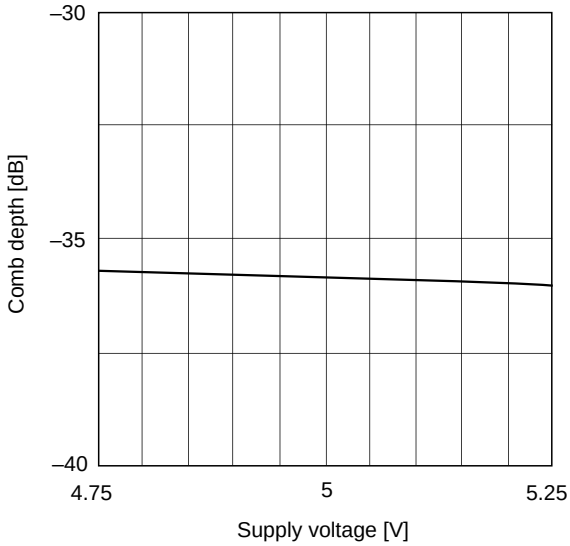
Low frequency gain vs. Supply voltage



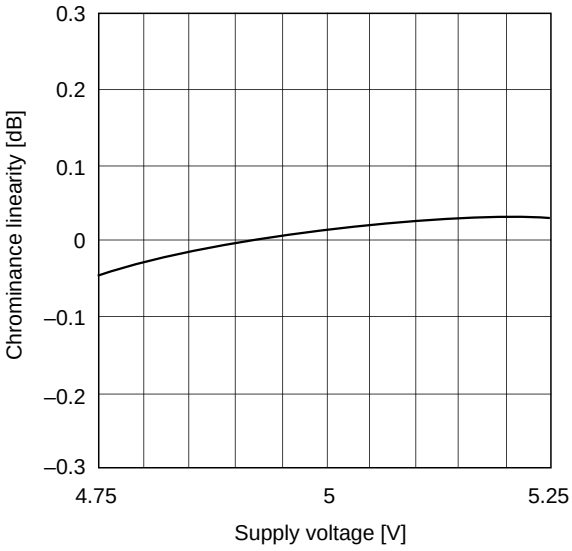
Frequency response vs. Supply voltage



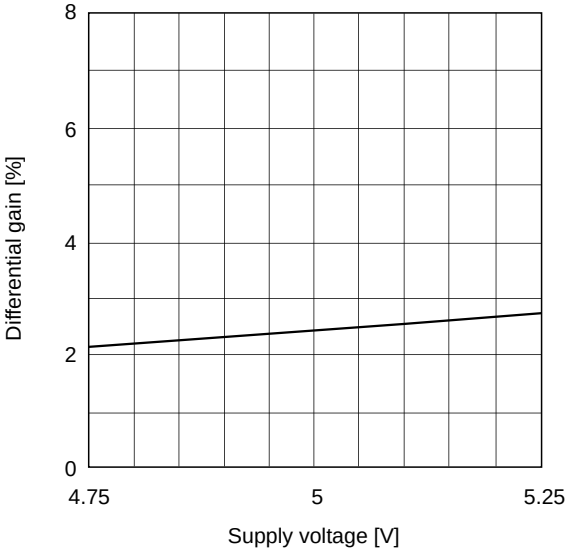
Comb depth vs. Supply voltage



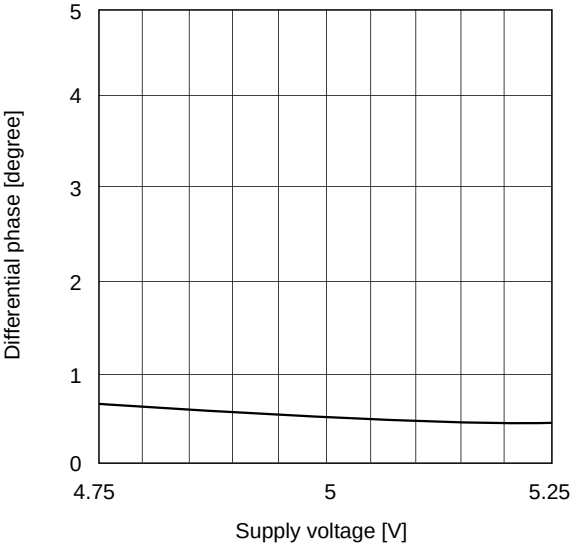
Chrominance linearity vs. Supply voltage



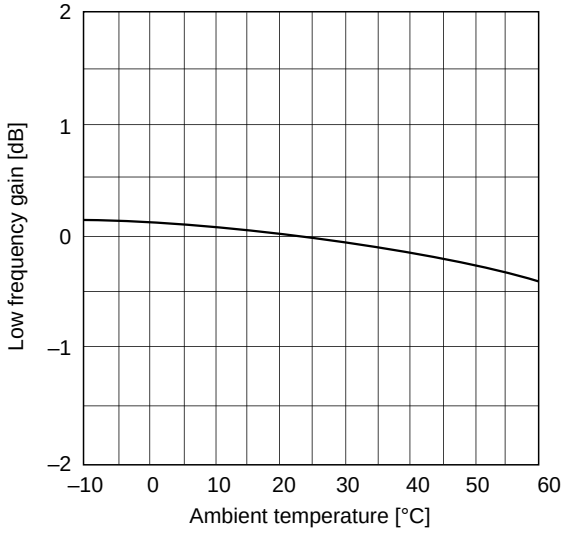
Differential gain vs. Supply voltage



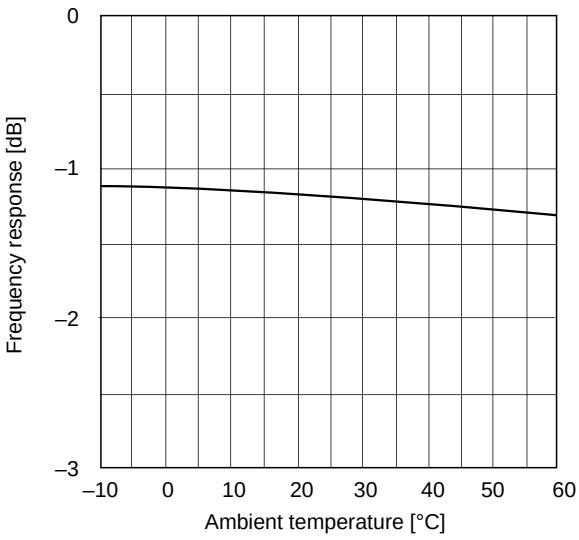
Differential phase vs. Supply voltage



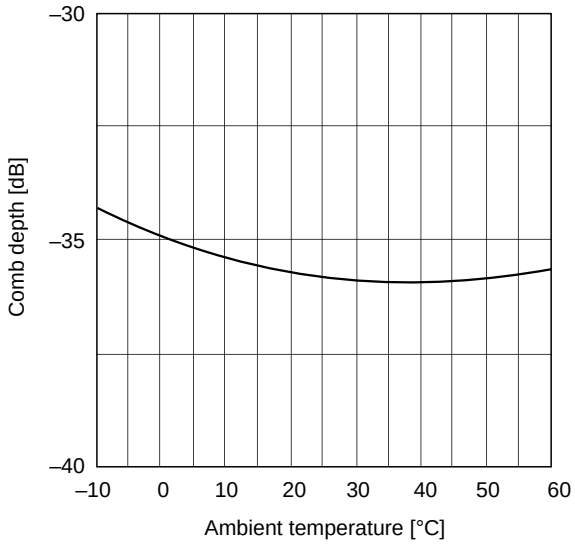
Low frequency gain vs. Ambient temperature



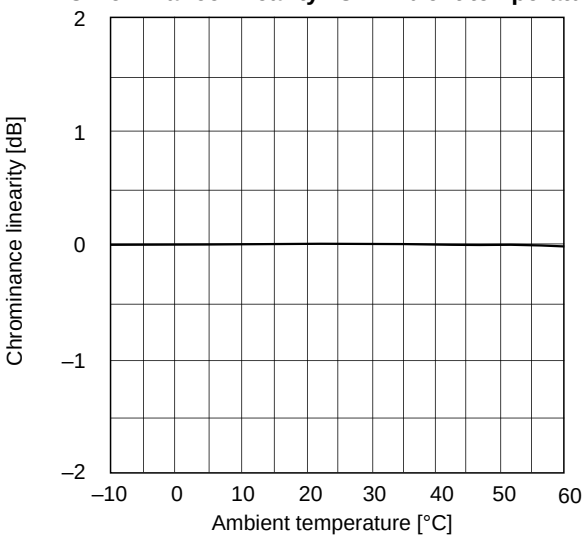
Frequency response vs. Ambient temperature



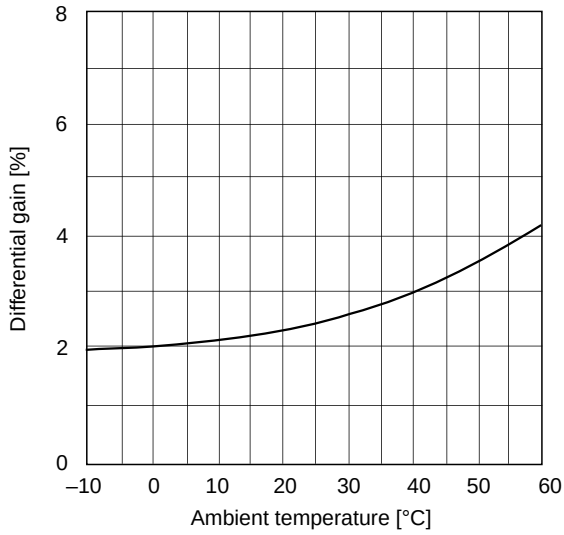
Comb depth vs. Ambient temperature



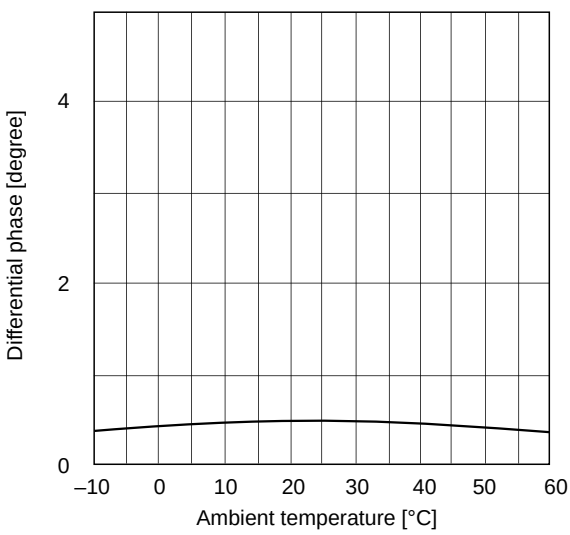
Chrominance linearity vs. Ambient temperature



Differential gain vs. Ambient temperature

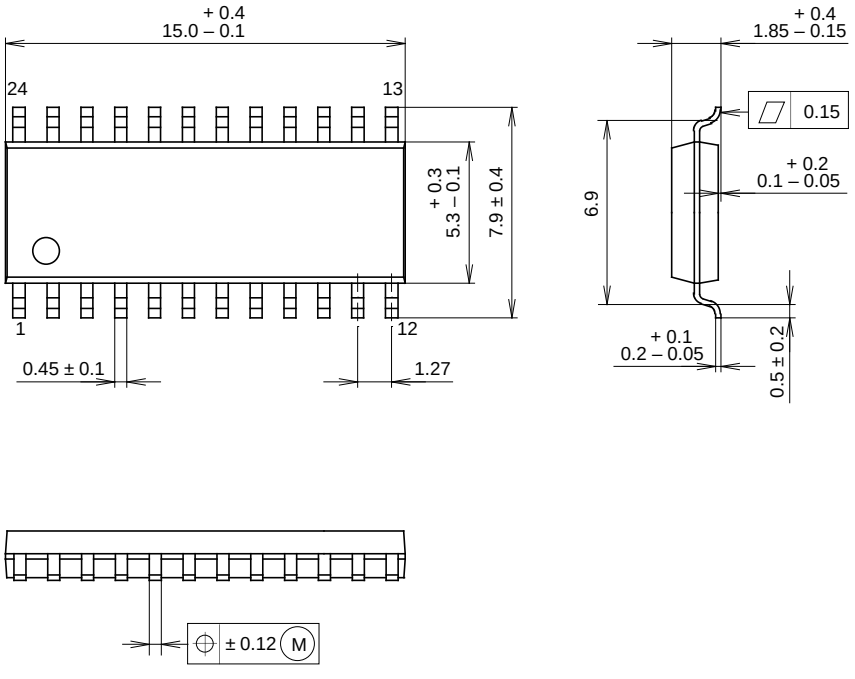


Differential phase vs. Ambient temperature



Package Outline Unit: mm

24PIN SOP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SOP-24P-L01
EIAJ CODE	∗SOP024-P-0300-A
JEDEC CODE	————

MOLDING COMPOUND	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY / 42ALLOY
PACKAGE WEIGHT	0.3g