

65,536-Word-by-18-Bit High-Speed CMOS Synchronous Static RAM Preliminary

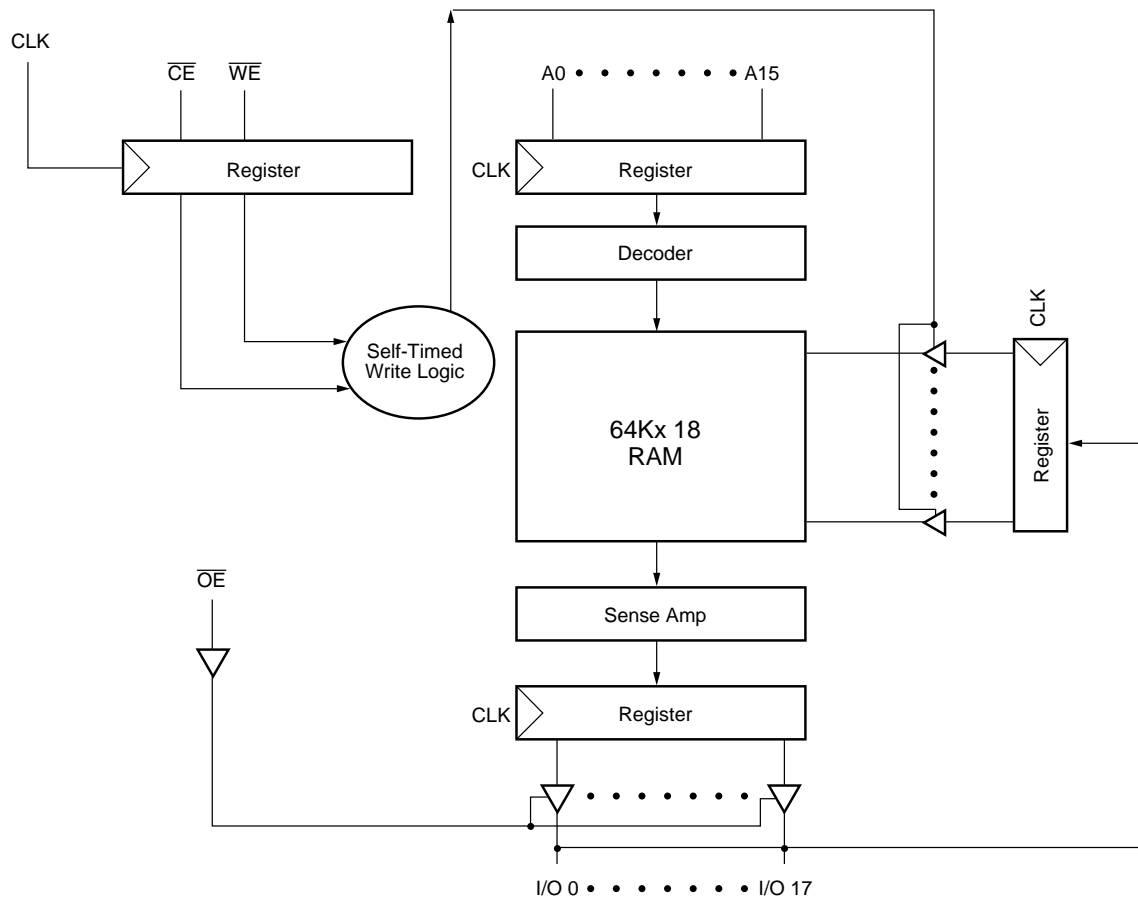
Description

The CXK77V1810GB/TM is a high-speed CMOS synchronous static RAM with common I/O pins, organized as 65,536-words-by-18-bits. This synchronous SRAM integrates input registers, high-speed SRAM and output registers onto a single monolithic IC. All input signals, except \overline{OE} , are latched at the positive edge of an external clock (CLK). The RAM data from the previous cycle is presented at the positive edge of the subsequent clock cycle. Write operation is initiated by the positive edge of CLK and is internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals. Asynchronous \overline{OE} adds the flexibility of data bus control. 100MHz operation is obtained from a single 3.3V power supply.

Features

- High speed, low power consumption
- Single +3.3V power supply: $3.3V \pm 5\%$
- Inputs and outputs are LVTTTL/LVCMOS-compatible
- Byte Select capability
- Asynchronous \overline{OE}
- Common data input and output
- 9ns cycle time (110MHz)
- All inputs (except \overline{OE}) and outputs are registered on a single clock edge
- Self-timed write cycle
- Package line-up:
 - GB: 7 x 17 Plastic Ball Grid Array with 50mil pitch
 - TM: 400mil, 50-pin TSOP II with .8mm pitch

Functional Block Diagram



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Pin Configuration (top view)

CXK77V1810GB

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|------|-----|-----------------|-----------------|-----------------|------|------|
| A | VDDQ | A0 | A2 | NC | A4 | A5 | VDDQ |
| B | NC | NC | NC | NC | NC | NC | NC |
| C | NC | A1 | A3 | VDD | A6 | A7 | NC |
| D | DQ8 | NC | VSS | NC | VSS | DQ9 | NC |
| E | NC | DQ7 | VSS | \overline{CE} | VSS | NC | DQ10 |
| F | VDDQ | NC | VSS | \overline{OE} | VSS | DQ11 | VDDQ |
| G | NC | DQ6 | \overline{LB} | NC | NC | NC | DQ12 |
| H | DQ5 | NC | VSS | NC | VSS | DQ13 | NC |
| J | VDDQ | VDD | NC | VDD | NC | VDD | VDDQ |
| K | NC | DQ4 | VSS | CLK | VSS | NC | DQ14 |
| L | DQ3 | NC | NC | NC | \overline{UB} | DQ15 | NC |
| M | VDDQ | DQ2 | VSS | \overline{WE} | VSS | NC | VDDQ |
| N | DQ1 | NC | VSS | A12 | VSS | DQ16 | NC |
| P | NC | DQ0 | VSS | A11 | VSS | NC | DQ17 |
| R | NC | A15 | NC | VDD | NC | A8 | NC |
| T | NC | A14 | A13 | NC | A10 | A9 | NC |
| U | VDDQ | NC | NC | NC | NC | NC | VDDQ |

CXK77V1810TM

| | | | |
|-----------------|------|----|--------------------|
| A ₄ | □ 1 | 50 | □ A ₅ |
| A ₃ | □ 2 | 49 | □ A ₆ |
| A ₂ | □ 3 | 48 | □ A ₇ |
| A ₁ | □ 4 | 47 | □ \overline{OE} |
| A ₀ | □ 5 | 46 | □ \overline{UB} |
| \overline{CE} | □ 6 | 45 | □ \overline{LB} |
| DQ ₈ | □ 7 | 44 | □ DQ ₉ |
| DQ ₇ | □ 8 | 43 | □ DQ ₁₀ |
| VDDQ | □ 9 | 42 | □ VDDQ |
| VSSQ | □ 10 | 41 | □ VSSQ |
| DQ ₆ | □ 11 | 40 | □ DQ ₁₁ |
| DQ ₅ | □ 12 | 39 | □ DQ ₁₂ |
| VDD | □ 13 | 38 | □ CLK |
| DQ ₄ | □ 14 | 37 | □ VSS |
| DQ ₃ | □ 15 | 36 | □ DQ ₁₃ |
| VSSQ | □ 16 | 35 | □ DQ ₁₄ |
| VDDQ | □ 17 | 34 | □ VDDQ |
| DQ ₂ | □ 18 | 33 | □ VSSQ |
| DQ ₁ | □ 19 | 32 | □ DQ ₁₅ |
| DQ ₀ | □ 20 | 31 | □ DQ ₁₆ |
| \overline{WE} | □ 21 | 30 | □ DQ ₁₇ |
| A ₁₅ | □ 22 | 29 | □ A ₈ |
| A ₁₄ | □ 23 | 28 | □ A ₉ |
| A ₁₃ | □ 24 | 27 | □ A ₁₀ |
| A ₁₂ | □ 25 | 26 | □ A ₁₁ |

Pin Description

| Symbol | Description | Symbol | Description |
|-------------|------------------------------|-----------------|-------------------------|
| A0 to A15 | Address input | CLK | Clock input |
| DQ0 to DQ8 | Lower Byte Data input/output | \overline{LB} | Lower Byte enable input |
| DQ9 to DQ17 | Upper Byte Data input/output | \overline{UB} | Upper Byte enable input |
| VDD | +3.3V power supply | \overline{CE} | Chip Enable input |
| VDDQ | +3.3 output power supply | \overline{WE} | Write Enable input |
| VSSQ | Output ground | \overline{OE} | Output Enable input |
| Vss | Ground | | |

Separate Vssq are available only in CXK77V1810TM.
 For proper operation, VDD ≥ VDDQ at all times, including power up.

Absolute Maximum Ratings

(Ta = +25°C, GND = 0V)

| Item | Symbol | Rating | Unit |
|------------------------------|---------|-------------------------------|----------|
| Supply voltage | VDD | -0.5 to +4.6 | V |
| Input voltage | VIN | -0.5 to Vcc + 0.5 (4.6V max.) | V |
| Output voltage | Vo | -0.5 to Vcc + 0.5 (4.6V max.) | V |
| Allowable power dissipation | Pd | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |
| Soldering temperature • time | Tsolder | 260 • 10 | °C • sec |

Truth Table

| \overline{CE} (tn) | \overline{WE} (tn) | \overline{UB} (tn) | \overline{LB} (tn) | \overline{OE} | Mode | DQ0-17 (tn) | DQ0-17 (tn+1) | VDD Current |
|-------------------------|-------------------------|-------------------------|-------------------------|-----------------|-------------------|----------------|------------------|----------------|
| H | X | X | X | X | Deselect | Don't care | Hi Z | ISB |
| L | H | X | X | H | Read, output Hi-Z | Don't care | Hi - Z | Icc |
| L | H | H | H | X | | | | |
| L | H | L | L | L | Read bits 0-17 | Don't care | DOUT(tn) | Icc |
| L | H | H | L | L | Read bits 0-8 | Don't care | DOUT(tn) | Icc |
| L | H | L | H | L | Read bits 9-17 | Don't care | DOUT(tn) | Icc |
| L | L | L | L | X | Write bits 0-17 | DIN(tn) | Hi-Z | Icc |
| L | L | H | L | X | Write bits 0-8 | DIN(tn) | Hi-Z | Icc |
| L | L | L | H | X | Write bits 9-17 | DIN(tn) | Hi-Z | Icc |

DC Recommended Operating Conditions

(Ta = +25°C, GND = 0V)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------|--------|--------|------|-------------|------|
| Supply voltage | VDD | 3.15 | 3.3 | 3.45 | V |
| Output supply voltage | VDDQ* | 3.15 | 3.3 | 3.45 | V |
| Input high voltage | VIH | 2.0 | — | VDD + 0.3** | V |
| Input low voltage | VIL | -0.3** | — | 0.8 | V |

*VDDQ must be \leq VDD at all times, including power up.

**VIL = -1.5V min. and VIH = VDD + 1.5V for pulse width less than 5ns.

Electrical Characteristics

DC and Operating Characteristics

(VCC = 3.3V \pm 10%, GND = 0V, Ta = 0 to = +70°C)

| Item | Symbol | Test Conditions | Min. | Typ* | Max. | Unit |
|--------------------------------|--------|---|------|------|------|---------|
| Input leakage current | ILI | VIN = GND to VDD | -1 | — | 1 | μ A |
| Output leakage current | ILO | VO = GND to VCC \overline{OE} = VIH | -1 | — | 1 | μ A |
| Operating power supply current | IDD | Cycle = min. Duty = 100% IOUT = 0mA | — | — | 220 | mA |
| Standby current | ISB | $\overline{CE} \geq$ VIH Cycle = min. Duty = 100% IOUT = 0mA | — | — | 150 | mA |
| Output high voltage | VOH | IOH = -2.0mA | 2.4 | — | — | V |
| Output low voltage | VOL | IOL = 2.0mA | — | — | 0.4 | V |

*VCC = 3.3V, Ta = +25°C

I/O Capacitance

(Ta = +25°C, f = 1MHz)

| Item | Symbol | Test Conditions | Min. | Max. | Unit |
|--------------------|--------|-----------------|------|------|------|
| Input capacitance | CIN | VIN = 0V | — | 5 | pF |
| Output capacitance | COUT | VOUT = 0V | — | 7 | pF |

Note: These parameters are sampled and are not 100% tested.

AC Electrical Characteristics

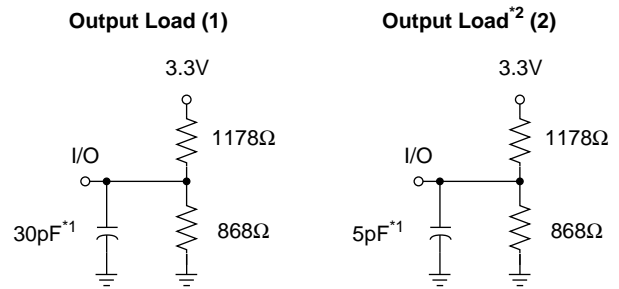
| Item | Symbol | -9 | | -10 | | -12 | | Unit |
|--|--------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Clock period | tCP | 9 | — | 10 | — | 12.5 | — | ns |
| Clock pulse high | tCH | 3.5 | — | 4 | — | 4 | — | ns |
| Clock pulse low | tCL | 3.5 | — | 4 | — | 4 | — | ns |
| Setup time | tS | 2.0 | — | 2.5 | — | 2.5 | — | ns |
| Hold time | tH | 0.5 | — | 0.5 | — | 0.5 | — | ns |
| Clock to output | tCQ | 2 | 5.5 | 2 | 6 | 2 | 7 | ns |
| Clock to output high impedance | tHZ*2 | — | 5.5 | — | 6 | — | 6 | ns |
| Clock to output low impedance | tLZ*2 | 2 | — | 2 | — | 2 | — | ns |
| \overline{OE} to output | tOE | 1 | 5 | 1 | 5 | 1 | 6 | ns |
| \overline{OE} to output high impedance | tOHZ*2 | — | 4.5 | — | 5 | — | 5 | ns |
| \overline{OE} to output low impedance | tOLZ*2 | 1 | — | 1 | — | 1 | — | ns |

1. All parameters are specified over the range 0 to +70°C.
2. These parameters are sampled and are not 100% tested.

AC Characteristics

AC Test Conditions (VDD = 3.3V ± 5%, Ta = 0 to +70°C)

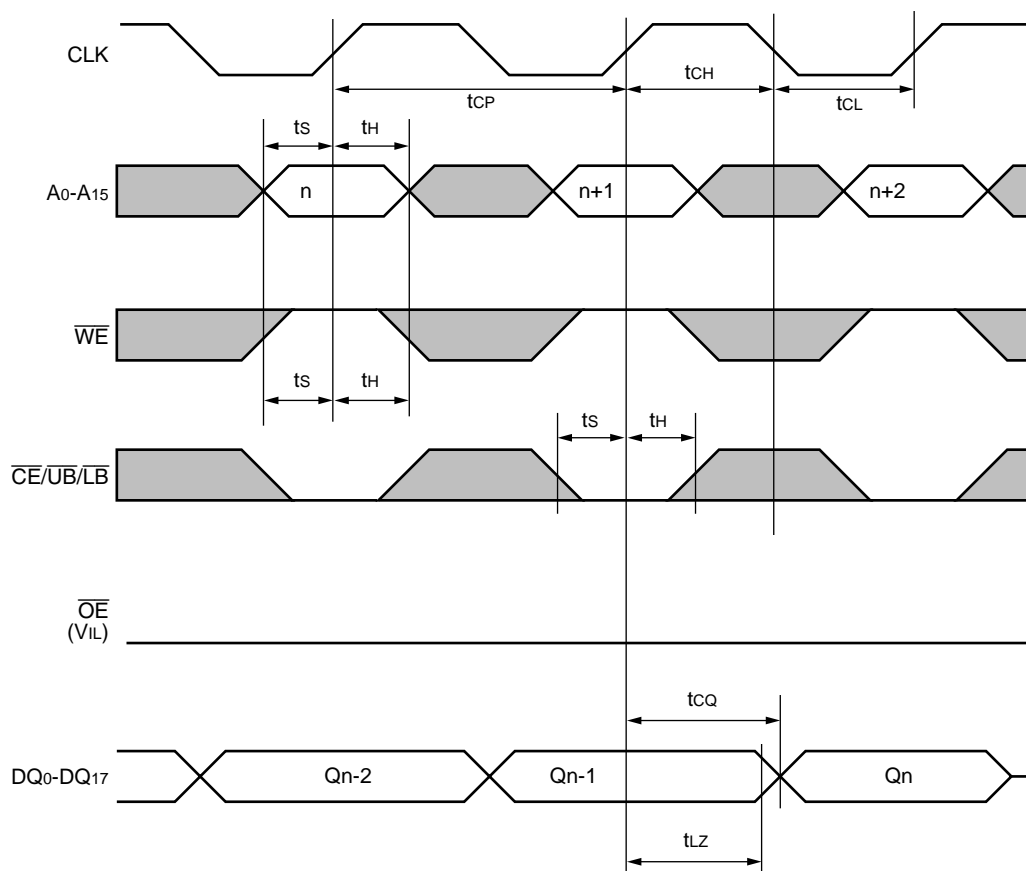
| Item | Conditions |
|------------------------|------------------------|
| Input pulse high level | V _{IH} = 2.4V |
| Input pulse low level | V _{IL} = 0.4V |
| Input rise time | t _r = 2ns |
| Input fall time | t _f = 2ns |
| Input reference level | 1.4V |
| Output reference level | 1.4V |
| Output load conditions | Figure 1 |



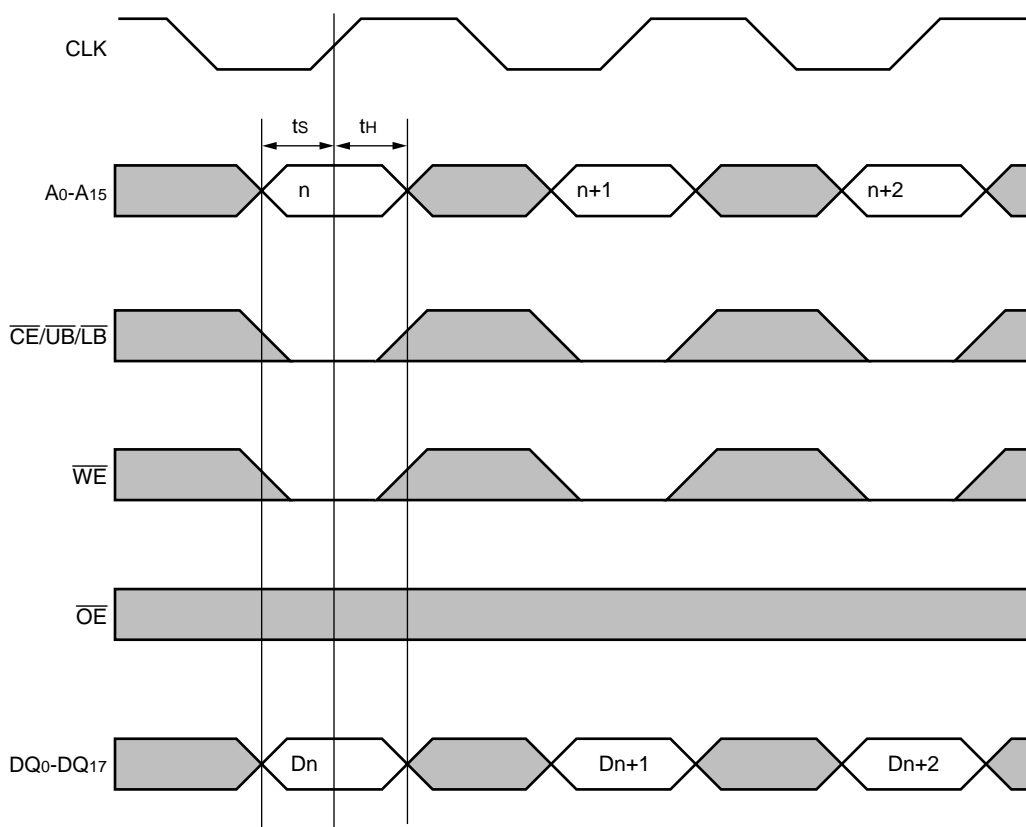
- *1. Including scope and jig capacitance.
- *2. For tLZ, tHZ

Figure 1

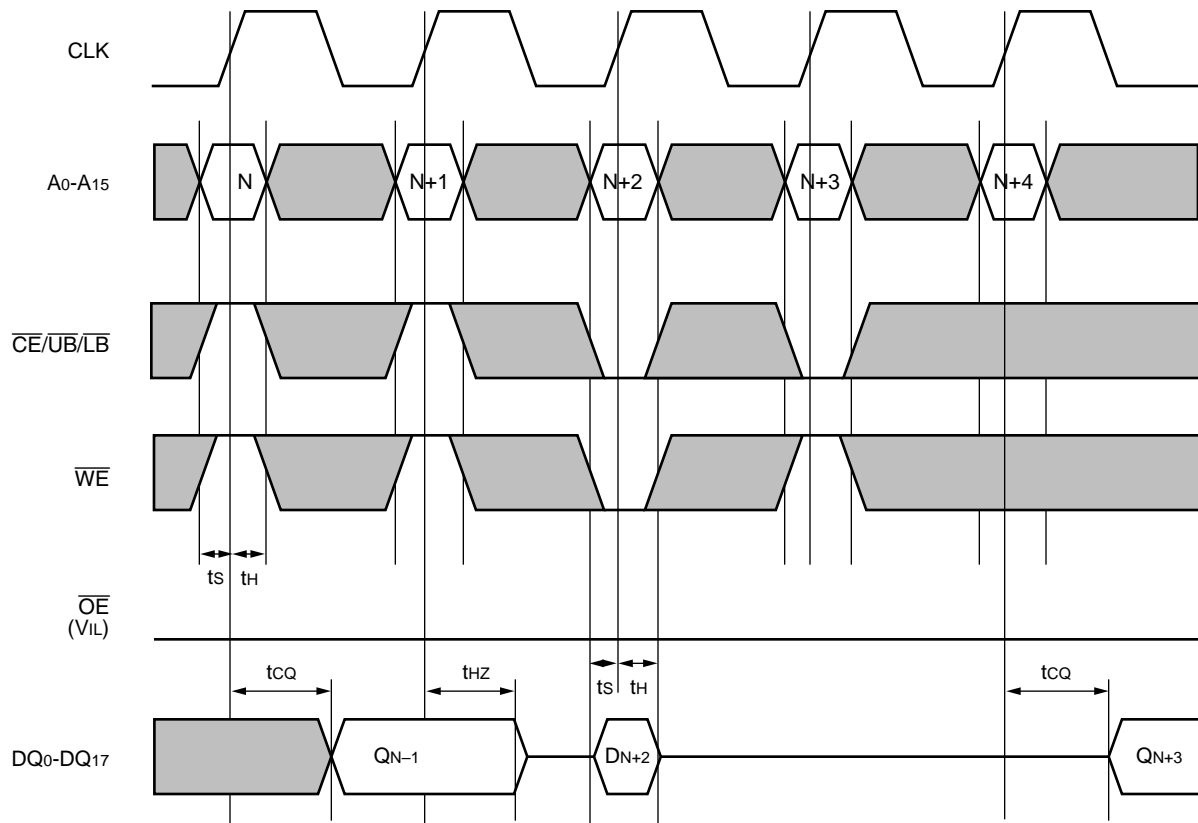
Timing Waveform of Read Cycle



Timing Waveform of Write Cycle



Timing Waveform of Read-Write-Read Cycle I ($\overline{CE}/\overline{UB}/\overline{LB}$ Control)



Timing Waveform of Read-Write-Read Cycle II (\overline{OE} Control)

