

8-bit 3-channel 50 MSPS Video A/D Converter with clamp function

Description

The CXD2303AQ is an 8-bit 3-channel CMOS A/D converter for video with synchronizing digital clamp function. The adoption of 2 step-parallel method achieves low power consumption and a maximum conversion rates of 50 MSPS.

Features

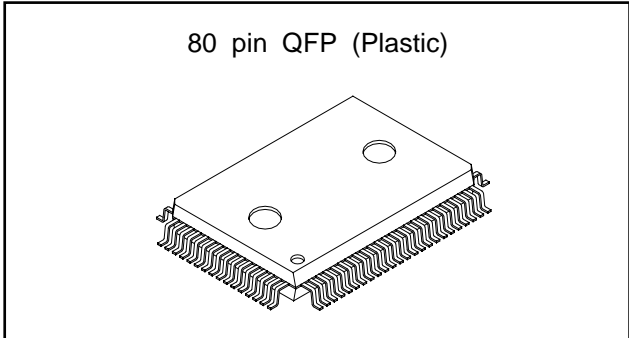
- Resolution : 8 bit±1/2 LSB (DL)
- Maximum sampling frequency : 50 MSPS
- Low power consumption : 400 mW (at 50 MSPS Typ.) (Reference current excluded)
- Synchronizing digital clamp function
- Clamp ON/OFF function
- Reference voltage self-bias circuit
- Input CMOS/TTL compatible
- 3-state TTL compatible output
- Single 5 V power supply or dual 5 V/3.3 V power supplies
- Low input capacitance 15 pF
- Reference impedance : 370 Ω (Typ.)
- Different digital output multiplex format:
 - 4 : 4 : 4 format
 - 4 : 2 : 2 format
 - 4 : 1 : 1 format

Applications

Wide range of applications that require high-speed A/D conversion such as monitor, TV and VCR.

Structure

Silicon gate CMOS IC



Absolute Maximum Ratings (Ta=25 °C)

- Supply voltage

AVDD, DVDD	7	V
------------	---	---
- Input voltage Vin

Digital output pins	DVDD+0.5 to DVSS–0.5	V
Other pins	AVDD+0.5 to AVSS–0.5	V
- Storage temperature

Tstg	–55 to +150	°C
------	-------------	----

Recommended Operating Conditions

- Supply voltage

AVDD, AVSS	4.75 to 5.25	V
DVDD, DVSS	3.0 to 5.5	V
DVSS–AVSS	0 to 100	mV
- Reference input voltage

VARB, VBRB, VCRB	0 or more	V
VART, VBRT, VCRT	2.7 or less	V
- Analog input

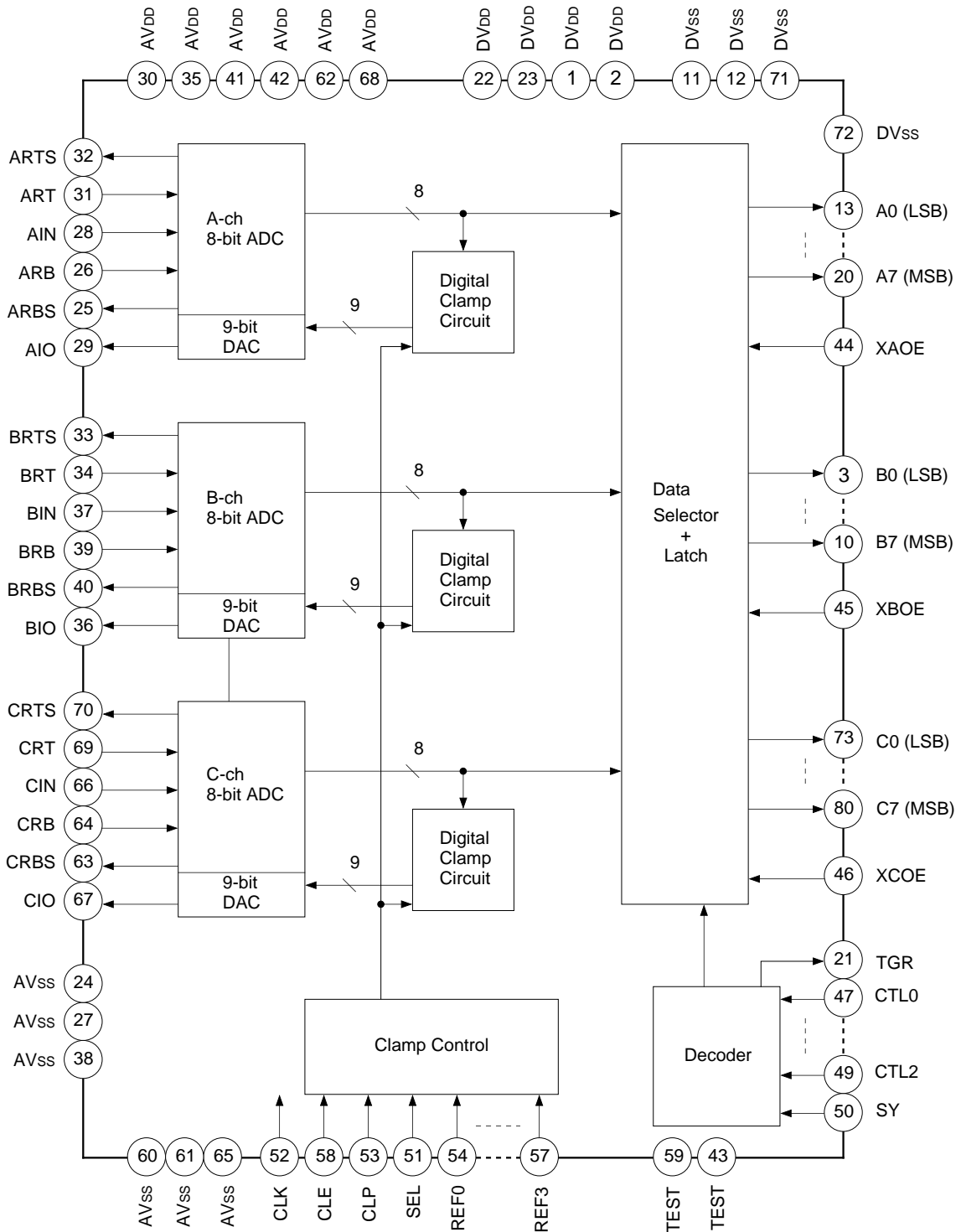
AIN, BIN, CIN	1.7 Vp-p or more	
---------------	------------------	--
- Clock pulse width

Tpw1, Tpw0	9 ns (min.) to 1.1 μs (max.)	
------------	------------------------------	--
- Operating ambient temperature

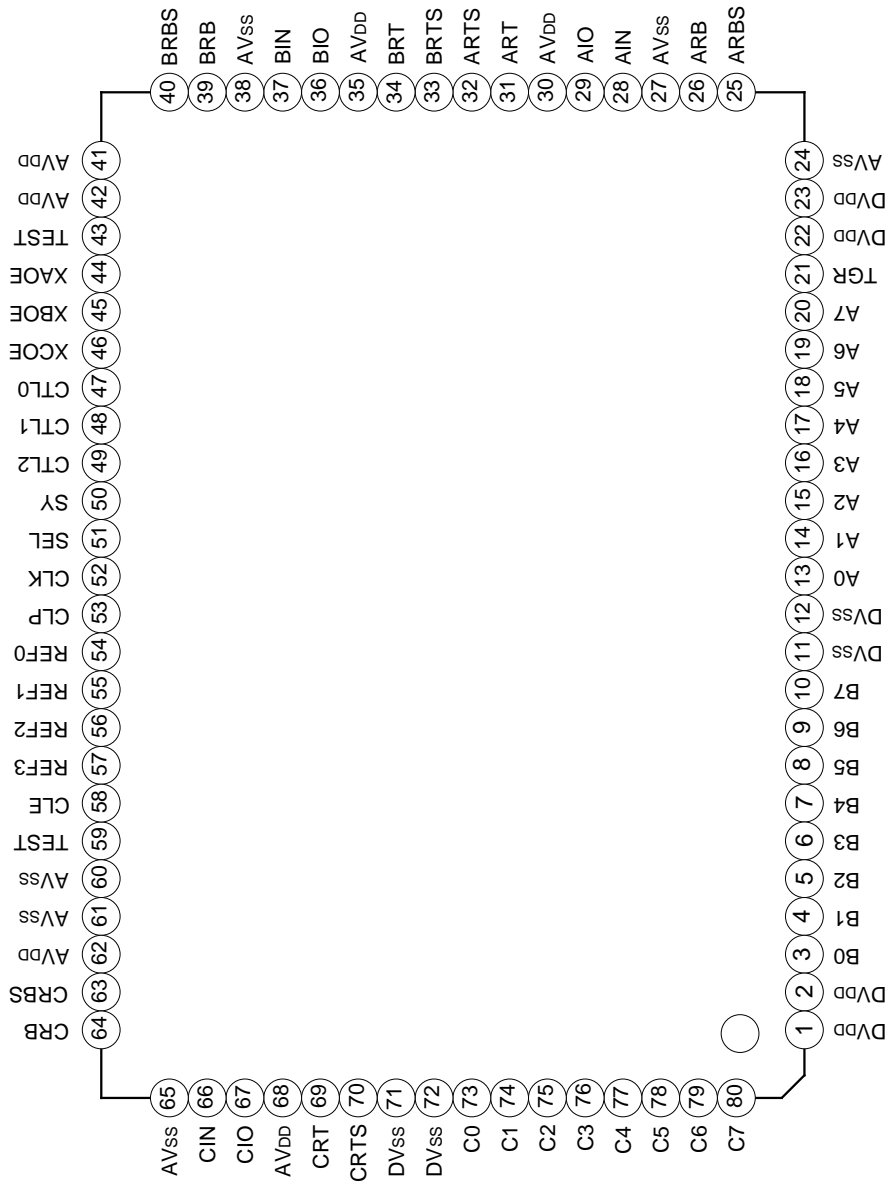
Topr	–40 to +85	°C
------	------------	----

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
1, 2, 22, 23	DVDD	—		Digital power supply. +5 V or +3.3 V
13 to 20 3 to 10 73 to 80	A0 to A7 B0 to B7 C0 to C7	O		Digital output. A0 (LSB) to A7 (MSB) B0 (LSB) to B7 (MSB) C0 (LSB) to C7 (MSB)
21	TGR	O		Trigger output. See the Tables and Timing Chart II described in the Output Format section.
11, 12, 71, 72	DVSS	—		Digital ground.
24, 27, 38, 60, 61, 65	AVSS	—		Analog ground.
25 40 63	ARBS BRBS CRBS	—		Shorting these pins to AVSS generates voltage of about 0.5 V at the ARB, BRB and CRB pins.
26 39 64	ARB BRB CRB	—		Reference voltage (bottom).
31 34 69	ART BRT CRT	—		Reference voltage (top).
32 33 70	ARTS BRTS CRTS	—		Shorting these pins to AVDD generates voltage of about 2.5 V at the ART, BRT and CRT pins.
28 37 66	AIN BIN CIN	I		

Pin No.	Symbol	I/O	Equivalent circuit	Description
29 36 67	AIO BIO CIO	O		<p>Analog output.</p> <p>The digital clamp circuit comprises a D/A converter whose outputs are available on these pins.</p>
30, 35, 41, 42, 62, 68	AVDD			Analog +5 V power supply.
43 59	TEST	I		<p>Normally open.</p> <p>Pull-down resistors are incorporated.</p>
44 45 46	XAOE XBOE XCOE	I		<p>Output enable input.</p> <p>When these pins are Low, data is output from the digital output pins. When these pins are High, the digital output pins are high impedance.</p> <p>The A, B and C channels can be controlled separately.</p> <p>Also, these pins are not synchronized with the clock signal.</p> <p>Pull-down resistors are incorporated.</p>
47 48 49	CTL0 CTL1 CTL2	I		<p>Determines the digital output mode. See the Mode Tables and Timing Charts.</p> <p>Pull-down resistors are incorporated.</p>
50	SY	I		<p>Controls the digital output mode switching timing. The mode is switched by detecting the transition point where this pin changes from Low to High. See the Mode Tables and Timing Charts for details.</p> <p>A pull-down resistor is incorporated.</p>

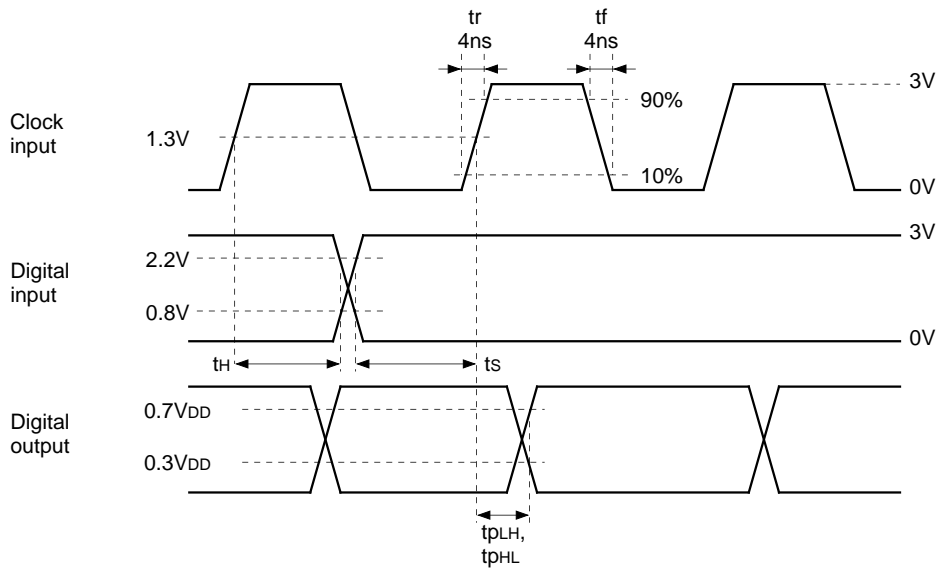
Pin No.	Symbol	I/O	Equivalent circuit	Description
51	SEL	I		<p>Controls the CLP signal polarity. When this pin is Low, CLP is High active. When this pin is High, CLP is Low active. This pin has a built-in pull-down resistor.</p>
52	CLK	I		<p>Clock input. A pull-down resistor is incorporated.</p>
53	CLP	I		<p>Clamp pulse input. The polarity can be set to either High or Low by setting SEL. This pin has a built-in pull-down resistor.</p>
54 55 56 57	REF0 REF1 REF2 REF3	I		<p>Determines the clamp circuit reference data. See the Mode Tables for the set data. These pins are not synchronized with the clock input signal. Pull-down resistors are incorporated.</p>
58	CLE	I		<p>Clamp enable. When this pin is Low, the clamp circuit does not operate. When this pin is High, the clamp circuit operates. A pull-down resistor is incorporated.</p>

Digital output

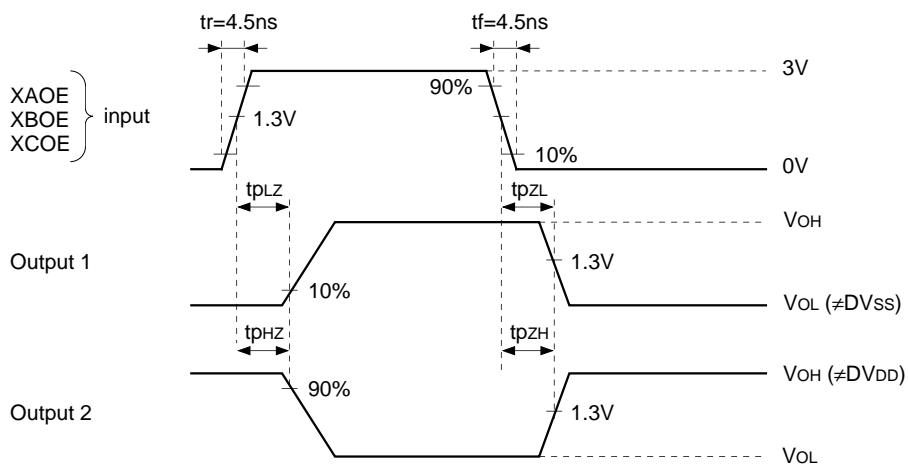
The following table shows the relationship between analog input voltage and digital output code.

Input signal voltage	Step	Digital output code	
		MSB	LSB
V _{ART} , V _{BRT} , V _{CRT}	0	1 1 1 1 1 1 1 1	
:	:		:
:	127	1 0 0 0 0 0 0 0	
:	128	0 1 1 1 1 1 1 1	
:	:		:
V _{ARB} , V _{BRB} , V _{CRB}	255	0 0 0 0 0 0 0 0	

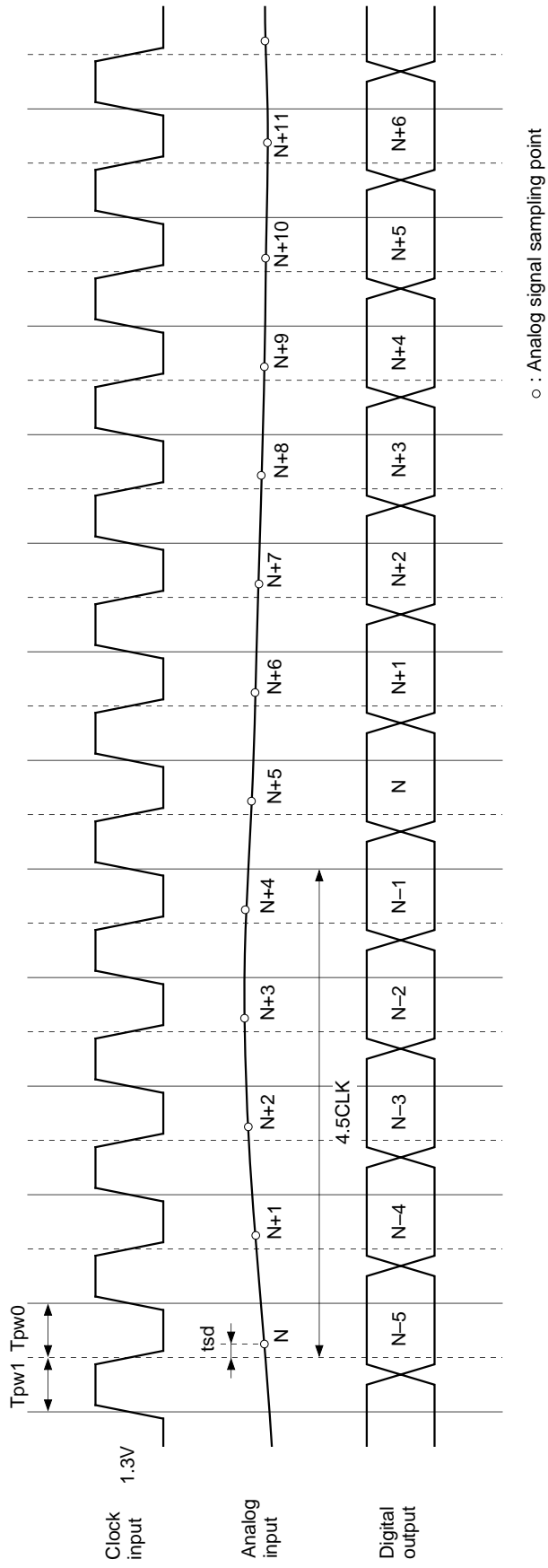
Timing Chart I



Timing Chart I-1.



Timing Chart I-2.



Timing Chart I-3



Electrical Characteristics

Analog characteristics (Fc=50 MSPS, AVDD=5 V, DVDD=3 to 5.5 V, VRB=0.5 V, VRT=2.5 V, Ta=25 °C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Conversion rate	Fc	AVDD=4.75 to 5.25 V Ta=-40 to +85 °C VIN=0.5 to 2.5 V FIN=1 kHz triangular wave		0.5		50	MSPS
Analog input band width	BW	Envelop	-1 dB		60		MHz
		RIN=33 Ω	-3 dB		100		
Differential non-linearity error	ED	End point			±0.3	±0.5	LSB
Integral non-linearity error	EL				±0.7	±1.5	
Offset voltage (*1)	EOT	Potential difference to ART, BRT, CRT		-50		-10	mV
	EOB	Potential difference to ARB, BRB, CRB		0		40	
Differential gain error	DG	NTSC 40 IRE mod ramp, Fc=14.3 MSPS			3		%
Differential phase error	DP				1.5		deg
Sampling delay	tsd				3		ns
Clamp offset voltage	Eoc	VIN=DC CIN=10 μF tpcw=2.75 μs Fc=14.3 MHz FCLP=15.75 kHz	Ref. Data= "00010000"			±1	LSB
			Ref. Data= "10000000"			±1	
Full-scale input ratio (*2)						0.5	%
Signal-to-noise ratio	SNR	FIN=150 kHz			43		dB
		FIN=500 kHz			42		
		FIN=1 MHz			42		
		FIN=3 MHz			41		
		FIN=10 MHz			38		
		FIN=20 MHz			35		
Spurious free dynamic range	SFDR	FIN=150 kHz			59		dB
		FIN=500 kHz			59		
		FIN=1 MHz			55		
		FIN=3 MHz			49		
		FIN=10 MHz			44		
		FIN=20 MHz			41		
Cross talk	CT	FIN=1 MHz sin wave			52		dB

(*1) The offset voltage EOB is a potential difference between ARB, BRB, CRB and a point of position where the voltage drops equivalent to 1/2 LSB of the voltage when the output data changes from "00000000" to "00000001". EOT is a potential difference between ART, BRT, CRT and a potential of point where the voltage rises equivalent to 1/2 LSB of the voltage when the output data changes from "11111111" to "11111110".

$$(*2) \text{ Full-scale input ratio} = \left| \frac{(2 V + E_{OT} - E_{OB}) \text{ of each channel}}{\text{Average of } (2 V + E_{OT} - E_{OB}) \text{ of each channel}} - 1 \right| \times 100 (\%)$$

DC characteristics (F_C=50 MSPS, AV_{DD}=5 V, DV_{DD}=5 V or 3.3 V, V_{RB}=0.5 V, V_{RT}=2.5 V, T_a=25 °C)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply current	I _{AD+IDD}	NTSC ramp wave input CLE=High F _{CLP} =15.75 kHz	DV _{DD} =5 V		80	100	mA
			DV _{DD} =3.3 V		70	90	
	I _{AD}	NTSC ramp wave input CLE=Low	DV _{DD} =5 V		70	90	
			DV _{DD} =3.3 V		60	80	
	I _{DD}	NTSC ramp wave input CLE=Low	DV _{DD} =5 V		5	10	
			DV _{DD} =3.3 V		5	10	
Reference current	I _{REF}	For every channel		4.1	5.4	7.7	mA
Reference resistance (RT to RB)	R _{REF}	For every channel		260	370	480	Ω
Self-bias	V _{RB1}	Shorts AV _{SS} and ARBS, BRBS, CRBS.		0.50	0.54	0.58	V
	V _{RT1-V_{RB1}}	Shorts AV _{DD} and ARTS, BRTS, CRTS.		1.80	1.92	2.04	
Analog input resistance	R _{IN}	AIN, BIN, CIN	F _C =50 MHz		13		kΩ
			F _C =35 MHz		16		
			F _C =20 MHz		30		
Input capacitance	C _{AI1}	AIN, BIN, CIN, V _{IN} =1.5 V+0.07 V _{rms}			15		pF
	C _{AI2}	ARTS, ART, ARB, ABFS, BRTS, BRT, BRB, BRBS, CRTS, CRT, CRB, CRBS				9	
	C _{DIN}	Digital input pin				9	
Output capacitance	C _{AO}	AIO, BIO, CIO				11	pF
	C _{DO}	Digital output pin				11	
Digital input voltage	V _{IH}	AV _{DD} =4.75 to 5.25 V DV _{DD} =3 to 5.5 V		2.2			V
	V _{IL}	T _a =-40 to +75 °C				0.8	
Digital input current	I _{IH}	V _I =0 V to AV _{DD}		-40		240	μA
	I _{IL}	T _a =-40 to +75 °C					
Digital output current	I _{OH}	XOE=0 V DV _{DD} =5 V	VOH=DV _{DD} -0.8 V			-2	mA
	I _{OL}	T _a =-40 to 75 °C	VOL=0.4 V	4			
	I _{OH}	XOE=0 V DV _{DD} =3.3 V	VOH=DV _{DD} -0.8 V			-1.2	
	I _{OL}	T _a =-40 to 75 °C	VOL=0.4 V	2.4			
	I _{OZH}	XOE=3 V DV _{DD} =3 to 5.5 V	VOH=DV _{DD}	-40		40	μA
	I _{OZL}	T _a =-40 to 75 °C	VOL=0 V				

DC Characteristic (Continue)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Digital output voltage	V _{OH}	XOE=0 V DV _{DD} =5 V	I _{OH} =-2 mA	DV _{DD} -0.8			V
	V _{OL}	Ta=-20 to 75 °C	I _{OL} =4 mA			0.4	
	V _{OH}	XOE=0 V DV _{DD} =3.3 V	I _{OH} =-1.2 mA	DV _{DD} -0.8			
	V _{OL}	Ta=-20 to 75 °C	I _{OL} =2.4 mA			0.4	

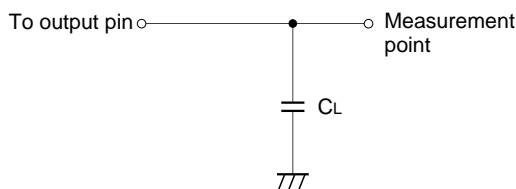
Timing

(F_C=50 MSPS, AV_{DD}=5 V, DV_{DD}=5 V or 3.3 V, V_{RB}=0.5 V, V_{RT}=2.5 V, Ta=25 °C)

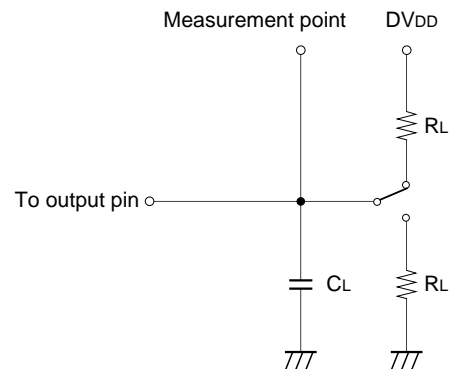
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output data delay	t _{PLH}	C _L =15 pF XOE=0 V	DV _{DD} =5 V	4.5	8.5	11.0	ns
	t _{PHL}				7.4		
	t _{PLH}		DV _{DD} =3.3 V	3.8	10.0	13.8	
	t _{PHL}				6.7		
Tri-state output enable time	t _{pZH}	R _L =1 kΩ C _L =15 pF	DV _{DD} =5 V	4.2	7.1	11.3	ns
	t _{pZL}				8.0		
	t _{pZH}		DV _{DD} =3.3 V	3.5	8.4	12.8	
	t _{pZL}				7.2		
Tri-state output disable time	t _{PHZ}	R _L =1 kΩ C _L =15 pF	DV _{DD} =5 V	3.6	6.8	9.5	ns
	t _{PLZ}				6.3		
	t _{PHZ}		DV _{DD} =3.3 V	2.9	6.8	10.5	
	t _{PLZ}				6.0		
Setup time	t _s	CTL0 to 2, CLP, SY		3.5			ns
Hold time	t _h			4.5			ns
Pulse width	t _H	CLK conversion	CLP	2			Cycle
			SY	1			

Electrical Characteristics Measurement Circuit

Output data delay measurement circuit



Tri-state output measurement circuit

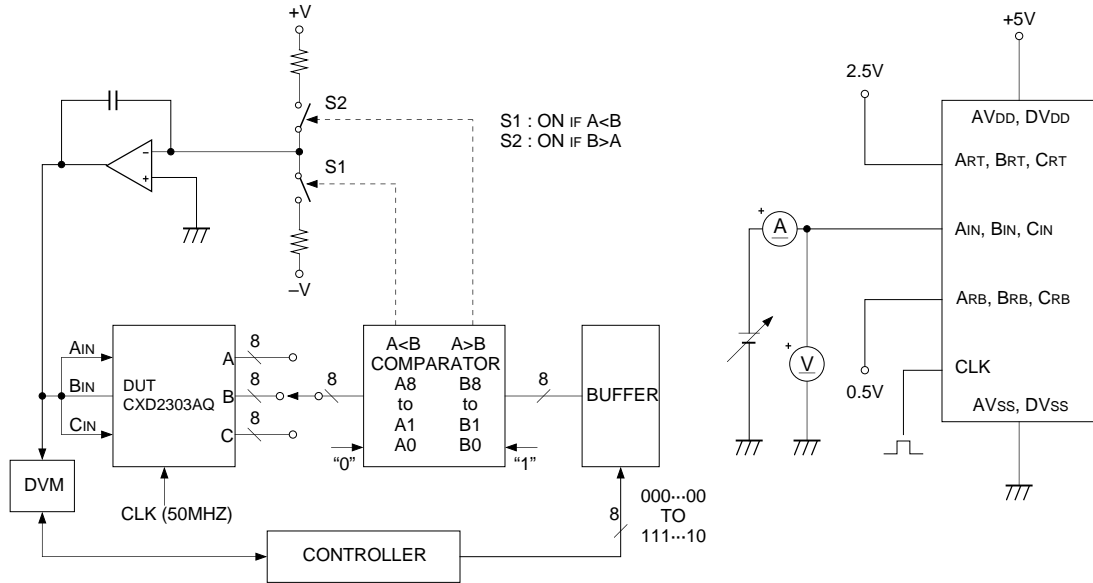


Note) C_L includes capacitance of probes.

Integral non-linearity error
 Differential non-linearity error
 Offset voltage

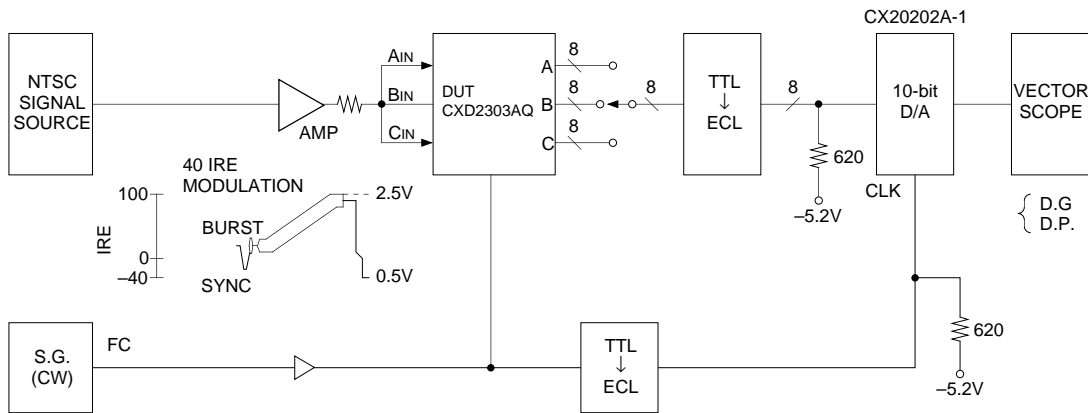
measurement circuit

Analog input resistance measurement circuit

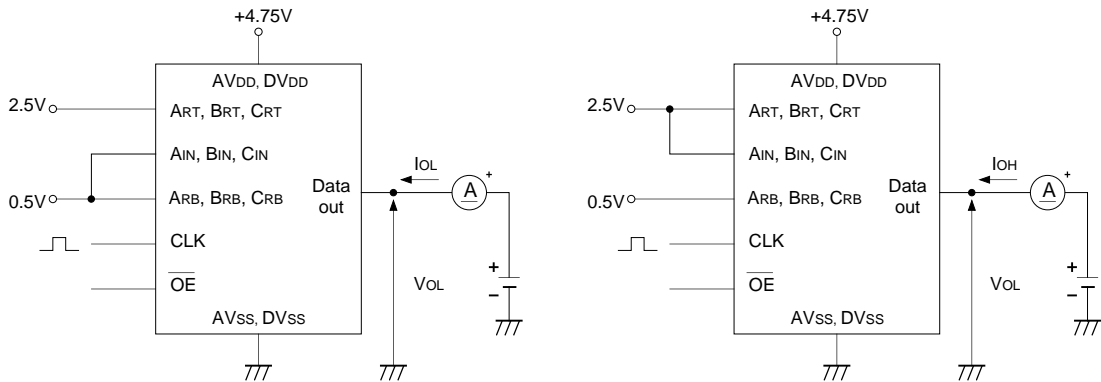


Differential gain error
 Differential phase error

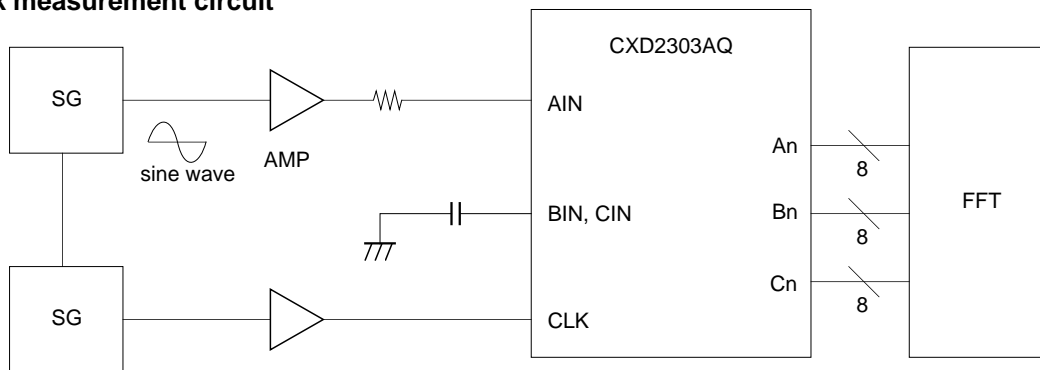
measurement circuit



Digital output current measurement circuit



Cross talk measurement circuit



Note : This diagram shows the case where the channel A is measured.
The same as for measuring the channels B and C.

Description of Operation

1. Output Format

The CXD2303AQ can select six different types of output formats through a combination of the CTL0, CTL1 and CTL2 inputs as shown in the table below. Output is synchronized to the SY input signal transition from Low to High.

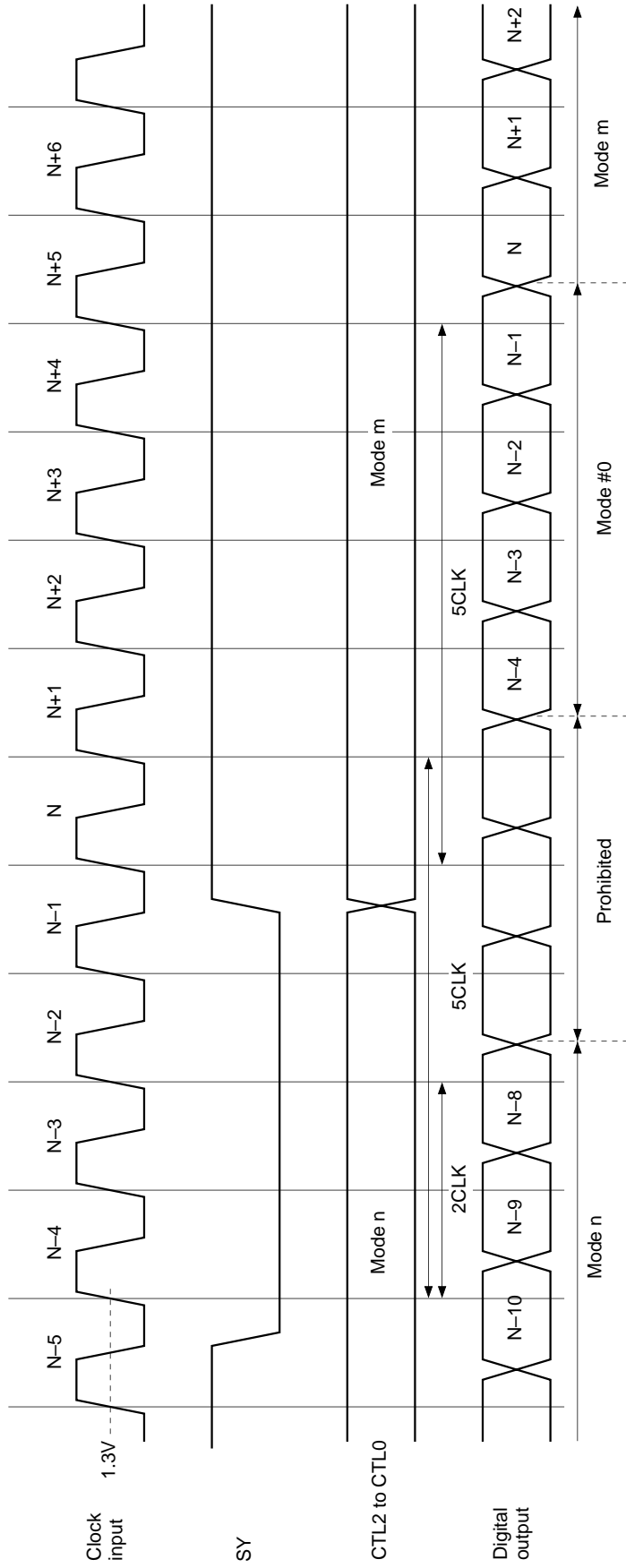
Table 1. Setting values and output formats

Setting			Output	
CTL2	CTL1	CTL0	Mode	Format
L	L	L	0	4 : 4 : 4
L	L	H	1	4 : 2 : 2 (8 fs)
L	H	L	2	4 : 2 : 2 (D2)
L	H	H	3	4 : 2 : 2 (Special)
H	L	L	4	4 : 1 : 1
H	L	H	5	4 : 1 : 1 (Special)
H	H	L	6	Simple boundary scan 1
H	H	H	7	Simple boundary scan 2

Note that when the SY input is open or Low level, the output format is mode #0 (4 : 4 : 4).

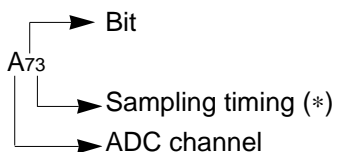
However, when the SY input signal temporarily goes to Low level for the mode switching, the mode changes as shown in Timing Chart II. When digital data is being output in the mode n output format, if the SY input signal changes from High level to Low level, the digital data continues to be output in the mode n output format for the following two clocks. The output format for the digital data output from the third to fifth clocks is not established, so its use is prohibited. If the SY input signal remains Low level, the digital data is output in the mode #0 output format from the sixth clock. After the SY input signal changes from Low level to High level, the digital data is output in the mode m output format from the sixth clock. At this time, the data output at the sixth clock is the data A/D converted from the analog input signal that was sampled at the falling edge of the clock input signal immediately after the SY input signal changes from Low level to High level.

The output format control input signals CTL2, CTL1 and CTL0 are fetched only in sync with the rising edge of the clock input signal after the SY input signal has risen.



Timing Chart II

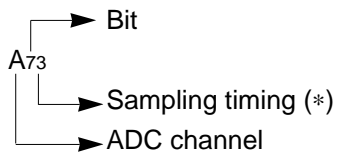
Mode #0 4 : 4 : 4



ADC channel	Output	Data							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	B71	B72	B73	B74	B75	B76	B77
	B6	B60	B61	B62	B63	B64	B65	B66	B67
	B5	B50	B51	B52	B53	B54	B55	B56	B57
	B4	B40	B41	B42	B43	B44	B45	B46	B47
	B3	B30	B31	B32	B33	B34	B35	B36	B37
	B2	B20	B21	B22	B23	B24	B25	B26	B27
	B1	B10	B11	B12	B13	B14	B15	B16	B17
	B0	B00	B01	B02	B03	B04	B05	B06	B07
C	C7	C70	C71	C72	C73	C74	C75	C76	C77
	C6	C60	C61	C62	C63	C64	C65	C66	C67
	C5	C50	C51	C52	C53	C54	C55	C56	C57
	C4	C40	C41	C42	C43	C44	C45	C46	C47
	C3	C30	C31	C32	C33	C34	C35	C36	C37
	C2	C20	C21	C22	C23	C24	C25	C26	C27
	C1	C10	C11	C12	C13	C14	C15	C16	C17
	C0	C00	C01	C02	C03	C04	C05	C06	C07
TGR		Low →							

Note (*) : See Timing Chart II.

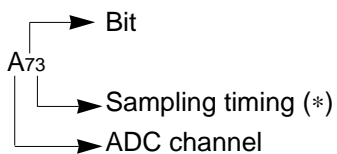
Mode #1 4 : 2 : 2 (8 fs)



ADC channel	Output	Data							
A	A7	A70	A70	A72	A72	A74	A74	A76	A76
	A6	A60	A60	A62	A62	A64	A64	A66	A66
	A5	A50	A50	A52	A52	A54	A54	A56	A56
	A4	A40	A40	A42	A42	A44	A44	A46	A46
	A3	A30	A30	A32	A32	A34	A34	A36	A36
	A2	A20	A20	A22	A22	A24	A24	A26	A26
	A1	A10	A10	A12	A12	A14	A14	A16	A16
	A0	A00	A00	A02	A02	A04	A04	A06	A06
B	B7	B70	B70	C70	C70	B74	B74	C74	C74
	B6	B60	B60	C60	C60	B64	B64	C64	C64
	B5	B50	B50	C50	C50	B54	B54	C54	C54
	B4	B40	B40	C40	C40	B44	B44	C44	C44
	B3	B30	B30	C30	C30	B34	B34	C34	C34
	B2	B20	B20	C20	C20	B24	B24	C24	C24
	B1	B10	B10	C10	C10	B14	B14	C14	C14
	B0	B00	B00	C00	C00	B04	B04	C04	C04
C	C7	B70	A70	C70	A72	B74	A74	C74	A76
	C6	B60	A60	C60	A62	B64	A64	C64	A66
	C5	B50	A50	C50	A52	B54	A54	C54	A56
	C4	B40	A40	C40	A42	B44	A44	C44	A46
	C3	B30	A30	C30	A32	B34	A34	C34	A36
	C2	B20	A20	C20	A22	B24	A24	C24	A26
	C1	B10	A10	C10	A12	B14	A14	C14	A16
	C0	B00	A00	C00	A02	B04	A04	C04	A06
TGR		High	Low	→		High	Low	→	

Note (*): See Timing Chart II.

Mode #2 4 : 2 : 2 (D2)

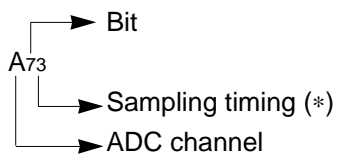


ADC channel	Output	Data							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	C70	B72	C72	B74	C74	B76	C76
	B6	B60	C60	B62	C62	B64	C64	B66	C66
	B5	B50	C50	B52	C52	B54	C54	B56	C56
	B4	B40	C40	B42	C42	B44	C44	B46	C46
	B3	B30	C30	B32	C32	B34	C34	B36	C36
	B2	B20	C20	B22	C22	B24	C24	B26	C26
	B1	B10	C10	B12	C12	B14	C14	B16	C16
	B0	B00	C00	B02	C02	B04	C04	B06	C06
C	C7	HiZ	→	→	→	→	→	→	→
	C6	HiZ	→	→	→	→	→	→	→
	C5	HiZ	→	→	→	→	→	→	→
	C4	HiZ	→	→	→	→	→	→	→
	C3	HiZ	→	→	→	→	→	→	→
	C2	HiZ	→	→	→	→	→	→	→
	C1	HiZ	→	→	→	→	→	→	→
	C0	HiZ	→	→	→	→	→	→	→
TGR		High	Low	High	Low	High	Low	High	Low

HiZ : High impedance

Note (*) : See Timing Chart II.

Mode #3 4 : 2 : 2 (Special)

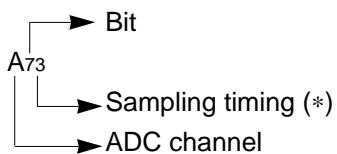


ADC channel	Output	Data							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B70	C71	B72	C73	B74	C75	B76	C77
	B6	B60	C61	B62	C63	B64	C65	B66	C67
	B5	B50	C51	B52	C53	B54	C55	B56	C57
	B4	B40	C41	B42	C43	B44	C45	B46	C47
	B3	B30	C31	B32	C33	B34	C35	B36	C37
	B2	B20	C21	B22	C23	B24	C25	B26	C27
	B1	B10	C11	B12	C13	B14	C15	B16	C17
	B0	B00	C01	B02	C03	B04	C05	B06	C07
C	C7	HiZ	→	→	→	→	→	→	→
	C6	HiZ	→	→	→	→	→	→	→
	C5	HiZ	→	→	→	→	→	→	→
	C4	HiZ	→	→	→	→	→	→	→
	C3	HiZ	→	→	→	→	→	→	→
	C2	HiZ	→	→	→	→	→	→	→
	C1	HiZ	→	→	→	→	→	→	→
	C0	HiZ	→	→	→	→	→	→	→
TGR		High	Low	High	Low	High	Low	High	Low

HiZ : High impedance

Note (*) : See Timing Chart II.

Mode #4 4 : 1 : 1

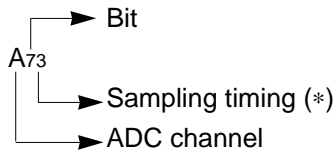


ADC channel	Output	Data								
A	A7	A70	A71	A72	A73	A74	A75	A76	A77	
	A6	A60	A61	A62	A63	A64	A65	A66	A67	
	A5	A50	A51	A52	A53	A54	A55	A56	A57	
	A4	A40	A41	A42	A43	A44	A45	A46	A47	
	A3	A30	A31	A32	A33	A34	A35	A36	A37	
	A2	A20	A21	A22	A23	A24	A25	A26	A27	
	A1	A10	A11	A12	A13	A14	A15	A16	A17	
	A0	A00	A01	A02	A03	A04	A05	A06	A07	
B	B7	B70	B50	B30	B10	B74	B54	B34	B14	
	B6	B60	B40	B20	B00	B64	B44	B24	B04	
	B5	C70	C50	C30	C10	C74	C54	C34	C14	
	B4	C60	C40	C20	C00	C64	C44	C24	C04	
	B3	HiZ	→							
	B2	HiZ	→							
	B1	HiZ	→							
	B0	HiZ	→							
C	C7	HiZ	→							
	C6	HiZ	→							
	C5	HiZ	→							
	C4	HiZ	→							
	C3	HiZ	→							
	C2	HiZ	→							
	C1	HiZ	→							
	C0	HiZ	→							
TGR		High	Low	→		High	Low	→		

HiZ : High impedance

Note (*) : See Timing Chart II.

Mode #5 4 : 1 : 1 (Special)



ADC channel	Output	Data							
A	A7	A70	A71	A72	A73	A74	A75	A76	A77
	A6	A60	A61	A62	A63	A64	A65	A66	A67
	A5	A50	A51	A52	A53	A54	A55	A56	A57
	A4	A40	A41	A42	A43	A44	A45	A46	A47
	A3	A30	A31	A32	A33	A34	A35	A36	A37
	A2	A20	A21	A22	A23	A24	A25	A26	A27
	A1	A10	A11	A12	A13	A14	A15	A16	A17
	A0	A00	A01	A02	A03	A04	A05	A06	A07
B	B7	B30	B70	C32	C72	B34	B74	C36	C76
	B6	B20	B60	C22	C62	B24	B64	C26	C66
	B5	B10	B50	C12	C52	B14	B54	C16	C56
	B4	B00	B40	C02	C42	B04	B44	C06	C46
	B3	HiZ	—————>						
	B2	HiZ	—————>						
	B1	HiZ	—————>						
	B0	HiZ	—————>						
C	C7	HiZ —————>							
	C6	HiZ —————>							
	C5	HiZ —————>							
	C4	HiZ —————>							
	C3	HiZ —————>							
	C2	HiZ —————>							
	C1	HiZ —————>							
	C0	HiZ —————>							
TGR		High	Low	—————>		High	Low	—————>	

HiZ : High impedance

Note (*) : See Timing Chart II.

Mode #6, 7 simple boundary scan 1 and 2

The CXD2303AQ has a simple boundary scan function.

Table 2. Simple boundary scan

Bits			Output data	
			MODE #6	MODE #7
A7	B7	C7	H	L
A6	B6	C6	L	H
A5	B5	C5	H	L
A4	B4	C4	L	H
A3	B3	C3	H	L
A2	B2	C2	L	H
A1	B1	C1	H	L
A0	B0	C0	L	H

Note : CLK and SY must be set.

2. Clamp Function

The following two points should be noted when using the digital clamp circuit.

- The clamp pulse must be supplied externally.
- The clamp circuit is not designed for V cycle clamping.

16 different reference levels can be selected for the digital clamp circuit through a combination of the REF0, REF1, REF2 and REF3 inputs as shown in the table below. Note that the REF0, REF1, REF2 and REF3 input signals are fetched asynchronously with the clock input signal.

Table 3. Setting values and reference levels

Setting				Reference level				
REF3	REF2	REF1	REF0	Mode	Channel A		Channels B and C	
					Decimal	Binary	Decimal	Binary
L	L	L	L	0	16	00010000	128	10000000
L	L	L	H	1	32	00100000	128	10000000
L	L	H	L	2	48	00110000	128	10000000
L	L	H	H	3	64	01000000	128	10000000
L	H	L	L	4	1	00000001	1	00000001
L	H	L	H	5	16	00010000	16	00010000
L	H	H	L	6	32	00100000	32	00100000
L	H	H	H	7	48	00110000	48	00110000
H	L	L	L	8	239	11101111	127	01111111
H	L	L	H	9	223	11011111	127	01111111
H	L	H	L	A	207	11001111	127	01111111
H	L	H	H	B	191	10111111	127	01111111
H	H	L	L	C	254	11111110	254	11111110
H	H	L	H	D	239	11101111	239	11101111
H	H	H	L	E	223	11011111	223	11011111
H	H	H	H	F	207	11001111	207	11001111

The digital clamp circuit operates in the way the average value of the A/D-converted analog input signal data sampled during the 32 clock cycles after the clamp pulse is input and the reference data set by REF0 to REF3 are compared, and the result difference becomes smaller (See Timing Chart III). Therefore, take notice that when there is the fixed noise and others during the 32 cycles of the clock signal, the digital clamp circuit deals with the noise portion as the signal and it comes to the stable state still including the error. Photos 1 and 2 show the clamp circuit responses for the Application Circuit 1.

Photo 2 shows that inputting the clamp pulse during the vertical hold has no effect on the input signal.

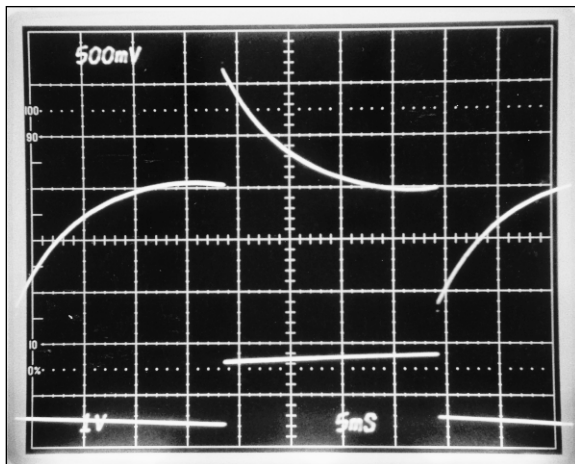
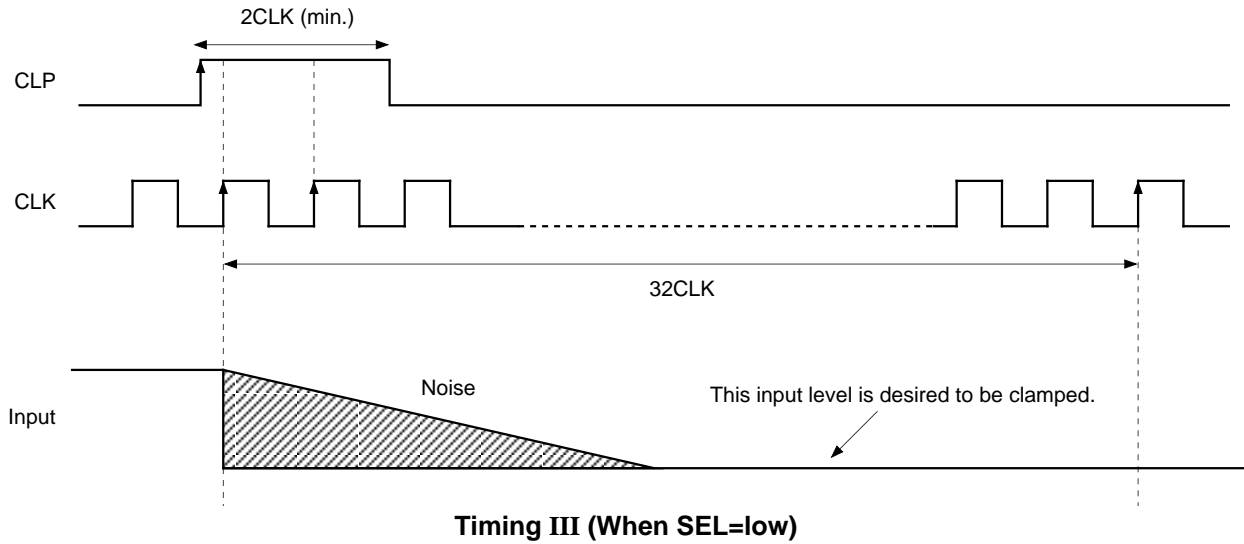


Photo 1. Response waveform of clamp circuit
(When $F_{CLK}=50$ MSPS, clamp pulse is NTSC SYNC and reference data is 128)

Upper: Analog input pin waveform
(H: 5 ms/div., V: 500 mV/div.)
Lower: Analog input signal waveform
(H: 5 ms/div., V: 2 V/div.)

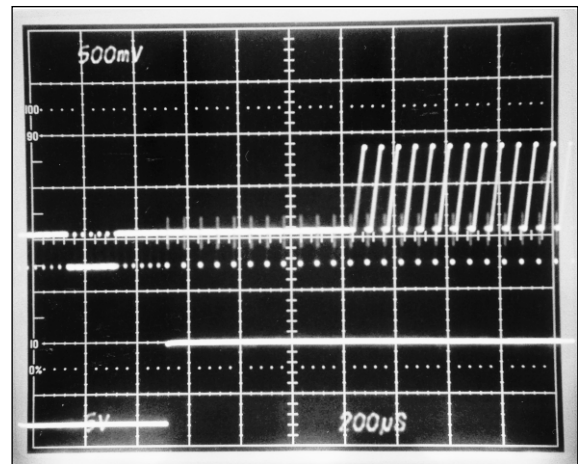


Photo 2. Response waveform of clamp circuit
($F_{CLK}=50$ MSPS, clamp pulse is NTSC SYNC and reference data is 128)

Upper: Analog input pin waveform
(H: 200 μ s/div., V: 5 V/div.)
Lower: Vertical hold pulse
(H: 200 μ s/div., V: 500 mV/div.)

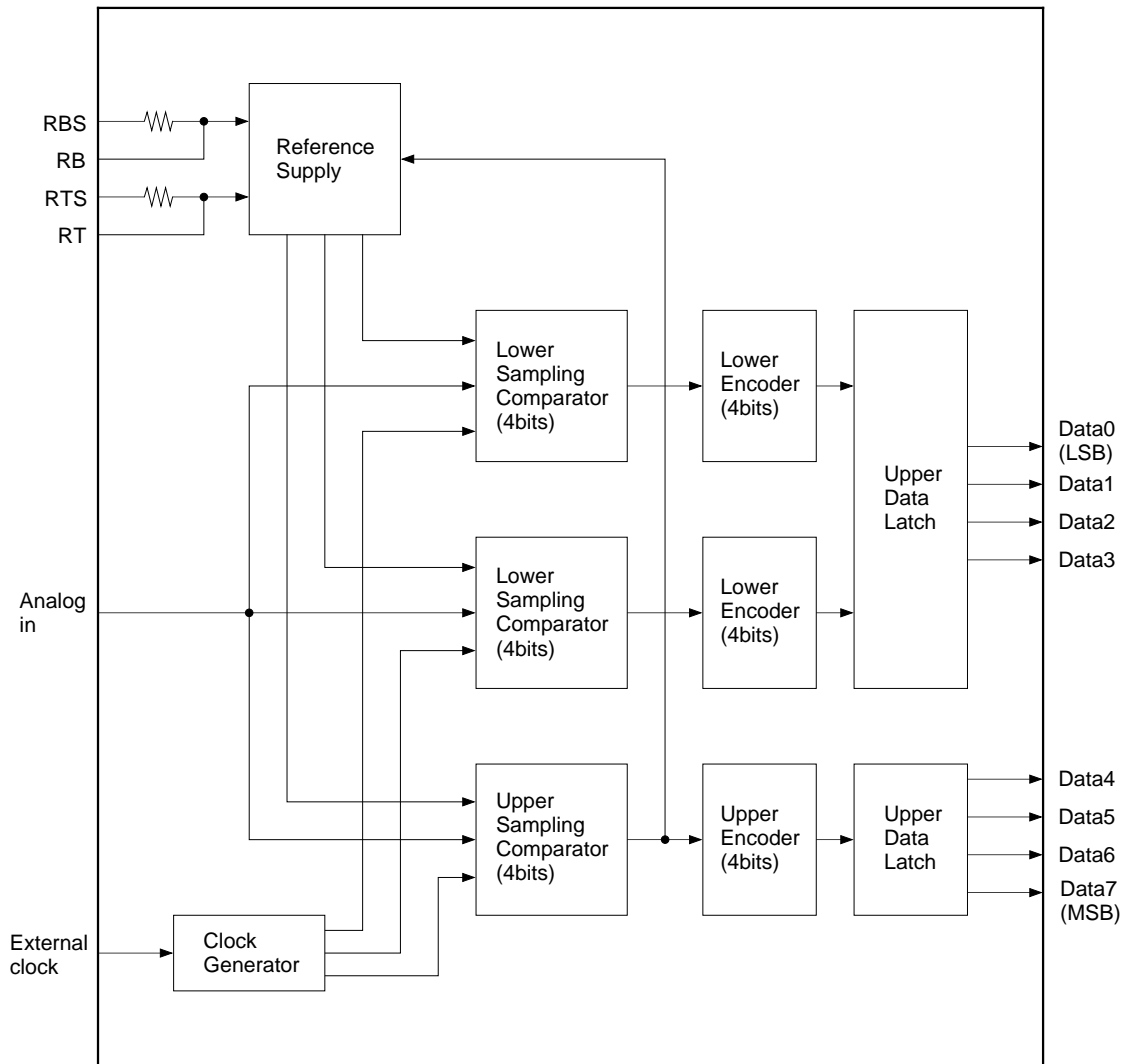
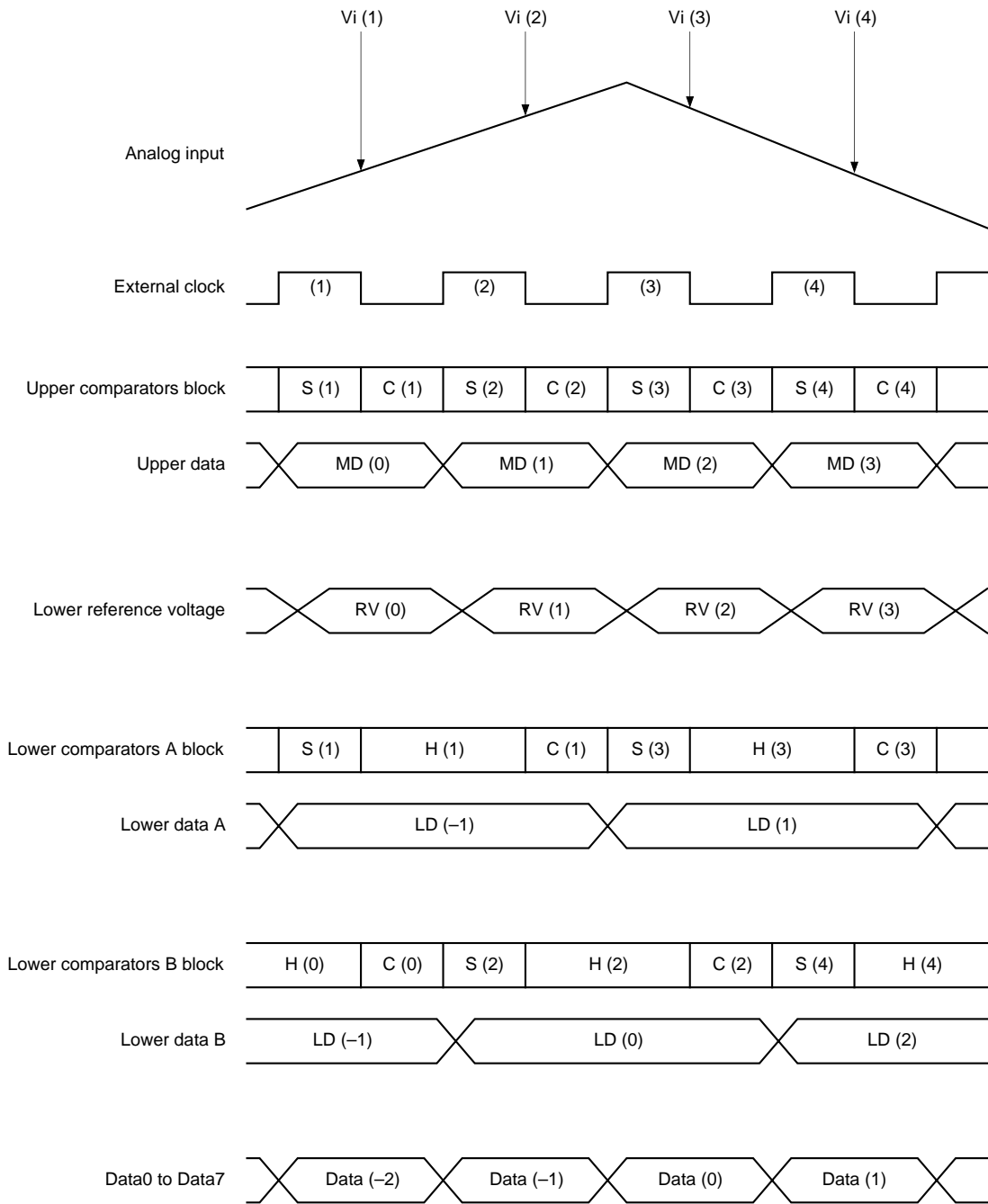


Fig. 1. 8-bit ADC block diagram



Timing Chart IV

3. 8-bit ADC Operation (See Fig.1 and Timing Chart IV)

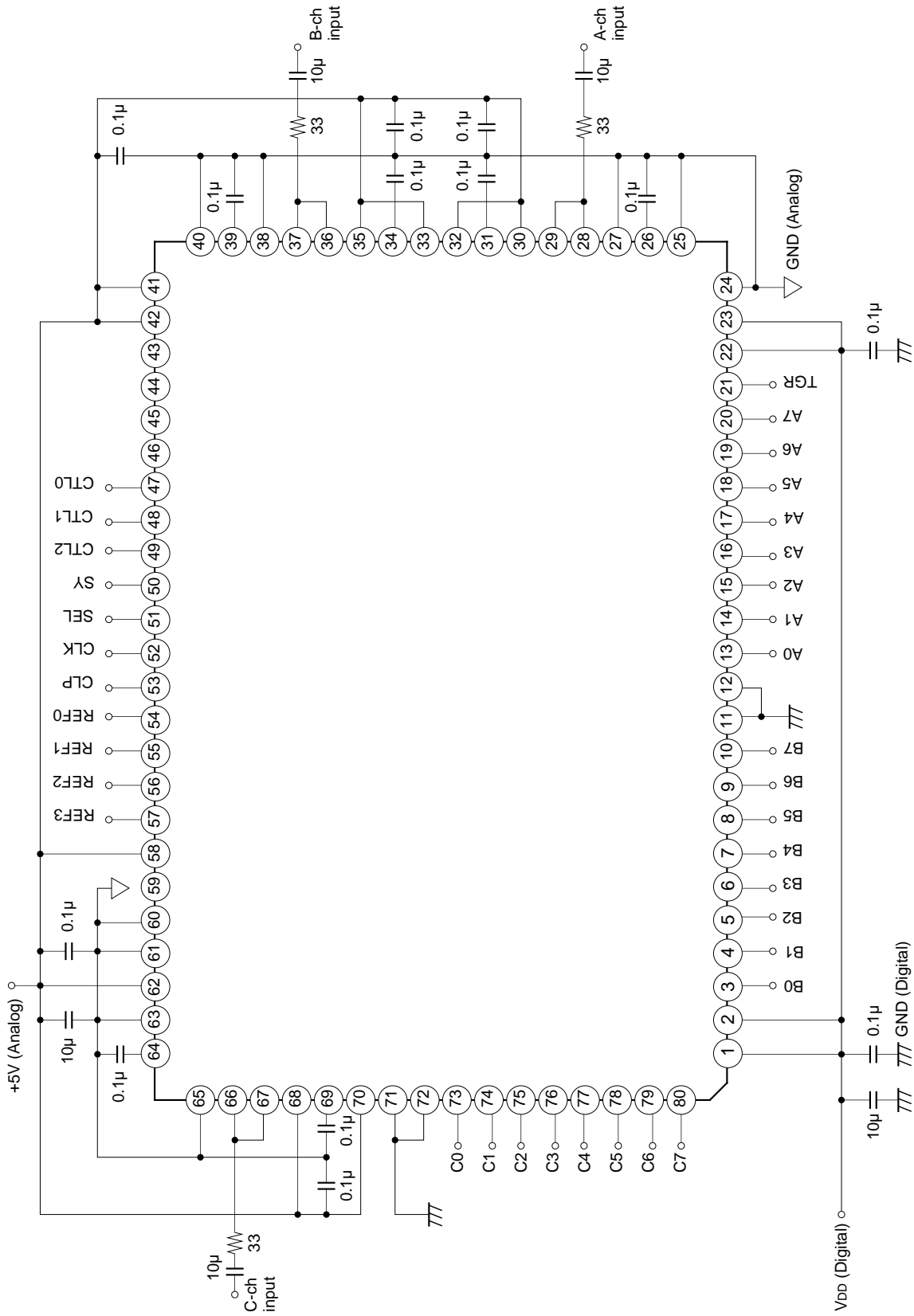
1) The CXD2303AQ includes 3 channels of the 8-bit A/D converter. This converter has the 2-step parallel system, composed of a 4-bit upper comparator and two 4-bit lower comparator blocks. The reference voltage that is equal to the voltage between RT-RB/16 is constantly applied to the upper 4-bit comparator block. Voltage corresponded to the upper data is fed to the lower 4-bit comparator block through the reference supply. RTS and RBS pins serve for the self-generation of RT (Reference voltage top) and RB (Reference voltage bottom), and they are also used as the sense pins as shown in the Application Circuit 3.

- 2) This IC uses an offset cancel type comparator that operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the Timing Chart IV with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.
- 3) The operation of respective parts is as indicated in the Timing Chart IV. For instance the input voltage V_i (1) is sampled at the falling edge of the external clock (1) by means of the upper comparator block and the lower comparator A block.
The upper comparator block establishes comparison data MD (1) at the rising edge of the external clock (2). Simultaneously the reference supply generates the lower reference voltage RV (1) corresponded to the upper results. The lower comparator A block establishes comparison data LD (1) at the rising edge of the external clock (3). MD (1) and LD (1) are combined and output as Out (1) at the rising edge of the external clock (4). Accordingly, there is a 2.5 clock delay from the analog input sampling point to the A/D converter digital data output.
Note that there is a 4.5 clock delay from the analog input sampling point to the digital data output because the output data selector circuit is located at the stage after the A/D converter circuit. (See the item 5 of Notes on Operation)

Notes on Operation

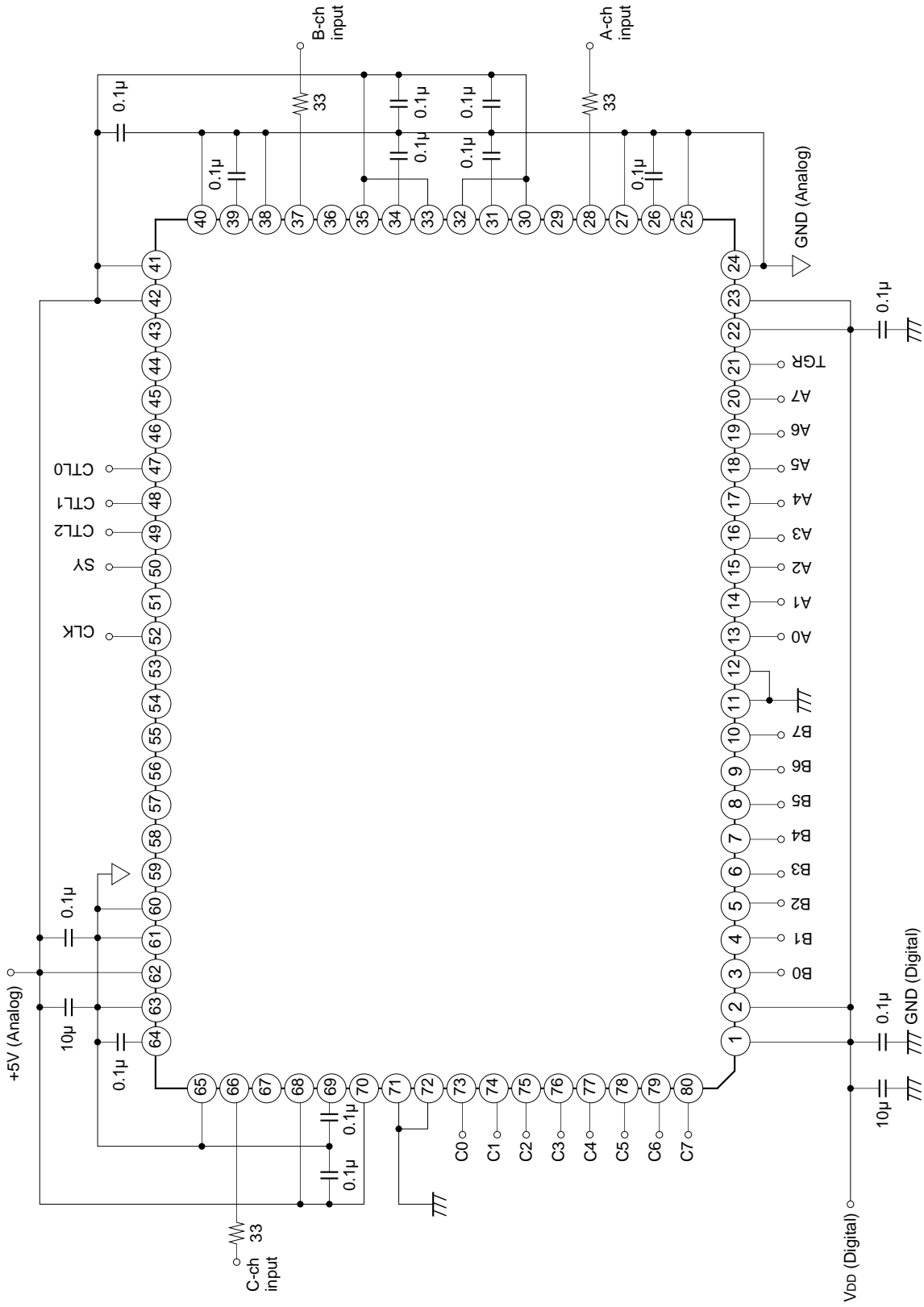
1. Power supply and ground
To reduce the effects of noise, separate the analog and digital systems around the device. Bypass both the digital and analog power supply pins to the respective grounds using ceramic capacitors of about 0.1 μF set as close to the pin as possible.
2. Analog input
Compared with flash type A/D converters, the input capacitance of the analog input is rather small. However, driving must be performed with an amplifier featuring sufficient bands and drive capability. When driving with an amplifier of low output impedance, parasitic oscillation may occur. This can be prevented by inserting resistance of about 33 Ω in series between the amplifier output and A/D input. When the input signals of Pins 28, 37 and 66 are monitored, the kickback noise of the clock can be found. However, this has no effect on the A/D conversion characteristics.
3. Clock input
The clock line wiring should be as short as possible and should be separated from other circuits to avoid any interference with other signals.
4. Reference input
Voltages ART to ARB, BRT to BRB and CRT to CRB supports dynamic range of the analog input. Stable characteristics can be obtained by bypassing these pins to GND using capacitors of about 0.1 μF . The self-bias function that generates V_{RT} =about 2.5 V and V_{RB} =about 0.6 V is activated by shorting ARTS, BRTS and CRTS to AV_{DD} and ARBS, BRBS and CRBS to AV_{SS} , respectively.
5. Timing
Analog input is sampled at the falling edge of CLK and output as digital data synchronized with a delay of 4.5 clocks at its rising edge (see Timing Chart I-3). The delay from the clock rising edge to the data output is about 9 ns (DV_{DD} =5 V).
6. Output enable pins
Pins 13 to 20 (A0 to A7) are in the output mode by leaving XAOE open or connecting it to DV_{SS} , and these pins are in the high impedance mode by connecting XAOE to DV_{DD} . Pins 3 to 10 (B0 to B7) have the same relationship with XBOE, and Pins 73 to 80 (C0 to C7) with XCOE, respectively.

Application Circuit
1. When clamp and self-bias are used



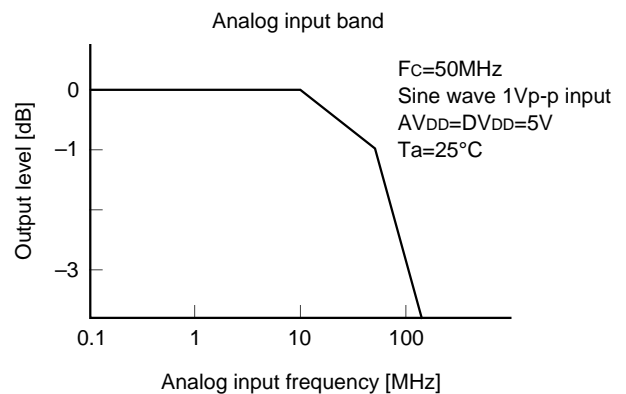
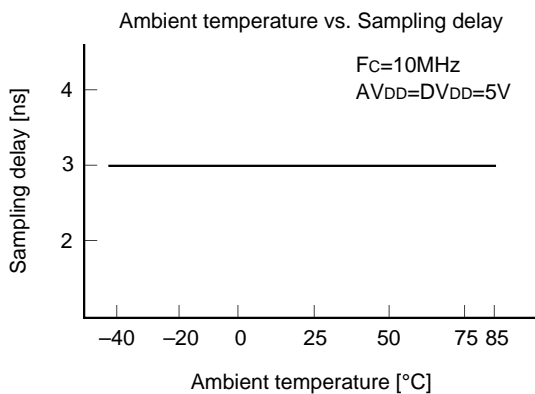
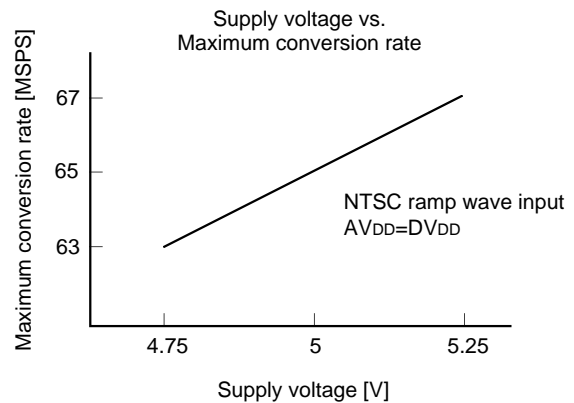
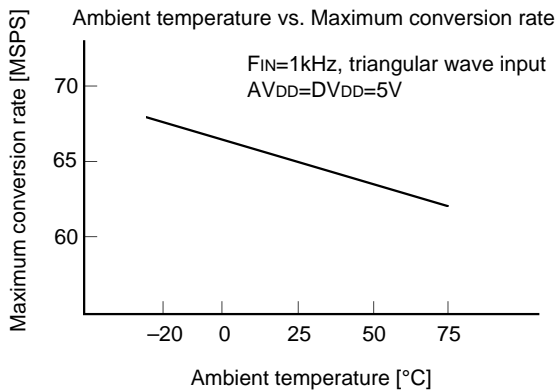
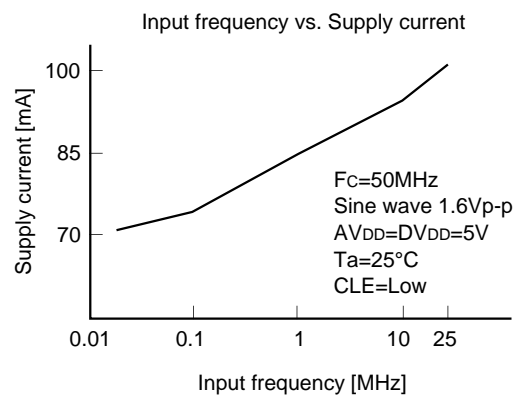
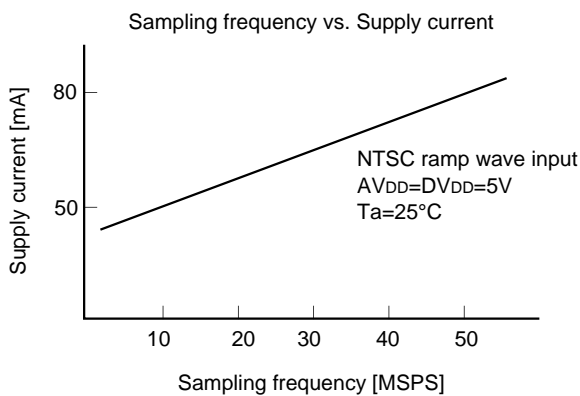
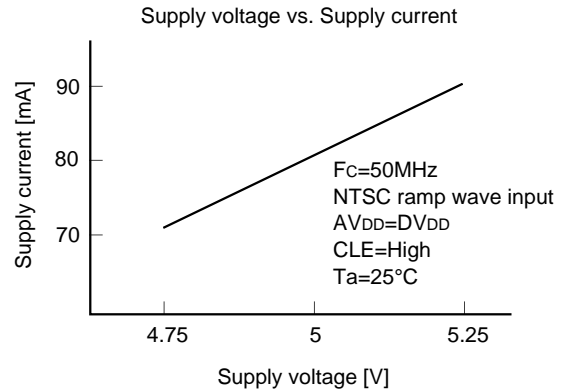
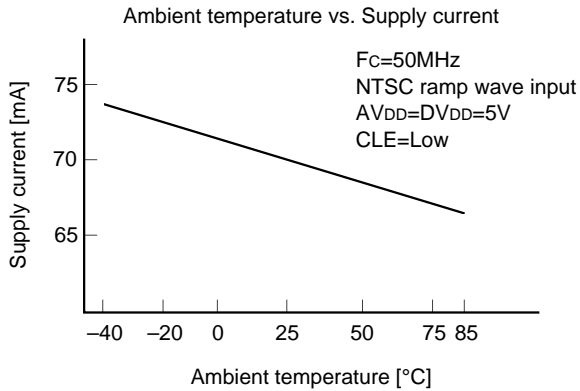
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

2. When self-bias is used, and clamp is not used

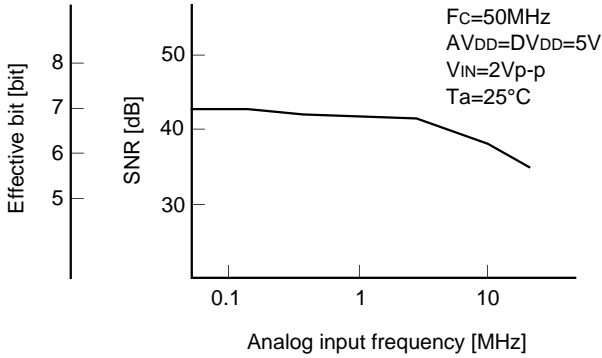


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

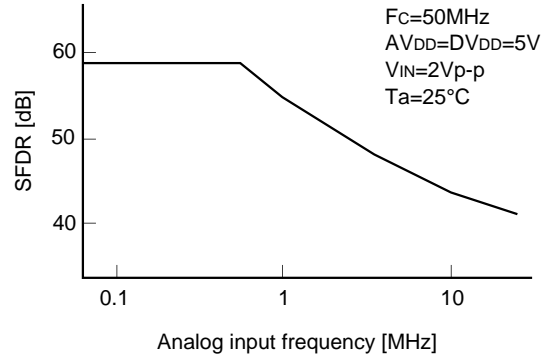
Example of Representative Characteristics



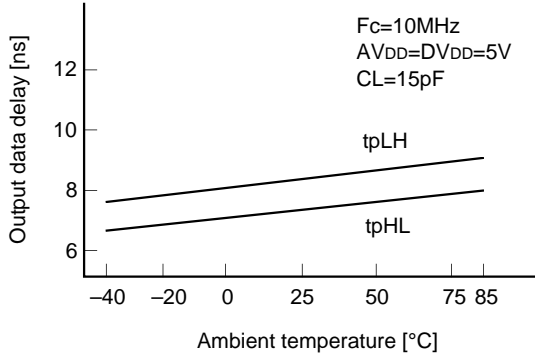
Analog input frequency vs. SNR, effective bit



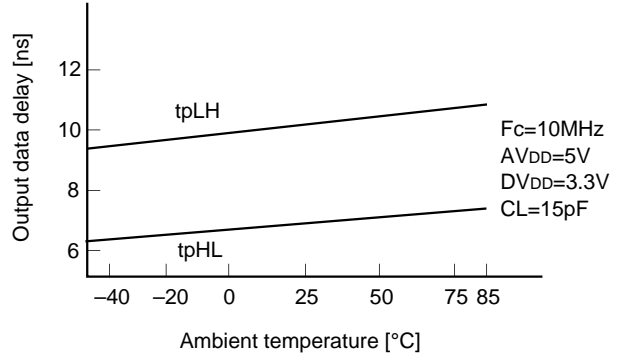
Analog input frequency vs. SFDR



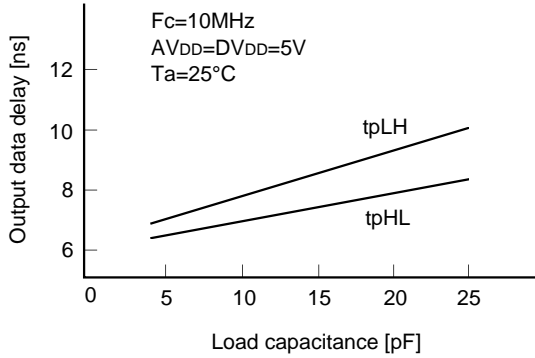
Ambient temperature vs. Output data delay



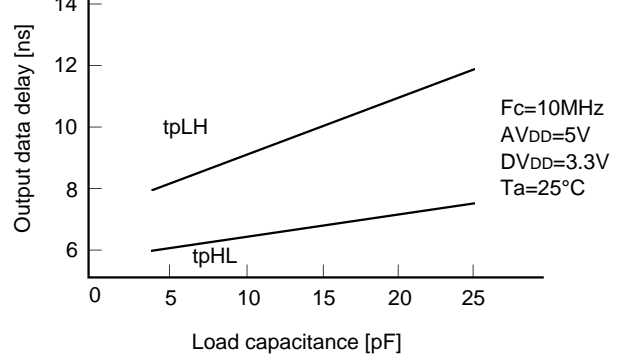
Ambient temperature vs. Output data delay



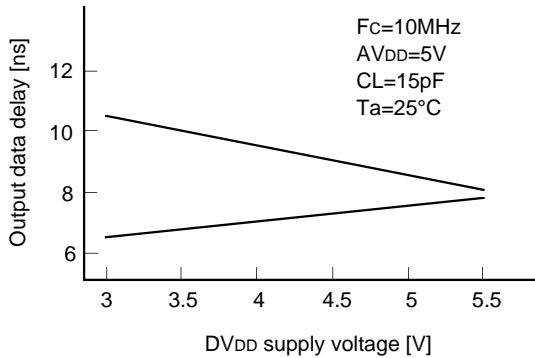
Load capacitance vs. Output data delay



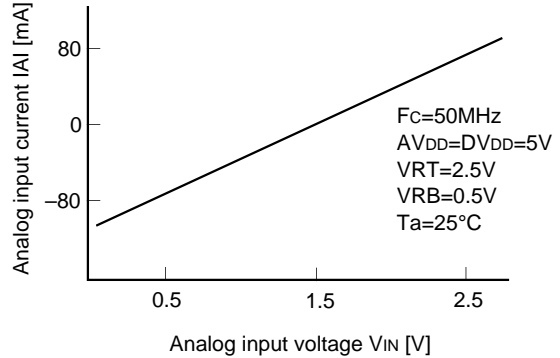
Load capacitance vs. Output data delay

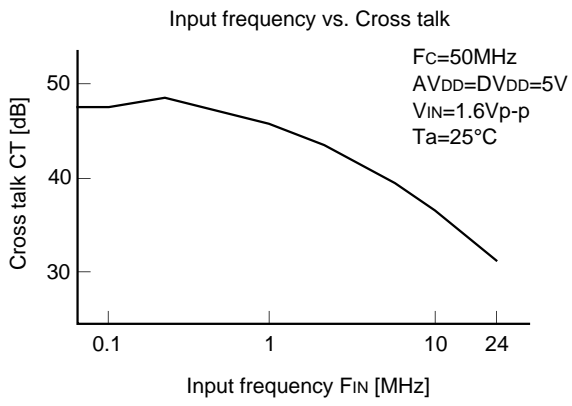


DVDD supply voltage vs. Output data delay



Analog input voltage vs. Input current

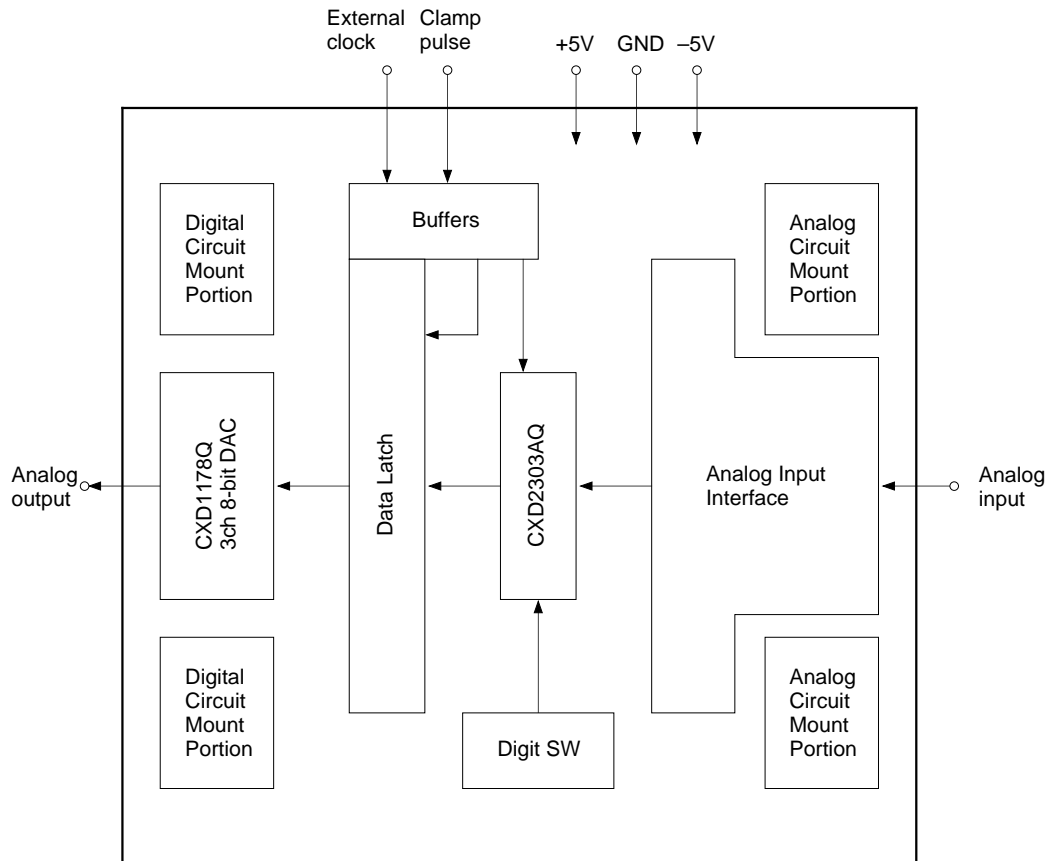




CXD2303Q Evaluation Board

Evaluation boards are available for the CMOS converter CXD2303AQ.

Block Diagram



Characteristics

- Resolution 8 bits
- Maximum conversion rate 50 MHz
- Supply voltage ± 5.0 V (Single +5 V power supply possible at self-bias use)

Supply voltage

Item	Min.	Typ.	Max.	Unit
+5 V			185	mA
-5 V			20	

Clock input

Either 1 or 2 should be used.

1. TTL
 - Pulse width T_{CW1} 9 ns (min.)
 - T_{CW0} 9 ns (min.)
2. Sine wave

Analog Output (CXD1178Q) (RL = 200 Ω)

Item	Min.	Typ.	Max.	Unit
Analog output	1.8	2.0	2.2	V
Full-scale output ratio (*)	0	1.5	3	%

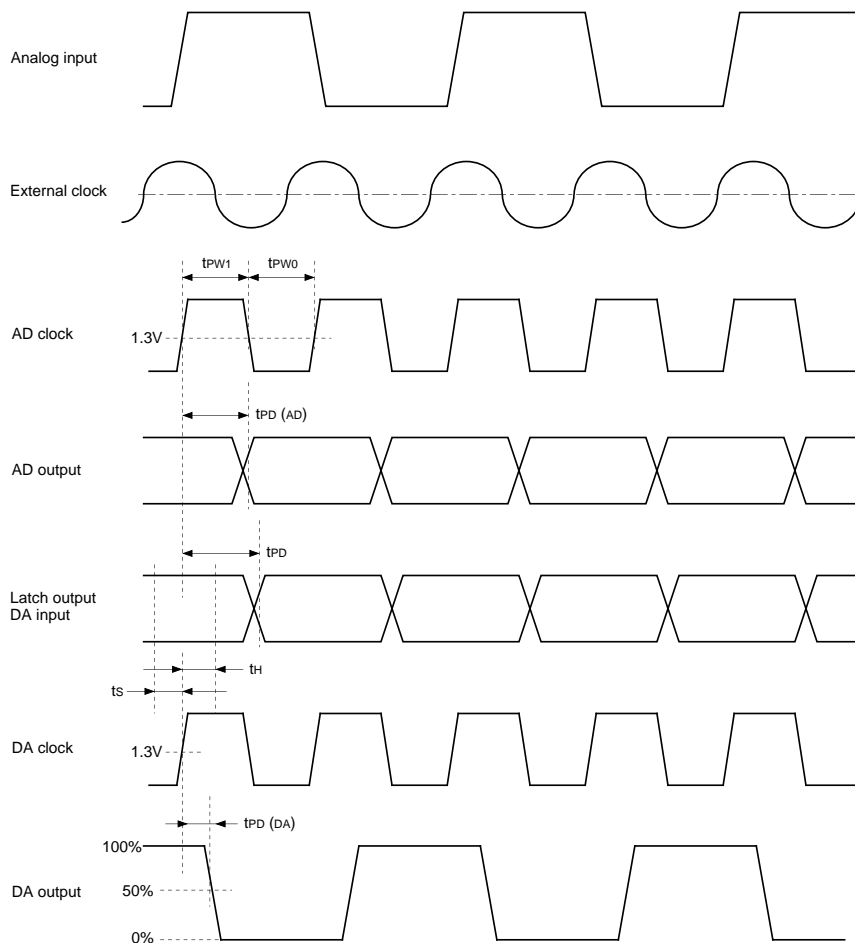
$$* \text{ Full-scale output ratio} = \left| \frac{\text{Full-scale voltage of each channel}}{\text{Average of the full-scale voltage of each channel}} - 1 \right| \times 100 [\%]$$

Output Format (CXD2303AQ)

The table shows the output format of AD converter.

Analog input voltage	Step	Digital output code	
		MSB	LSB
VART, VBRT, VCRT	0	1 1 1 1 1 1 1 1	
:	:	:	:
:	127	1 0 0 0 0 0 0 0	
:	128	0 1 1 1 1 1 1 1	
:	:	:	:
VARB, VBRB, VCRB	255	0 0 0 0 0 0 0 0	

Timing Chart



Item	Symbol	Min.	Typ.	Max.	Unit
External clock (*)		1			V
Clock High time	T _{PW1}	9		1100	ns
Clock Low time	T _{PW0}	9		1100	ns
Data delay (AD)	t _{PD (AD)}	4.5		11.0	ns
Data delay (latch)	t _{DD}			9.5	ns
Setup time	t _s	5			ns
Hold time	t _h	10	10		ns
Propagation delay time (DA)	t _{PD (DA)}		10		ns

* In the case of a sine wave, the effects of jitter increase as the input voltage decreases.

List of Parts

Resistor

R20	75 Ω
R21	75 Ω
R30A, B, C	510 Ω
R31A, B, C	510 Ω
R32A, B, C	510 Ω
R33A, B, C	100 kΩ
R34A, B, C	75 Ω
R35A, B, C	33 kΩ
R50	3.3 kΩ
R51	200 Ω
R52	200 Ω
R53	200 Ω
VR20	2 kΩ
VR21	2 kΩ
VR30A, B, V	2 kΩ
VR31A, B, V	2 kΩ
VR50	1 kΩ

Transistor

Q30A, B, C	2SC2785
Q31A, B, C	2SC2785
Q32A, B, C	2SC2785

IC

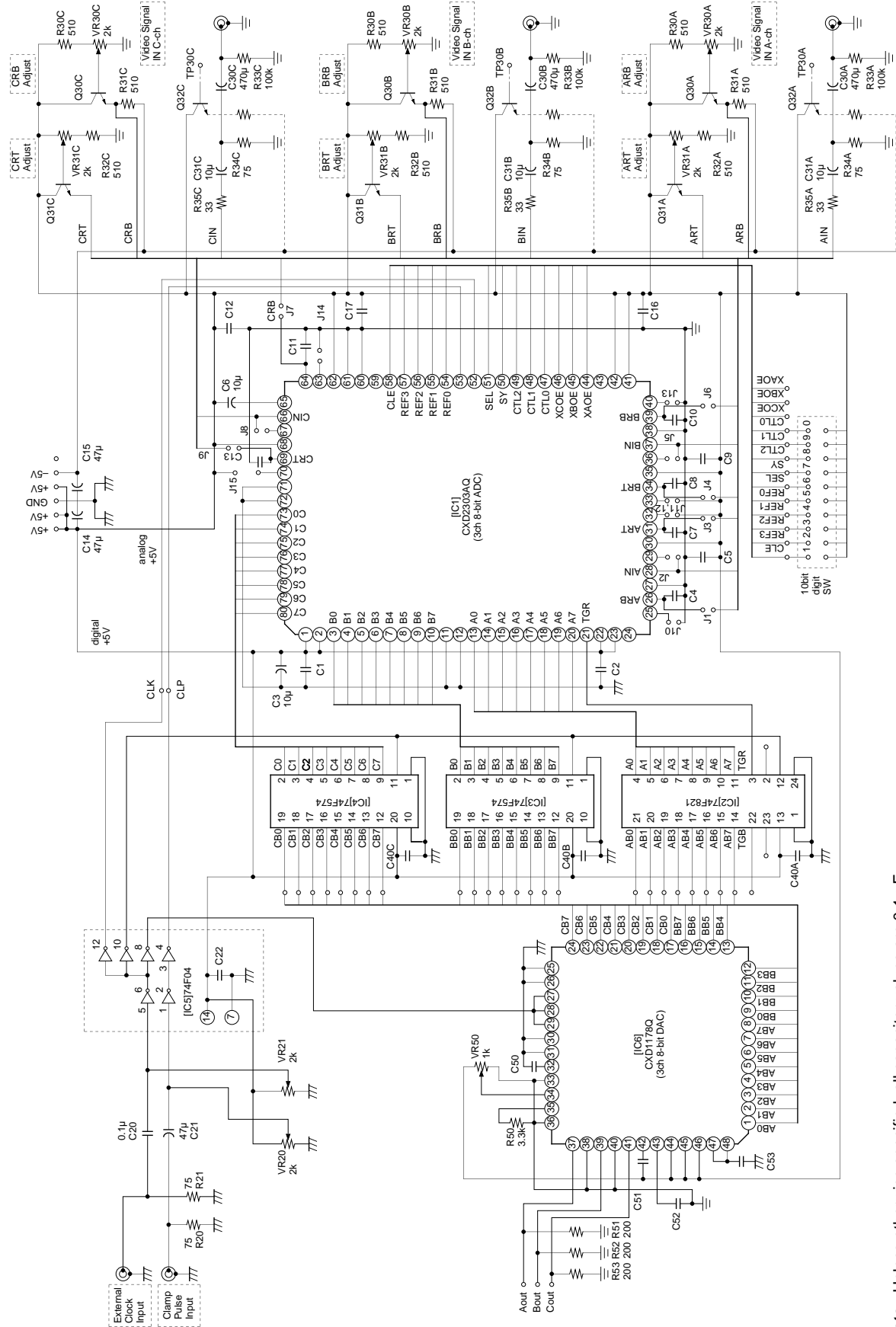
IC1	CXD2303AQ
IC2	74F821
IC3	74F574
IC4	74F574
IC5	74F04
IC6	CXD1178Q

Capacitor

C1	0.1 μF
C2	0.1 μF
C3	10 μF
C4	0.1 μF
C5	0.1 μF
C6	10 μF
C7	0.1 μF
C8	0.1 μF
C9	0.1 μF
C10	0.1 μF
C11	0.1 μF
C12	0.1 μF
C13	0.1 μF
C14	47 μF
C15	47 μF
C16	0.1 μF
C17	0.1 μF
C20	0.1 μF
C21	47 μF
C22	0.1 μF
C30A, B, C	470 μF
C31A, B, C	10 μF
C30A, B, C	0.1 μF
C50	0.1 μF
C51	0.1 μF
C52	0.1 μF
C53	0.1 μF

Others

Connector	BNC-LR-PC-3 (Hirose Electric Co.,Ltd.)
DIP SW	



Note : Unless otherwise specified, all capacitor values are 0.1 μ F.

Adjustment

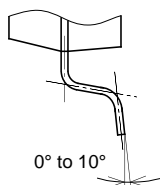
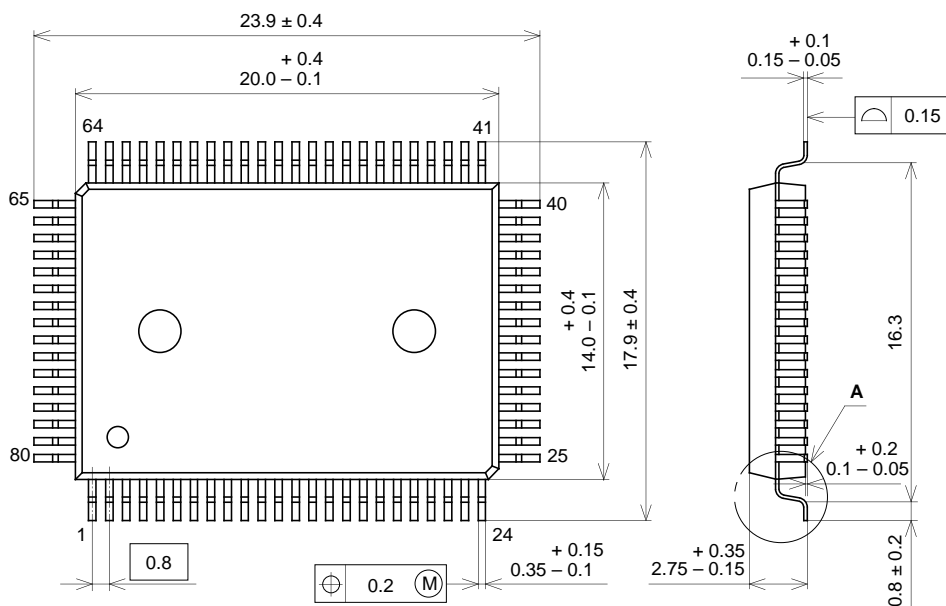
1. Vref adjustment (VR30, VR31)
Adjustment of A/D converter reference voltage. ARB, BRB and CRB are adjusted through VR30A, VR30B and VR30C, respectively, and ART, ARB and CRT through VR31A, VR31B and VR31C. When self-bias is used, there is no need for adjustment. Reference voltage is set through self-bias delivery.
2. DAC output full-scale adjustment (VR50)
Full-scale voltage of D/A converter output is adjusted to about 2 V at the PCB shipment.
3. Clamp pulse and clock signal DC voltage adjustment (VR20, VR21)
The clamp pulse and the clock signal DC voltages are adjusted.
4. DIP switches
All DIP switches other than CLE are set to OFF when the PCB is shipped from the factory. Only CLE is set to ON.

Notes on Operation

1. Reference voltage
When ARTS, BRTS and CRTS are connected to AV_{DD} and at the same time ARBS, BRBS and CRBS are connected to AV_{SS}, the self-bias function causes the ART, BRT and CRT voltage to become about 2.5 V, and the ARB, BRB, and CRB voltage to become about 0.5 V. On the evaluation board, either self-bias or the external reference voltage can be selected depending on the junction method of the jumper line. When shipped from the factory, the reference voltage is set to self-bias. To select the external reference voltage, adjust the dynamic range (V_{RT}-V_{RB}) to 1.7 V_{p-p} or more.
2. Clock input
The clock signal should be supplied externally.
3. The three latch ICs (74F574, 74F821) are not absolutely necessary for the evaluation of the ADC and DAC. That is, operation is performed normally if the ADC output data is directly input to the DAC input. However, as the ADC output data is hardly ever D/A converted without executing digital signal processing, it was mounted on the main board to indicate an example layout of digital signal processing IC. Use the latch IC output when the ADC output data is used.
4. When clamp is not used
Turning CLE to Low will set the clamp function OFF. In this case, the DC element is cut off by means of C31A, C31B and C31C on the main board and DC voltage on the ADC side of C31A, C31B and C31C turns to about (V_{ART}+V_{ARB}) /2, (V_{BRT}+V_{BRB}) /2, and (V_{CRT}+V_{CRB}) /2. To transfer DC elements of input signals, short C31A, C31B and C31C. At that time, it is necessary to bias input signals, but keeping R34A, R34B and R34C open, Q32A, Q32B, Q32C can also be used as buffer. Use the open space for the bias circuit.
5. Clamp pulse latch
The latch is incorporated in the CLP pin of the CXD2303AQ.
6. Peripheral through hole
There is a group of through holes on the analog input, output and logic. They are to be used when mounting additional circuits to the evaluation board. Use when necessary.
The connector hole on the DAC part is used to mount the test chassis mount jack.

Package Outline Unit : mm

80PIN QFP (PLASTIC)



DETAIL A

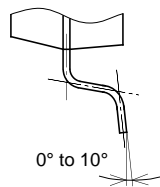
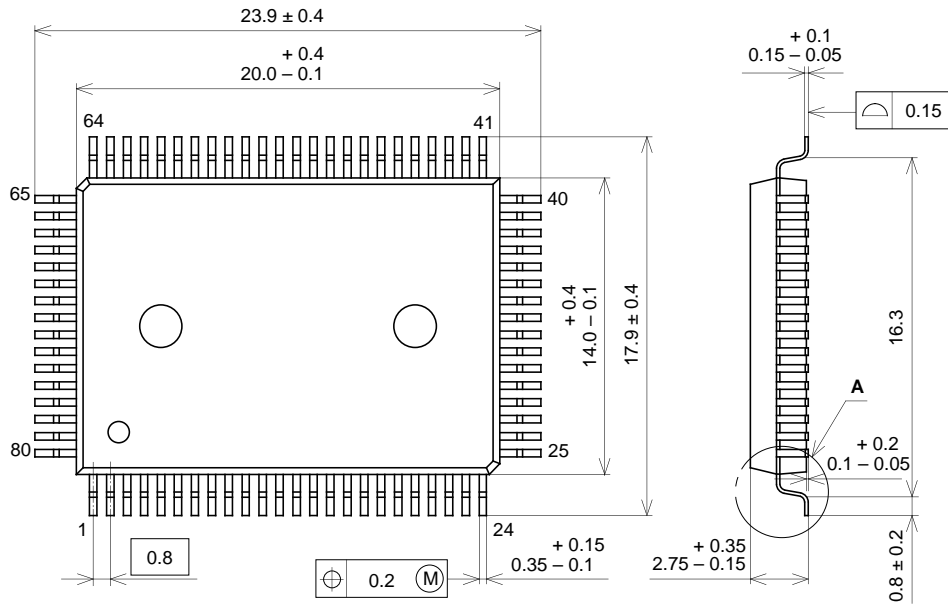
SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

Package Outline Unit : mm

80PIN QFP (PLASTIC)



DETAIL A

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	_____

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18μm