Digital Comb Filter (NTSC)

Description

The CXD2073Q is an adaptive comb filter compatible with NTSC system, and provide high-precision Y/C separation with a single chip.

Features

- Y/C separation by adaptive processing
- Horizontal aperture compensation circuit
- 8-bit A/D converter (1 channel)
- 8-bit D/A converter (2 channels)
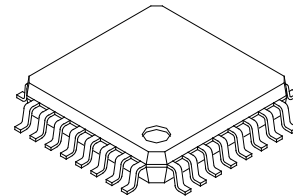- One 1H delay line
- 4 PLL
- Clamp circuit

32 pin QFP (Plastic)

Structure

Silicon gate CMOS IC

Applications

Y/C separation for color TVs and VCRs

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

- Supply voltage DV_{DD} V_{SS} – 0.5 to +7.0   V
-   DAVD V_{SS} – 0.5 to +7.0   V
-   ADVD V_{SS} – 0.5 to +7.0   V
-   PLVD V_{SS} – 0.5 to +7.0   V
- Input voltage V_I V_{SS} – 0.5 to V_{DD} +0.5 V
- Output voltage V_O V_{SS} – 0.5 to V_{DD} +0.5 V
- Operating temperature
  - T_{opr} –20 to +75   °C
- Storage temperature
  - T_{stg} –55 to +150   °C

Recommended Operating Conditions

- Supply voltage DV_{DD} 5.0 ± 0.25   V
-   DAVD   5.0 ± 0.25   V
-   ADVD   5.0 ± 0.25   V
-   PLVD   5.0 ± 0.25   V
- Operating temperature
  - T_{opr} –20 to +75   °C

E97411-PS

Pin Configuration (Top View)
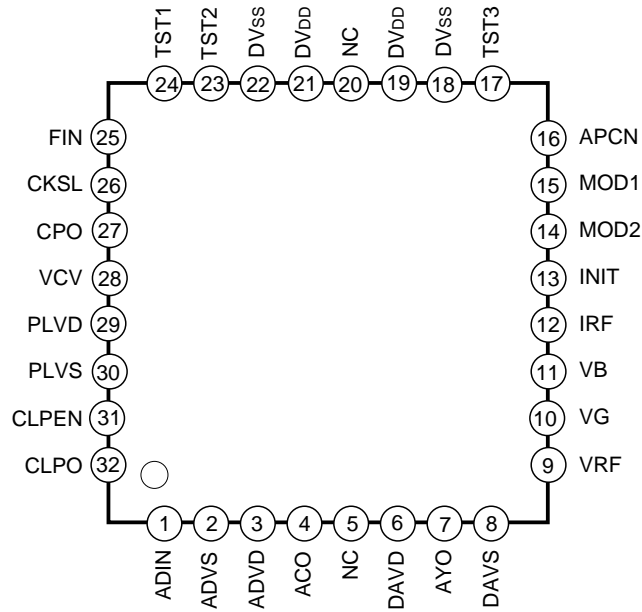
Block Diagram
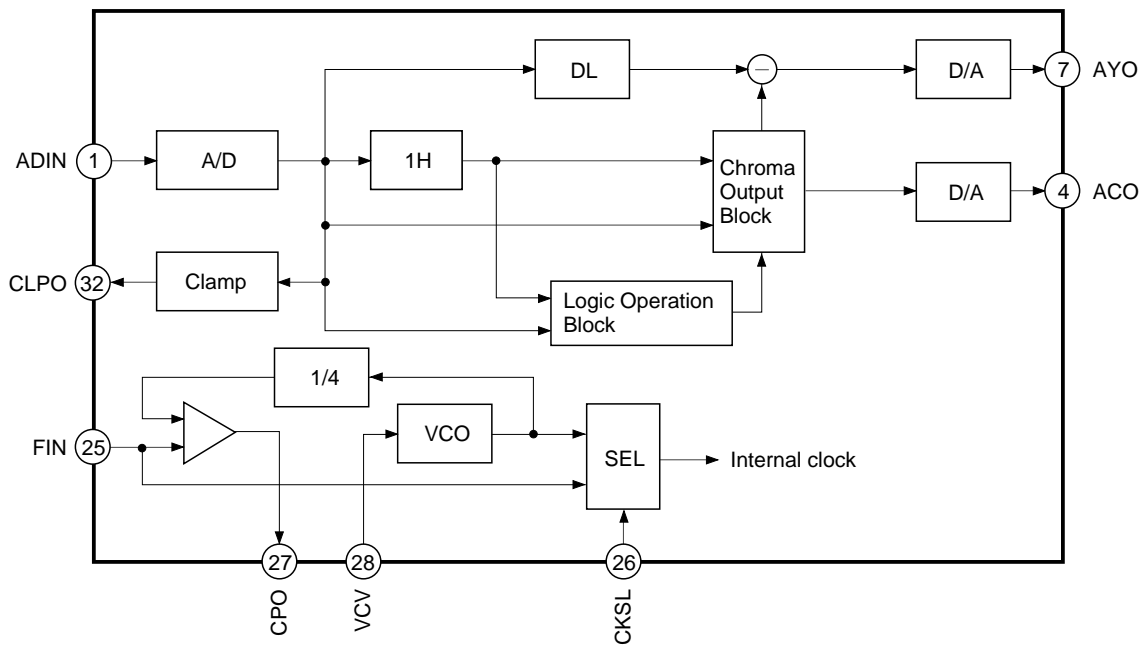
Pin Description

Pin No.	Symbol	I/O	Description
1	ADIN	I	Comb filter analog input (A/D converter input)
2	ADVS	—	Analog ground for A/D converter
3	ADVD	—	Analog power supply for A/D converter (+5V)
4	ACO	O	Analog chroma signal output
5	NC	—	Leave this pin open.
6	DAVD	—	Analog power supply for D/A converter (+5V)
7	AYO	O	Analog luminance signal output
8	DAVS	—	Analog ground for D/A converter
9	VRF	I	D/A converter VRF (reference voltage). Sets the full-scale value for D/A converter.
10	VG	O	Connect to DAVD via a capacitor of approximately 0.1µF.
11	VB	O	Connect to DAVS via a capacitor of approximately 0.1µF.
12	IRF	O	Connect a resistor of 16 times (16R) that of the output resistor "R" of AYO pin.
13	INIT	I	Test. Normally, fix to Low.
14	MOD2	I	Y/C separation status setting pins MOD2　MOD1 　L　　　L　　　　Adaptive processing mode 　L　　　H　　　　BPF separation fixed mode 　H　　　L　　　　Y through mode 　H　　　H　　　　Simple comb mode
15	MOD1	I	
16	APCN	I	Aperture compensation switching 　L: Aperture compensation OFF 　H: Aperture compensation ON
17	TST3	O	Test. Normally, leave this pin open.
18	DV$_{SS}$	—	Digital ground
19	DV$_{DD}$	—	Digital power supply (+5V)
20	NC	—	Leave this pin open.
21	DV$_{DD}$	—	Digital power supply (+5V)
22	DV$_{SS}$	—	Digital ground
23	TST2	O	Test. Normally, leave this pin open.
24	TST1	I	Test. Normally, fix to Low.
25	FIN	I	FSC clock input. Input burst-locked fsc when PLL is used. Input burst-locked 4fsc when PLL is not used.
26	CKSL	I	PLL control. 　L: Clock, which is input to FIN, is supplied internally when PLL is not used. 　H: 4fsc of VCO oscillation output is supplied to internal clock when PLL is used.
27	CPO	O	Phase comparison output for built-in PLL. Leave this pin open when PLL is not used.
28	VCV	I	Built-in VCO oscillation control voltage input. Connect to PLVS when PLL is not used.
29	PLVD	—	PLL power supply (+5 V)
30	PLVS	—	PLL ground
31	CLPEN	I	Clamp enable 　L: Clamp function is enabled. 　H: Clamp function is disenabled.
32	CLPO	O	Connect to ADIN when clamp circuit is used. Leave this pin open when clamp circuit is not used.

Electrical Characteristics $(V_{DD} = 5 \pm 0.25V, V_{SS} = 0V, T_a = -20 \text{ to } +75°C)$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	DV_{DD}	—	4.75	5.0	5.25	V
	ADVD					
	DAVD					
	PLVD					
Operating temperature	T_{opr}	—	−20	—	+75	°C
Supply current	I_{DD}	Clock 14MHz	—	—	60	mA
High level input voltage	V_{IH}	CMOS level	$V_{DD} \times 0.7$	—	V_{DD}	V
Low level input voltage	V_{IL}	CMOS level	V_{SS}	—	$V_{DD} \times 0.3$	V
High level output voltage	V_{OH}	$I_{OH} = -2mA$	$V_{DD} - 0.8$	—	V_{DD}	V
Low level output voltage	V_{OL}	$I_{OL} = 4mA$	V_{SS}	—	0.4	V
Logical Vth	LVth		—	$V_{DD}/2$	—	V
Input voltage	V_{IN}	FIN (Pin 25)	0.5	—	V_{DD}	Vp-p
Feedback resistor	R_{FB}		250k	1M	2.5M	Ω

A/D Converter Characteristics $(V_{DD} = 5V, T_a = 25°C, f = 10MHz)$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		14.3	—	—	MSPS
Analog input band width	BW	−3dB	—	18	—	MHz
Input bias	BOTTOM		0.48	0.52	0.56	V
	TOP − BOTTOM		1.96	2.08	2.22	V
Output data delay	tpd		—	—	45	ns
Differential linearity error	E_D		−1.0	—	+1.0	LSB
Integral linearity error	E_L		−3.0	—	+3.0	LSB

D/A Converter Characteristics $(V_{DD} = 5V, V_{RF} = 2V, I_{RF} = 3.3k\Omega, R = 200\Omega, T_a = 25°C, f = 10MHz)$

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax	—	14.3	—	—	MSPS
Differential linearity error	E_D	—	−0.8	—	+0.8	LSB
Integral linearity error	E_L	—	−2.0	—	+2.0	LSB
Output full-scale voltage	V_{FS}	—	1.805	1.90	1.995	V
Output full-scale current	I_{FS}	—	—	9.5	15	mA
Output offset voltage	V_{OS}	—	—	—	1.0	mV
Precision guaranteed output voltage range	V_{OC}	—	1.8	—	2.1	V

Clamp (V$_{DD}$ = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clamp level[*1]	CLV		—	0.67	—	V

[*1] Sync tip clamp

Description of Functions

• Horizontal aperture compensation

Compensates aperture degradation accompanied by D/A conversion.

This compensation is effective for the following modes; adaptive processing, Y through, and simple comb modes.

• Adaptive processing mode

This mode detects interline correlation, switches between comb filter processing and BPF processing, and operates Y/C separation.

• Y through mode

The composite video signal input from ADIN (Pin 1) is A/D converted. It is also D/A converted, and then output from AYO (Pin 7).

At this time, the output of ACO (Pin 4) is the same output as that of adaptive processing mode.

• BPF mode

C signal is generated by passing composite video signal through BPF.

Y output is a signal in which the C signal generated is subtracted from input composite video signal.

• Simple comb mode

Y/C separation is operated by the comb filter processing forcibly.

Modes	MOD1 (Pin 15)	MOD2 (Pin 14)
Adaptive processing mode	L	L
Y through mode	L	H
BPF mode	H	L
Simple comb mode	H	H

Application Circuit for D/A Converter

↑ : analog power supply 5V   ⏚ : analog ground
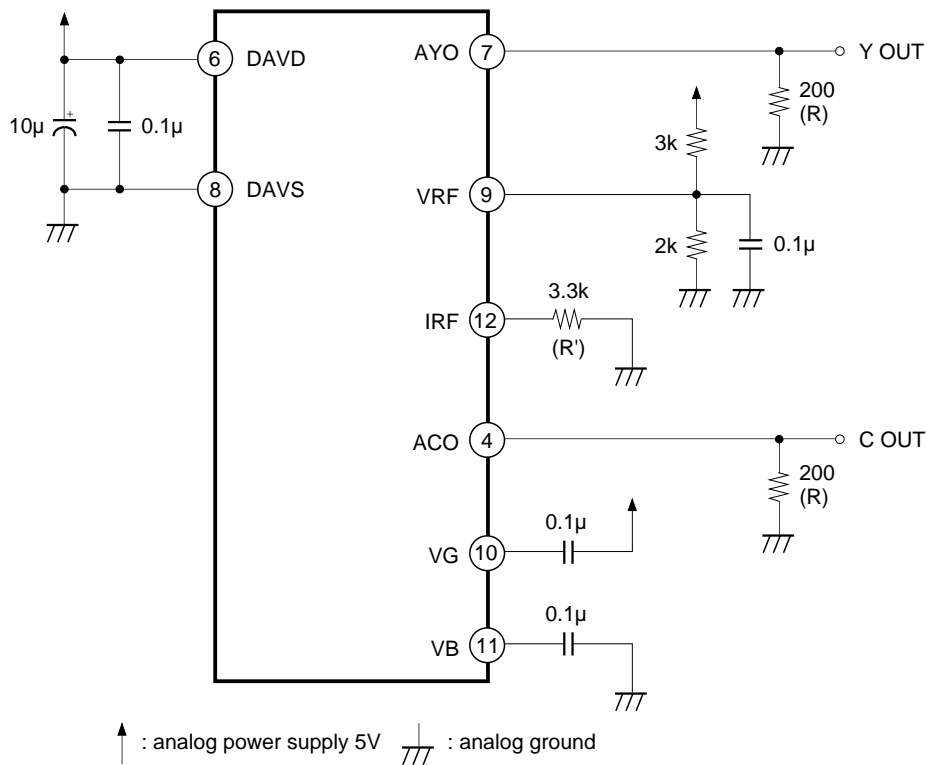
- Method of selecting output resistance

  The CXD2073Q has a built-in current output-type D/A converter. To obtain the output voltages, connect resistors to AYO and ACO pins.

  $$VFS = IFS \times R$$

  Here, VFS is output full-scale voltage, IFS is output full-scale current, and R is the output resistance connected to each IO.

  In addition, connect a resistance of 16 times the output resistor to the reference current pin IRF. In the case where the value comes to be impractical, use a value of resistance as close to the value calculated as possible. At that time,

  $$VFS = VRF \times 16 \times R/R'.$$

  R is the output resistance connected to each IO, R' is the resistance connected to IRF, and VRF is the VRF pin voltage. Power consumption can be reduced by using higher resistance values, but then glitch energy and data settling time increase contrastingly. Select optimum resistance values according to the system applications.

  In case of the circuit above, $VFS = 2 \, [V] \times 16 \times 0.2k/3.3k \approx 1.93 \, [V]$, $IFS = 1.93/0.2k \approx 9.65 \, [mA]$.

Notes on Operation

- Power supply, ground

  Separate the analog and digital systems around the device to reduce noise effect. Both analog and digital VDD are respectively bypassed to Vss as close to these VDD and Vss pins as possible through ceramic capacitors of approximately 0.1µF.

  Also, layout the power supply and ground pattern of the board substrate as wide as possible to lower impedance.

- Clock

  Use the burst-locked clock. Separate the clock line on the board substrate as far as possible from analog-related pins, analog power supply, and analog ground.

External Connection
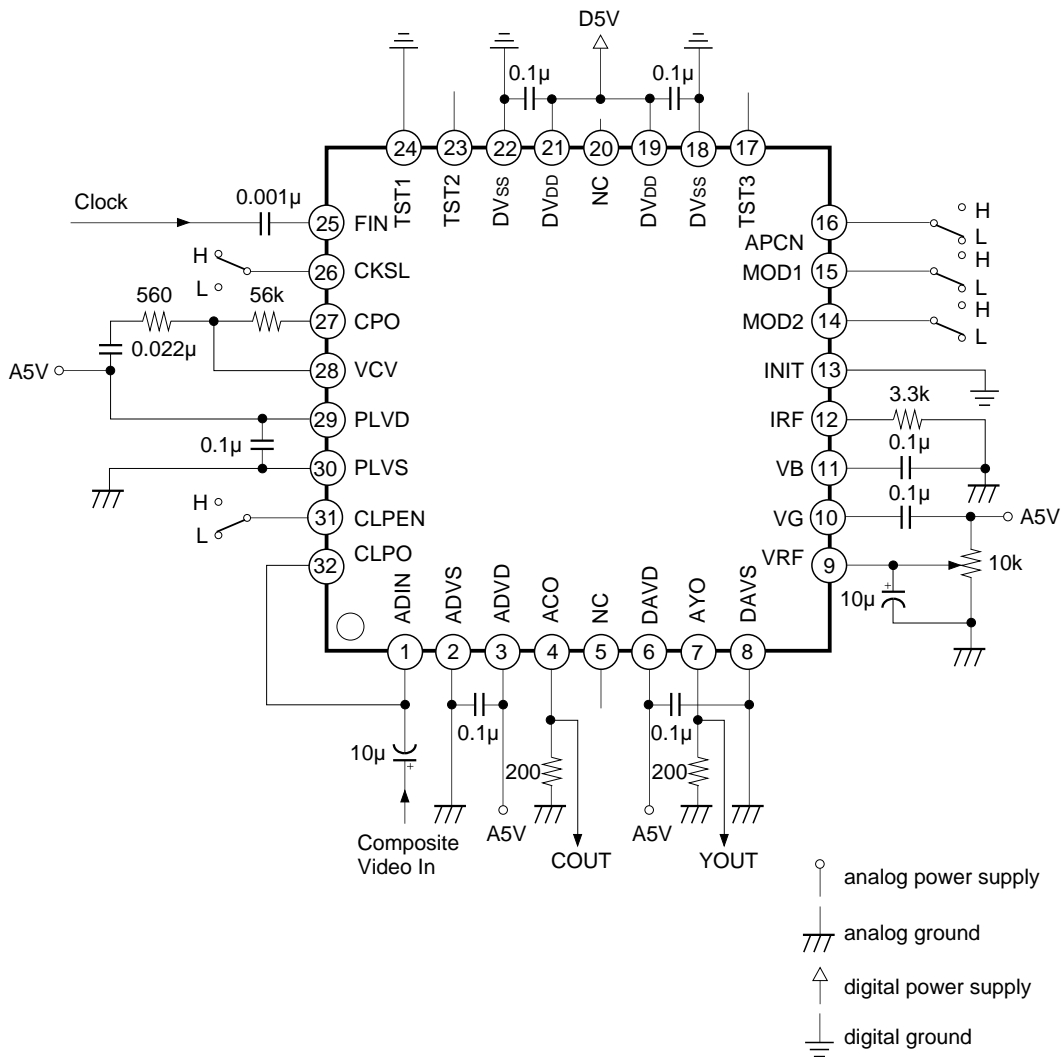
Selected Pins

| Pin No.	Symbol	H	L
14 15	MOD2 MOD1	Combination of MOD1 and MOD2 (MOD1, MOD2) = (L, L) Normal mode (L, H) Y through mode (H, L) BPF mode (L, H) Simple comb mode	
16	APCN	Horizontal aperture compensation ON	Horizontal aperture compensation OFF
26	CKSL	Internal quadruple PLL is used	Internal quadruple PLL is not used
31	CLPEN	Internal clamp is not used	Internal clamp is used

Application Circuit

(1) In case that fsc is used as clock
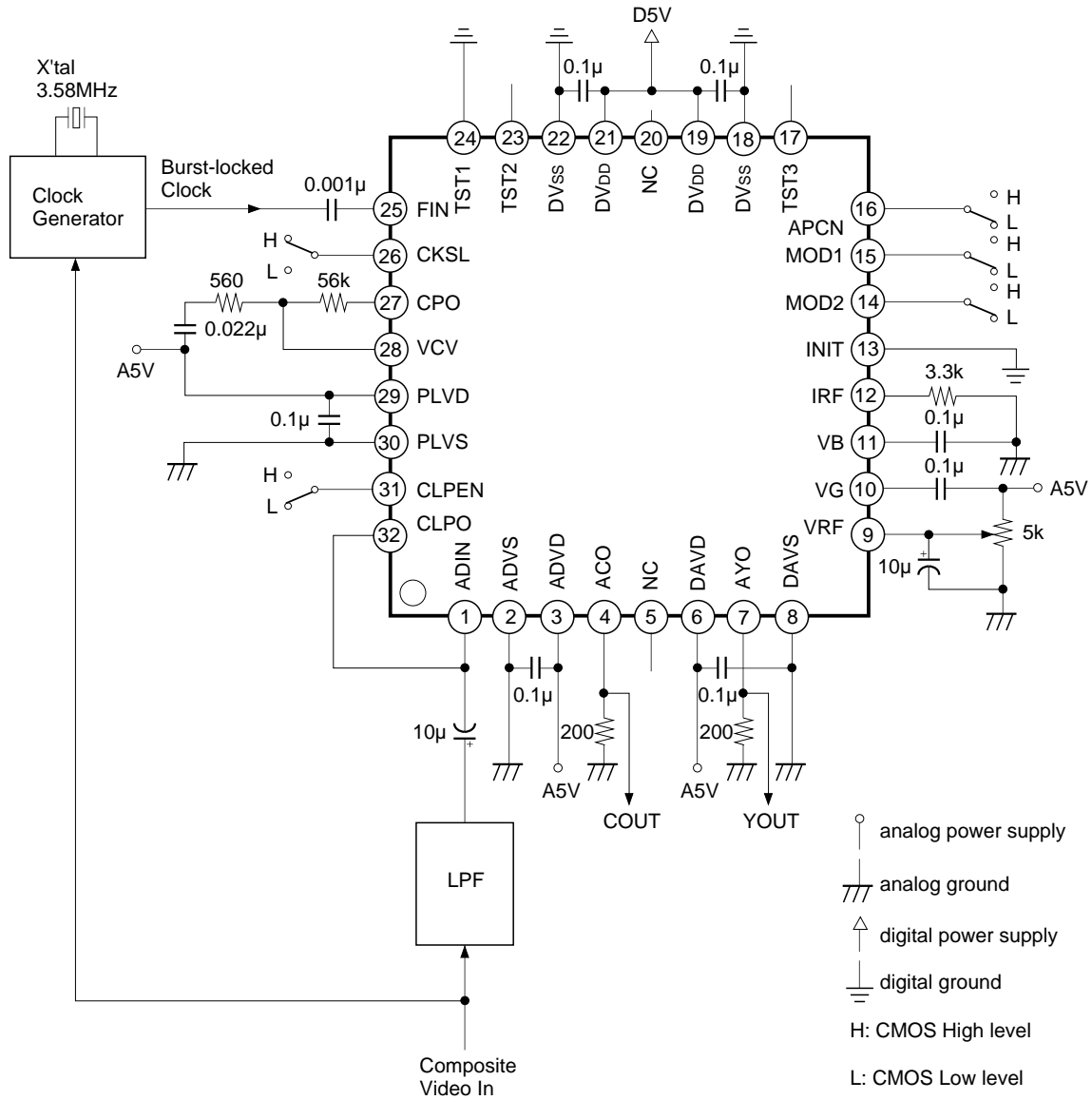
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.
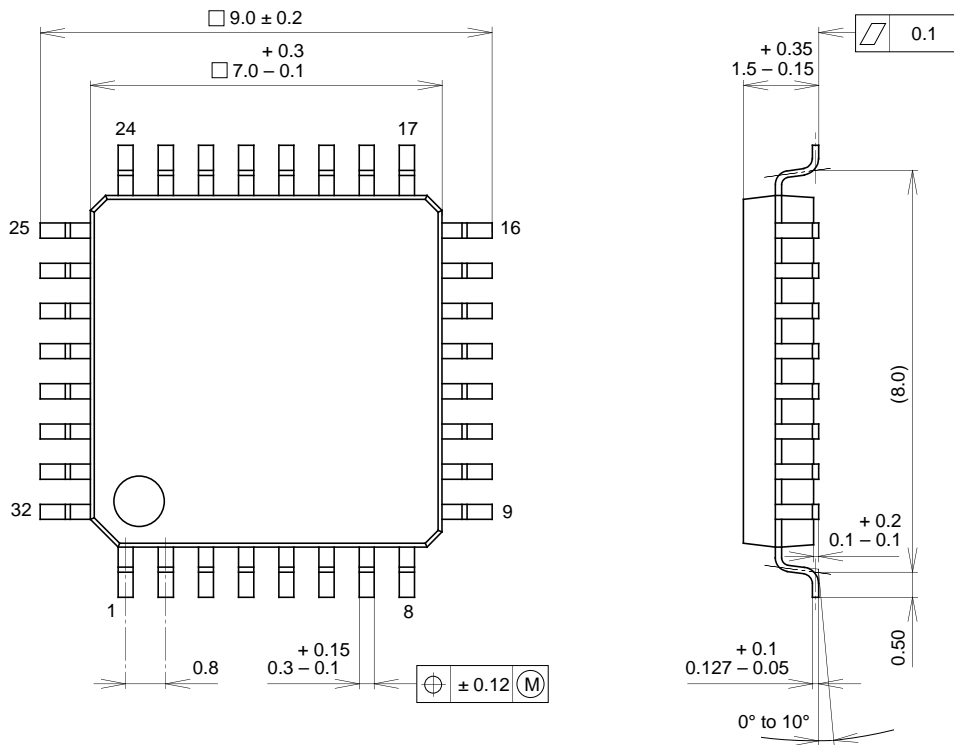
(2) In case that 4fsc is used as clock
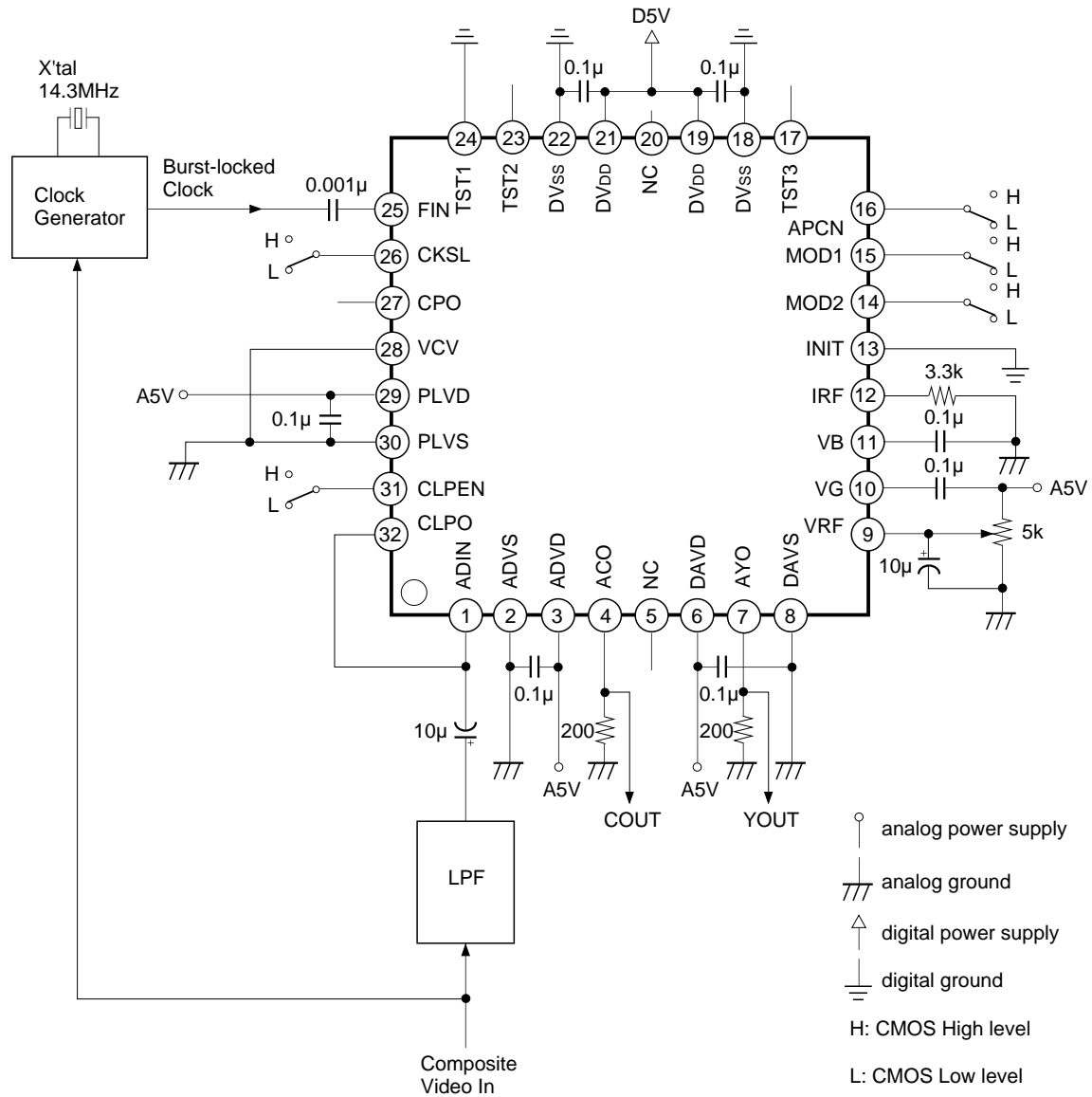
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline   Unit: mm

32PIN QFP (PLASTIC)

SONY CODE	QFP-32P-L01
EIAJ CODE	*QFP032-P-0707-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2g