

Digital Comb Filter (NTSC)

Description

The CXD2043Q is an adaptive comb filter compatible with NTSC system, and can provide high-precision Y/C separation with a single-chip.

Features

- Y/C separation by adaptive processing
- Horizontal aperture compensation circuit
- 8-bit A/D converter (1-channel)
- 8-bit D/A converter (2-channel)
- Two 1H delay lines
- 4-PLL

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

- Supply voltage

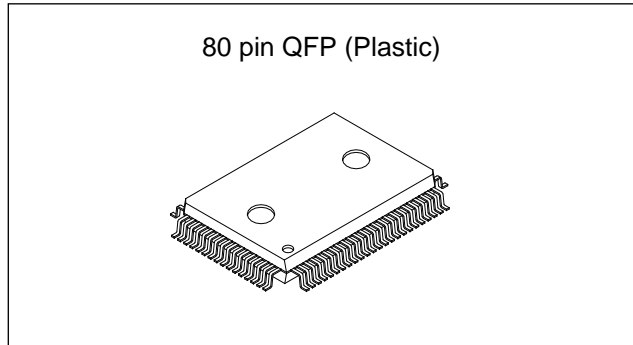
DVDD	Vss - 0.5 to +7.0	V
YVDD	Vss - 0.5 to +7.0	V
CVDD	Vss - 0.5 to +7.0	V
PVDD	Vss - 0.5 to +7.0	V
- Input voltage

Vi	Vss - 0.5 to VDD + 0.5	V
----	------------------------	---
- Output voltage

Vo	Vss - 0.5 to VDD + 0.5	V
----	------------------------	---
- Operating temperature

Topr	-20 to +75	°C
------	------------	----
- Storage temperature

Tstg	-55 to +150	°C
------	-------------	----



Recommended Operating Conditions

- Supply voltage

DVDD	5.0 ± 0.25	V
YVDD	5.0 ± 0.25	V
CVDD	5.0 ± 0.25	V
PVDD	5.0 ± 0.25	V
- Operating temperature

Topr	-20 to +75	°C
------	------------	----

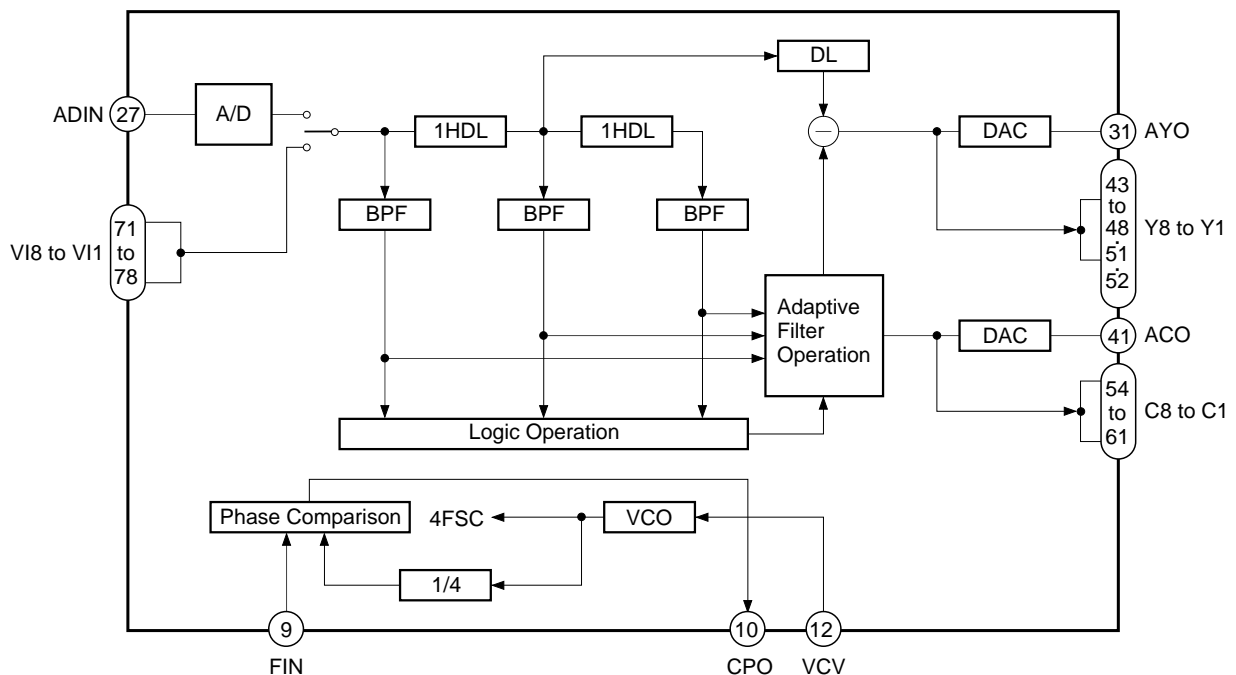
Structure

Silicon gate CMOS IC

Applications

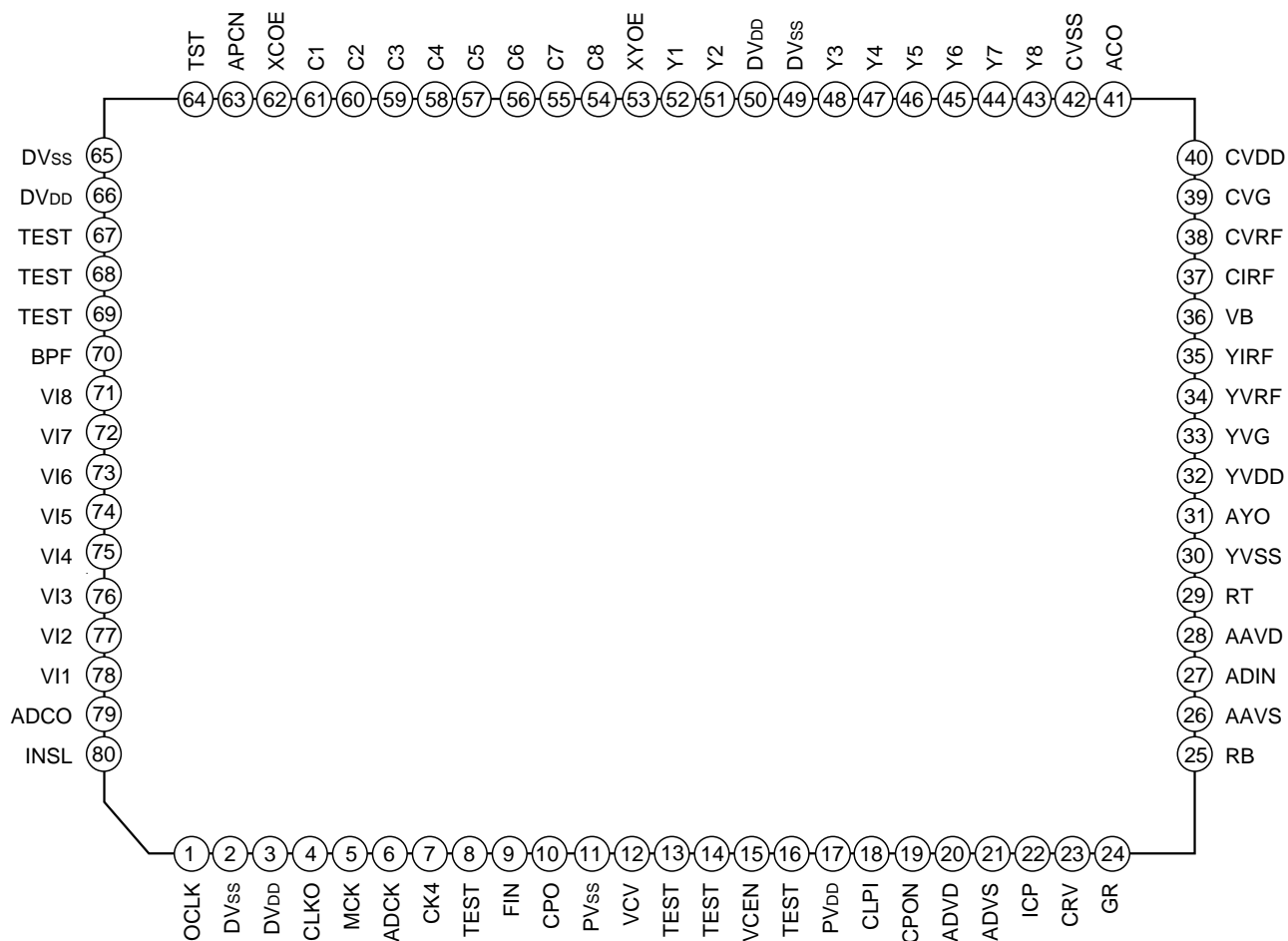
Y/C separation for color TVs and VCRs

Block Diagram



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Pin Configuration



Pin Description

Pin No.	Symbol	I/O	Description
1	OCLK	I	Clock amplifier input. Input at 0.8Vp-p or more by eliminating DC components with a capacitor.
2	DVSS	—	Digital ground
3	DVDD	—	Digital power supply
4	CLKO	O	Clock amplifier output. Left open when the clock amplifier is not used.
5	MCK	I	Master clock input
6	ADCK	I	Clock input for A/D converter. Input the same clock signal as for Pin 5.
7	CK4	O	4FSC clock output. Generated from the built-in 4-PLL.
8	TEST	I	Test. Fix to Low.
9	FIN	I	FSC clock input. Input FSC which is burst-locked. Connect to DVSS when the PLL is not used.
10	CPO	O	Phase comparison output for the built-in PLL. Left open when the PLL is not used.
11	PVSS	—	PLL analog ground

Pin No.	Symbol	I/O	Description
12	VCV	I	Control voltage input for the built-in VCO oscillation. Connect to PVSS when the PLL is not used.
13	TEST	I	Test. Fix to Low.
14	TEST	I	Test. Fix to Low.
15	VCEN	I	Built-in VCO oscillation enable. Connect to PVDD when using the PLL. Connect to PVSS when the PLL is not used.
16	TEST	O	Test. Left open.
17	PVDD	—	PLL analog power supply
18	CLPI	I	Clamp pulse input for A/D converter (negative polarity). Connect to DVDD when the clamp is off.
19	CPON	I	High: Clamp function is set to off, and only the normal A/D converter function is enabled. Low: Clamp function is enabled.
20	ADVD	—	Digital power supply for A/D converter
21	ADVS	—	Digital ground for A/D converter
22	ICP	I	Clamp control voltage
23	CRV	I	Clamp reference voltage input
24	GR	—	Connect to analog ground.
25	RB	O	A/D converter reference voltage (bottom)
26	AAVS	—	Analog ground for A/D converter
27	ADIN	I	Comb filter analog input (A/D converter input)
28	AAVD	—	Analog power supply for A/D converter
29	RT	O	A/D converter reference voltage (top)
30	YVSS	—	Analog ground for Y-D/A converter
31	AYO	O	Analog luminance signal output
32	YVDD	—	Analog power supply for Y-D/A converter
33	YVG	O	Connect to YVDD via a capacitor of approximately 0.1 μ F.
34	YVRF	I	VRF for Y. Sets the output full-scale value for Y.
35	YIRF	I	Connect a resistor of 16 times (16R) that of the output resistor "R" of AYO pin.
36	VB	O	Connect to YVSS via a capacitor of approximately 0.1 μ F.
37	CIRF	O	Connect a resistor of 16 times (16R) that of the output resistor "R" of ACO pin.
38	CVRF	I	VRF for C. Sets the output full-scale value for C.
39	CVG	O	Connect to CVDD via a capacitor of approximately 0.1 μ F.
40	CVDD	—	Analog power supply for C-D/A converter
41	ACO	O	Analog chroma signal output
42	CVSS	—	Analog ground for C-D/A converter
43	Y8	O	Digital luminance signal output (MSB)
44	Y7	O	Digital luminance signal output
45	Y6	O	Digital luminance signal output

Pin No.	Symbol	I/O	Description
46	Y5	O	Digital luminance signal output
47	Y4	O	Digital luminance signal output
48	Y3	O	Digital luminance signal output
49	DV _{SS}	—	Digital ground
50	DV _{DD}	—	Digital power supply
51	Y2	O	Digital luminance signal output
52	Y1	O	Digital luminance signal output (LSB)
53	XYOE	I	Digital luminance signal output control High: High impedance Low: Standard output
54	C8	O	Digital chroma signal output (MSB)
55	C7	O	Digital chroma signal output
56	C6	O	Digital chroma signal output
57	C5	O	Digital chroma signal output
58	C4	O	Digital chroma signal output
59	C3	O	Digital chroma signal output
60	C2	O	Digital chroma signal output
61	C1	O	Digital chroma signal output (LSB)
62	XCOE	I	Digital chroma signal output control. High: High impedance Low: Standard output
63	APCN	I	Aperture compensation switching. High: Aperture compensation ON Low: Aperture compensation OFF
64	TST	I	Y output through mode. High: Outputs the input composite video signal from the Y output. At this time, there is 1H + 18 clock delay from the input. Low: Y/C separation mode
65	DV _{SS}	—	Digital ground
66	DV _{DD}	—	Digital power supply
67	TEST	I	Test. Fix to Low.
68	TEST	I	Test. Fix to Low.
69	TEST	I	Test. Fix to Low.
70	BPF	I	High: Fixed to BPF separation Low: Standard mode
71	V18	I	Digital composite video input (MSB)
72	V17	I	Digital composite video input
73	V16	I	Digital composite video input
74	V15	I	Digital composite video input
75	V14	I	Digital composite video input
76	V13	I	Digital composite video input

Pin No.	Symbol	I/O	Description
77	VI2	I	Digital composite video input
78	VI1	I	Digital composite video input (LSB)
79	ADCO	I	High: Video signals taken in form A/D converter are output from the Y output pins (Y8 to Y1) as 8-bit digital data with a 3.5 clock delay. Low: Normal mode
80	INSL	I	Input switching. High: Digital input Low: Analog input.

Electrical Characteristics

DC Characteristics

(V_{DD} = 5 ± 0.25V, V_{SS} = 0V, Ta = -20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	DV _{DD}	—	4.75	5.0	5.25	V
	AAVD					
	ADVD					
	YVDD					
	CVDD					
Operating temperature	Topr	—	-20	—	+75	°C
Supply current	I _{DD}	Clock 14MHz	—	—	80	mA
High level input voltage	V _{IH}	CMOS level	V _{DD} × 0.7	—	V _{DD}	V
Low level input voltage	V _{IL}	CMOS level	V _{SS}	—	V _{DD} × 0.3	V
High level output voltage	V _{OH}	I _{OH} = -2mA	V _{DD} - 0.8	—	V _{DD}	V
		I _{OH} = -4mA (Pins 4, 7)				
Low level output voltage	V _{OL}	I _{OL} = 4mA	V _{SS}	—	0.4	
		I _{OL} = 8mA (Pins 4, 7)				
Logical V _{th}	LV _{th}	OCLK (Pin 1)	—	V _{DD} /2	—	V
Input voltage	V _{IN}		0.8	—	V _{DD}	V _{p-p}
Feedback resistor	R _{FB}		250k	1M	2.5M	Ω

AC Characteristics

(V_{DD} = 5 ± 0.25V, V_{SS} = 0V, Ta = -20 to +75°C, C_L = 20pF)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data setup time	t _{dsu}	MCK → VI [8 : 1]	15.0	—	—	ns
Data hold time	t _{dh}	MCK → VI [8 : 1]	10.0	—	—	ns
Propagation delay time	t _{pd}	MCK → Y [A : 1]	—	—	40	ns
		MCK → C [A : 1]				
Clock frequency	f	—	14	4fsc	15	MHz

Pin Capacitance

(Ta = 25°C, f = 1MHz, V_{IN} = V_{OUT} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	—	—	—	9	pF
Output capacitance	C _{OUT}	—	—	—	11	pF

ADC Characteristics(V_{DD} = 5V, T_a = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	f _{max}		14.3	—	—	MSPS
Analog input band width	BW	-3dB	—	18	—	MHz
Self bias	VRB		0.48	0.52	0.56	V
	VRT - VRB		1.96	2.08	2.22	V
Propagation delay time	t _{pd}		—	—	45	ns
Differential linearity error	E _D		-1.0	—	+1.0	LSB
Integral linearity error	E _L		-3.0	—	+3.0	LSB
Clamp offset voltage	EOC	V _{REF} = VRB	-20	0	+20	mV
		V _{REF} = VRT	-30	-10	+10	mV

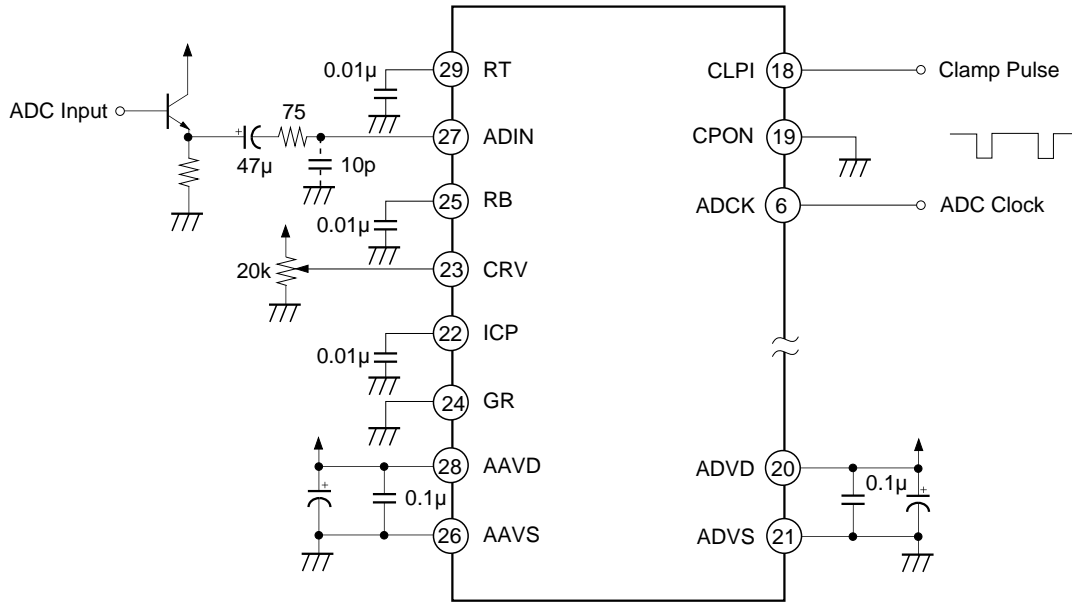
DAC Characteristics(V_{DD} = 5V, V_{RF} = 2V, I_{RF} = 3.3kΩ, R = 200Ω, T_a = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n	—	—	8	—	bit
Max. conversion speed	f _{max}	—	14.3	—	—	MSPS
Differential linearity error	E _D	—	-0.5	—	+0.5	LSB
Integral linearity error	E _L	—	-1.5	—	+1.5	LSB
Output full-scale voltage	V _{FS}	—	1.805	1.90	1.995	V
Output full-scale current	I _{FS}	—	—	9.5	15	mA
Output offset voltage	V _{OS}	—	—	—	1.0	mV
Precision guaranteed output voltage range	V _{OC}	—	1.8	—	2.1	V
Glitch energy	GE	*1	—	30	—	pV-s

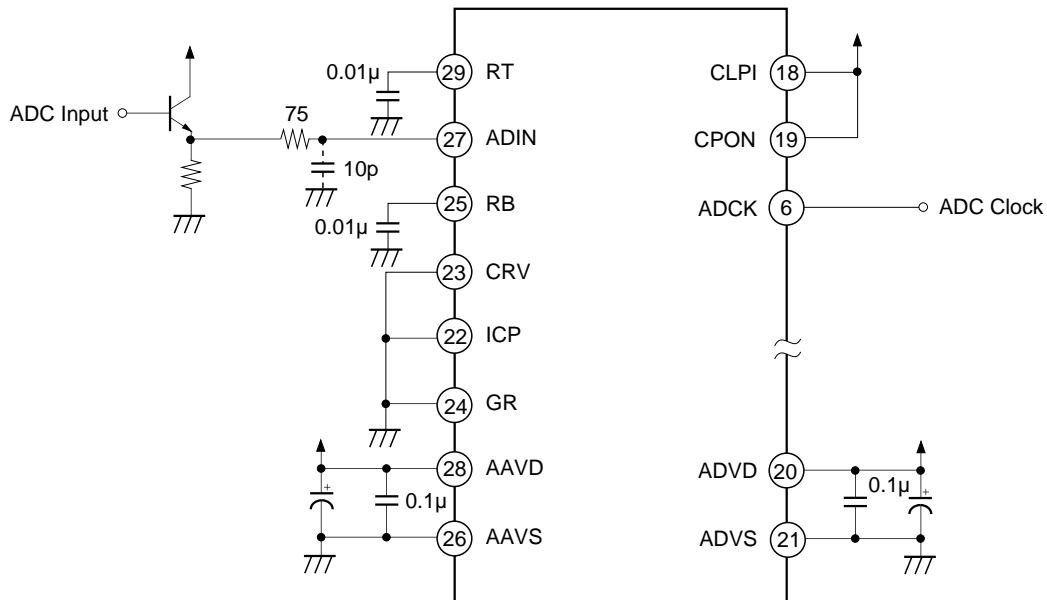
*1 R = 75Ω, 1Vp-p output

Application Circuit for A/D Converter

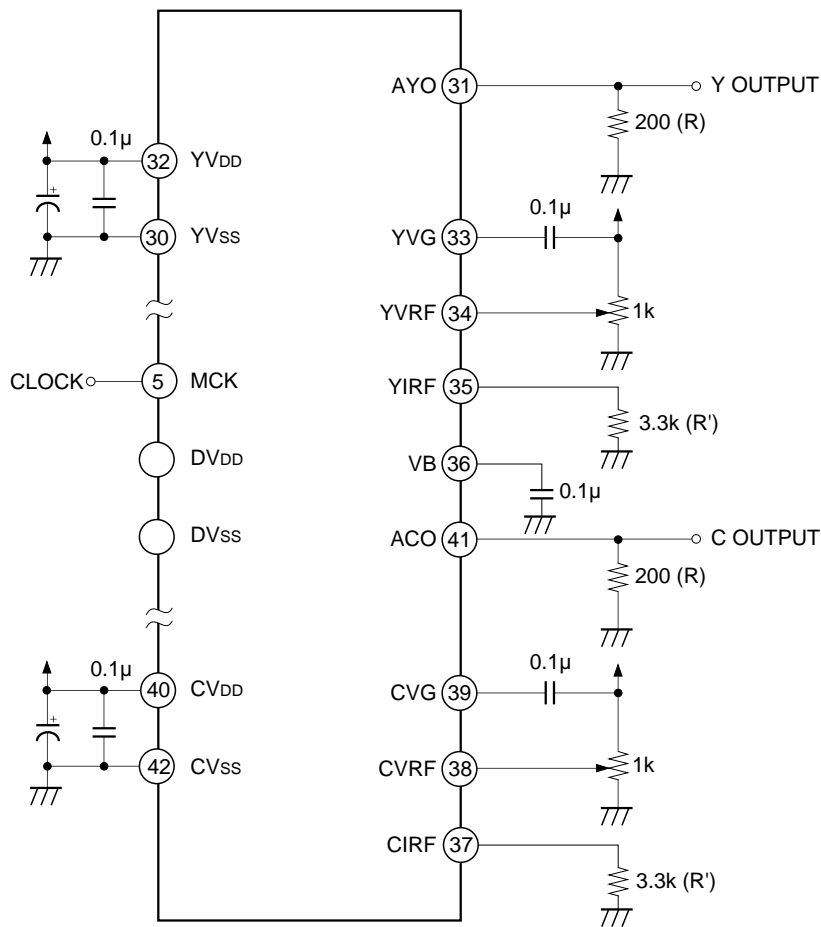
(1) In the case of input clamp pulse directly.



(2) In the case of not using the internal clamp circuit



Application Circuit for D/A Converter



• Method of Selecting Output Resistance

The CXD2043Q has a built-in current output-type D/A converter. To obtain the output voltages, connect resistances to AYO and ACO pins.

The voltage and current specifications are:

Output full-scale voltage: $V_{FS} = 0.5$ to $2.0V$

Output full-scale current: $I_{FS} = 0$ to $15mA$

Calculate the output resistance using the relationship $V_{FS} = I_{FS} \times R$. In addition, connect a resistance of 16 times the output resistance to the reference current pin (YIRF, CIRF). In the case where the value comes to be impractical, use a value of resistance as close to the value calculated as possible.

Note that, at this time, $V_{FS} = V_{RF} \times 16R/R'$ (V_{RF} : Pin voltage of YVRF and CVRF).

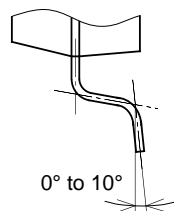
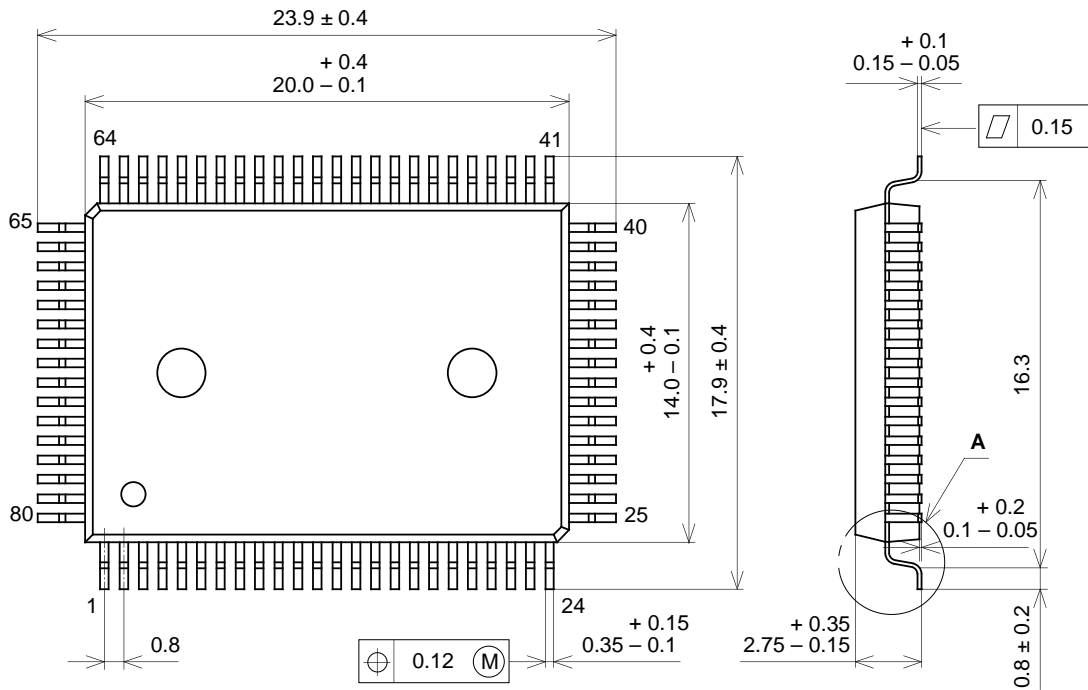
R is the resistance connected to AYO/ACO, and R' is the resistance connected to YIRF/CIRF. Power consumption can be reduced by using higher resistance values, but then glitch energy and data settling time increase contrastingly. Select optimum resistance values according to the system applications.

• VDD, VSS

Separate the analog and digital systems around the device to reduce noise effect. YVDD and CVDD are respectively by-passed to YVSS and CVSS as close to each other as possible through ceramic capacitor of approximately $0.1\mu F$.

Package Outline Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g