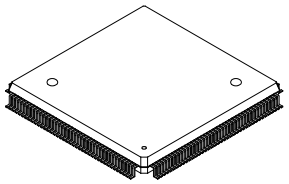
IEEE1394 LINK Layer / PCI Bridge LSI

Overview

The CXD1947Q is a single-chip implementation of the link layer protocol of the 1394 Serial Bus, with additional features to support the transaction and bus management layers.

The CXD1947Q includes a PCI bus interface and multiple DMA engines to enable high performance bus transfers.

160 pin QFP



Features

- 1394 Link Layer/PCI Bridge
- Conforms to IEEE1394 high speed Serial Bus
- Supports 100Mb/s and 200Mb/s 1394 bus speeds
- Conforms to PCI version 2.1 specification
- Supports 6 independent programmable DMA channels
  - — Asynchronous transmit (1)
  - — Asynchronous receive (1)
  - — Isochronous transmit (2)
  - — Isochronous receive (2)
- Three 128-word-deep FIFOs
  - — Asynchronous transmit
  - — Isochronous transmit
  - — Receive
- Includes interfaces to
  - — 1394 PHY interface (CXD1944 or equivalent)
  - — ROM (64K x 8)
  - — Silicon Serial ROM
- Supports big and little Endian data formats

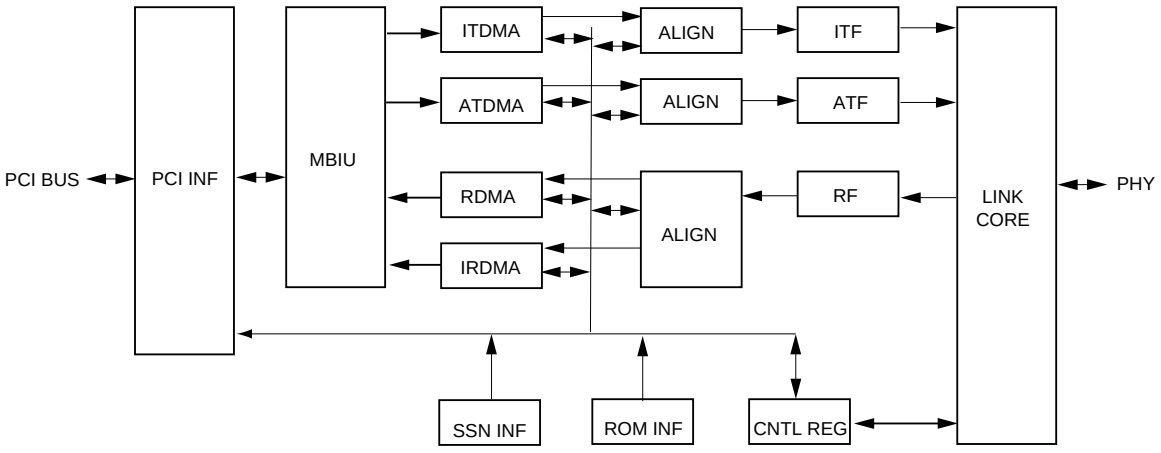
Device Structure

Silicon gate CMOS IC

Recommended Operating Conditions

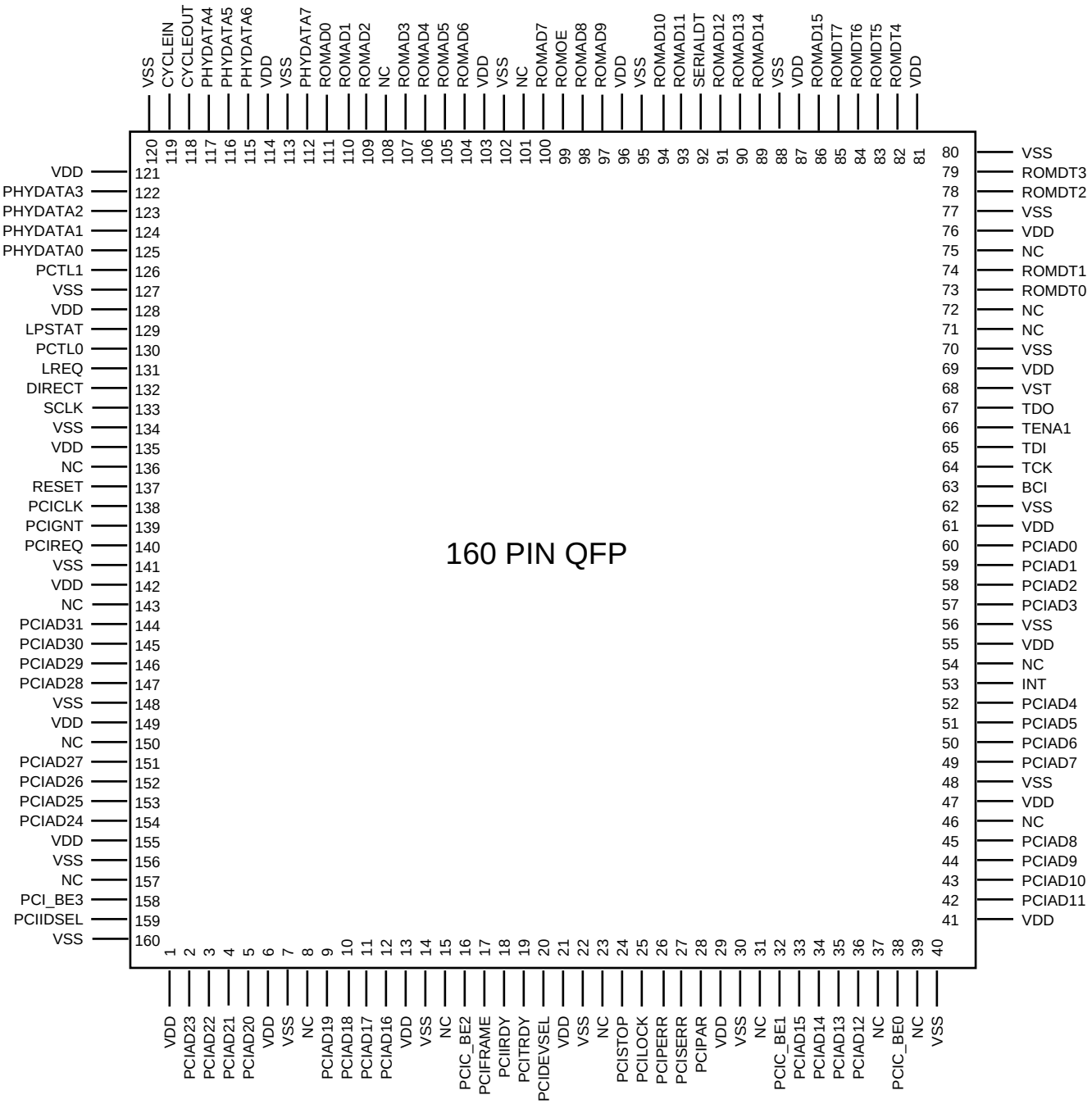
• Supply voltage	V_{DD}	3.0 to 3.6	V
• Operating temperature range	Topr	–20 to +75	°C

Block Diagram



MBIU:	Master Bus Interface	ALIGN:	Data Aligner	PHY:	Link Layer/Physical Layer 1394 Interface
ITDMA:	Isochronous Transmit DMA	ITF:	Isochronous Transmit FIFO		
ATDMA:	Asynchronous Transmit DMA	ATF:	Asynchronous Transmit FIFO	ROM INF:	ROM Interface
RDMA:	Receive DMA	RF:	Receive FIFO	CNTL REG:	Control Registers
IRDMA:	Isochronous Receive DMA	SSN INF:	Silicon Serial Number		

Pin Configuration



Functions

1. Asynchronous Function

The CXD1947Q can transmit and receive all of the defined 1394 packet formats. Packets to be transmitted are read out of host memory and received packets are written into host memory, both using DMA. CXD1947Q can be programmed to act as a bus bridge between PCI and 1394 by directly executing 1394 read and write requests to the first 4GB of node offset address as read and writes to PCI memory space. The CXD1947Q can also be programmed to automatically place the data from read response packets in the proper location in host memory, then optionally interrupt the host processor to indicate that the transaction is complete.

2. Isochronous Function

The CXD1947Q is capable of performing the cycle master function as defined by 1394. This means it contains a cycle timer and counter, and can transmit a special packet called a “cycle start” after every rising edge of the 8KHz cycle clock. The CXD1947Q can either generate the cycle clock from the 49.152MHz clock it receives from the PHY, or use the “CycleIn” pin directly. When not the cycle master, the CXD1947Q keeps its internal cycle timer synchronized with the cycle master node by correcting its own cycle timer with the reload value from the cycle start packet. The CXD1947Q supports two isochronous transmit channels and two isochronous receive channels. The CXD1947Q can regulate the rate of transmit to emulate data rates which are synchronous with, but not even multiples of, the 8KHz cycle clock.

3. PCI Interface

This block acts both as a master and a slave on the PCI bus. As a slave, it decodes and responds to accesses to registers within CXD1947Q. As a master, it acts on behalf of the DMA units to generate transactions on the PCI bus. These transactions are used to move streams of data between system memory and the devices, as well as to read and write the DMA command lists.

4. DMA

The CXD1947Q supports six independent DMA channels: one Asynchronous Transmit channel, one Asynchronous Receive channel, and four Isochronous channels. The CXD1947Q also has Physical DMA capability to respond to incoming requests to physical addresses. The DMA unit is made up of three controller modules which support these various DMA functions. Each module has access to the PCI Interface to perform move operations, and is capable of sequencing through buffer descriptor lists stored in main memory in order to find the next buffer address after a channel exhausts the previous buffer. This frees the system from stringent interrupt response requirements after buffer completions.

Each DMA controller stores the current channel program pointers and the current context for each of its DMA channels. A 32-bit incrementer updates both the Channel Program Pointers and the current buffer pointers. A 16-bit decrementer is used to adjust the count values for the channels. These incrementers and decrementers will be shared if a Controller unit has multiple channels.

5. Miscelleneous Functions

Upon detecting a bus reset, the CXD1947Q automatically turns off the asynchronous transmitter. The receiver remains on so that the CXD1947Q can receive PHY self-ID packets during the self-ID process which immediately follows the 1394 bus reset.

Following the bus reset operation, the CXD1947Q receives the new node ID from the PHY and updates its node ID register. Host system software must explicitly restart the transmitter, presumably after it has corrected the node addresses of any queued-up packets.

The CXD1947Q has an interface to a Dallas Semiconductor Silicon Serial Number™ chip. This interface retrieves a unique serial number which management software then uses to uniquely identify the node for which the CXD1947Q is attached on the 1394 interface.

6. Brief Hardware Description

The block diagram shows the CXD1947Q and its connections in a host system. The CXD1947Q attaches to the host via PCI bus. PCI provides an inexpensive and moderatly high performance point for the connection of I/O devices. PCI is a 32-bit, multiplexed address/data bus, capable of performing 32-bit transfers at a rate of 33MHz.

Package Outline Unit: mm

160 pin QFP (Plastic)