SONY

CXD1159Q

Sync. Signal Generator for Camera

Description

CXD1159Q is a sync. signal generator for consumer video cameras.

32 pin QFP (Plastic)

Features

- Adapts to NTSC or PAL through mode switching.
- Low power consumption.
- Phase comparator and built in inverter for active filter.
- Internal/External sync.

Functions

- Generator of various sync. signals.

Structure

Silicon gate CMOS

Application

- Video cameras

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	V_{SS} * − 0.5 to 7.0	V
• Input voltage	V_I	V_{SS} * − 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} * − 0.5 to V_{DD} + 0.5	V
• Storage temperature	Tstg	− 55 to + 150	°C

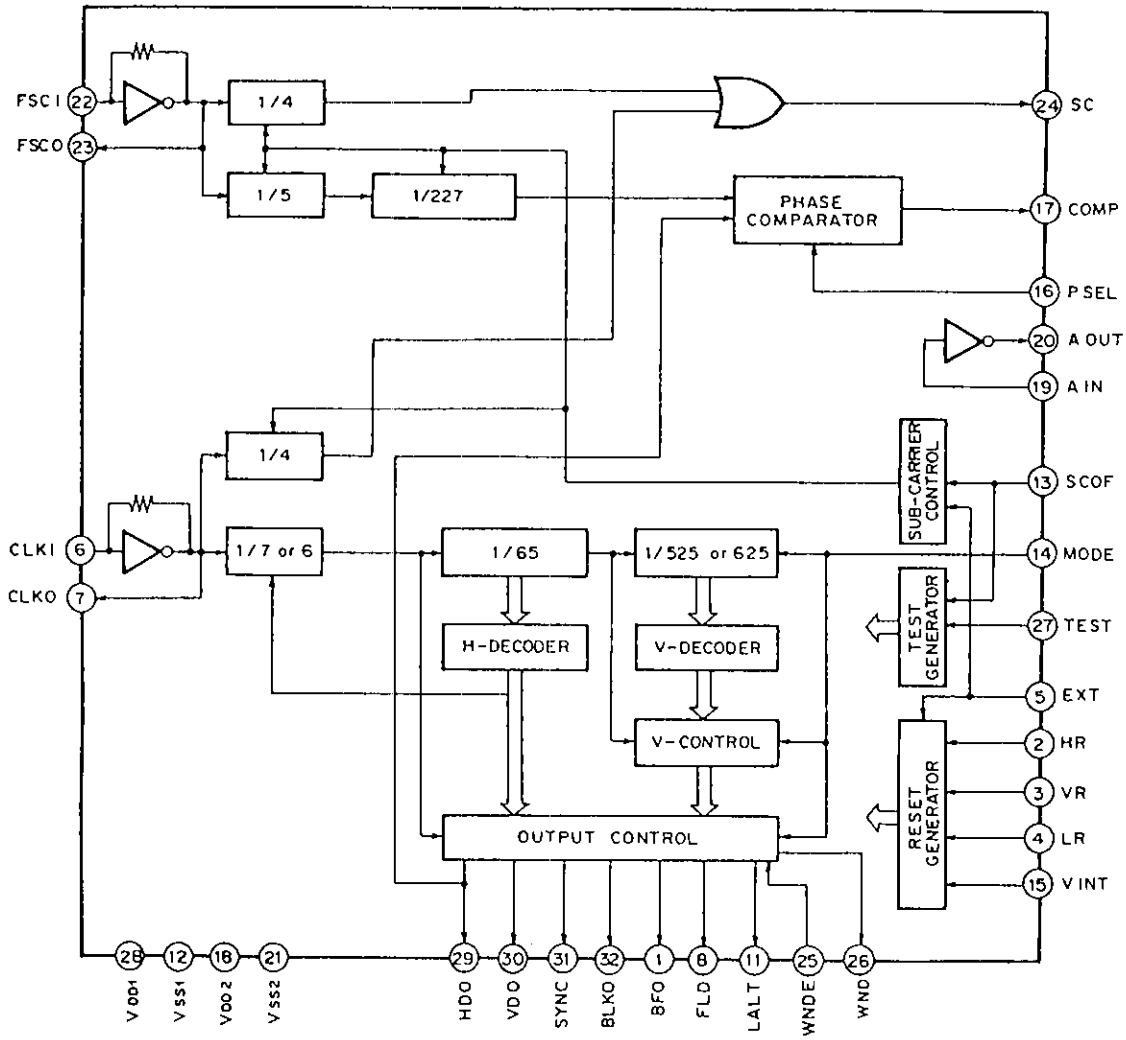
*Vss = 0V

Rcommended Operating Conditions

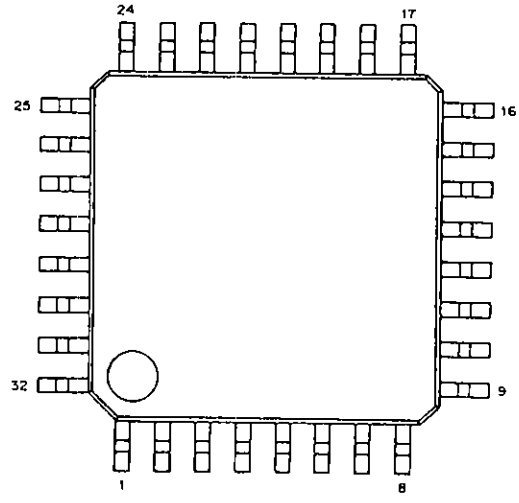
• Supply voltage	V_{DD}	4.5 to 5.5	V
• Operating temperature	Topr	− 20 to + 75	°C

E80924A0X - ST

Block Diagram



Pin Configuration



Pin Description

No.	Symbol	I/O	Description
1	BFO	O	Burst flag pulse
2	HR	I	H reset input
3	VR	I	V reset input
4	LR	I	LALT reset input
5	EXT	I	Internal/External mode switching $\overline{INT}$/EXT
6	CLKI	I	Clock input (NTSC : 14.31818MHz, PAL : 14.1875MHz)
7	CLKO	O	Clock output
8	FLD	O	Field pulse
9	N.C.	—	
10	N.C.	—	
11	LALT	O	Line alternate pulse
12	V_{SS1}	—	GND
13	SCOF	I	Sub carrier suppress input L : OFF
14	MODE	I	NTSC/PAL mode switching $\overline{NTSC}$/PAL
15	VINT	I	Initialize input
16	PSEL	I	Phase comparator polarity switch
17	COMP	O	Phase comparator output
18	V_{DD2}	—	+5 power supply for filter inverter
19	AIN	I	Input for filter inverter
20	AOUT	O	Output for filter inverter
21	V_{SS2}	—	GND for filter inverter
22	FSCI	I	4 fsc clock input
23	FSCO	O	4 fsc clock output
24	SC	O	Sub carrier output
25	WNDE	I	WND output enable input (at L : Enable)
26	WND	O	Window output
27	TEST	I	Test input (Normally "L")
28	V_{DD1}	—	+5V
29	HDO	O	Horizontal drive pulse
30	VDO	O	Vertical drive pulse
31	SYNC	O	Composite sync. pulse
32	BLKO	O	Composite blanking pulse

Electrical Characteristics

DC characteristics

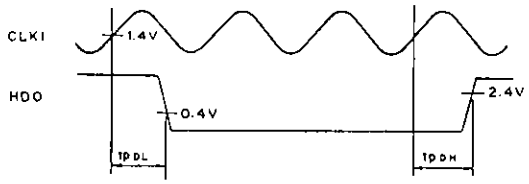
V_{DD} = 5V ± 10%, V_{SS} = 0V, Topr = − 20 to + 75℃

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current		I_{DD}			2.0		mA
		I_{DDS}	Static state*1	0		0.1	mA
Output voltage I *2	H level	V_{OH}	I_{OH} = − 2mA	V_{DD} − 0.5		V_{DD}	V
	L level	V_{OL}	I_{OL} = 4mA	V_{SS}		0.4	V
Output voltage II *3	H level	V_{OH}	I_{OH} = − 1.5mA	2.5		V_{DD}	V
	L level	V_{OL}	I_{OL} = 1.5mA	V_{SS}		2.5	V
Input voltage	H level	V_{IH}		0.7V_{DD}			V
	L level	V_{IL}				0.3V_{DD}	V
Input leak current		I_{LI}	V_I = 0V to V_{DD}	− 10		10	μA
Input leak current *4		I_{LZ}		− 10		10	μA

* 1. $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
* 2. Output pins except "AOUT".
* 3. "AOUT" pin.
* 4. Three state pin.

AC characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Falling edge delay time	t_{PDL}	V_{OL} = 0.4V			45	ns
Rising edge delay time	t_{PDH}	V_{OH} = 2.4V			45	ns

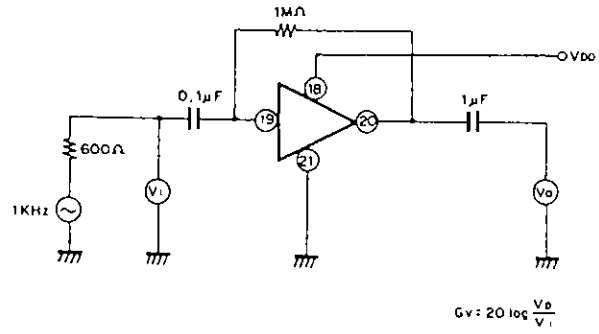


I/O capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			8	pF
Output pin	C_{OUT}			8	pF

Test conditions : $V_{DD} = V_I$ = 0V, f_M = 1MHz

Test circuit



Filter amplifier characteristics

Voltage gain Gv 25dB (Typ.)

Functions

1. Generation of various sync. signals (See the Timing Chart.)

Various sync. signals are generated from clocks.

- Clock frequencies

NTSC : $910f_H$ (14.31818MHz)
PAL : $908f_H$ (14.1875MHz)
$4f_{SC}$ (17.734475MHz)

For the System Clock
NTSC : $910f_H/7$
PAL : $908f_H/7$ or 6

2. PAL PLL for 4fsc

To a master clock of $908f_H$ is matched a phase of $4f_{SC}$. The polarity of the phase comparator can be switched according to the type of external filter (passive or active).

Filter	PSEL	Master ($908f_H$)	$4f_{SC}$	COMP
Passive	L	Fast	Delay	H
		Slow	Fast	L
Active	H	Fast	Delay	L
		Slow	Fast	H

3. SC (Sub-Carrier) generation

Mode	INT or EXT	SC
NTSC	INT	$910f_H/4$
NTSC	EXT	$4f_{SC}/4$
PAL	×	$4f_{SC}/4$

INT : Internal mode
(EXT = L)
EXT : External mode
(EXT = H)

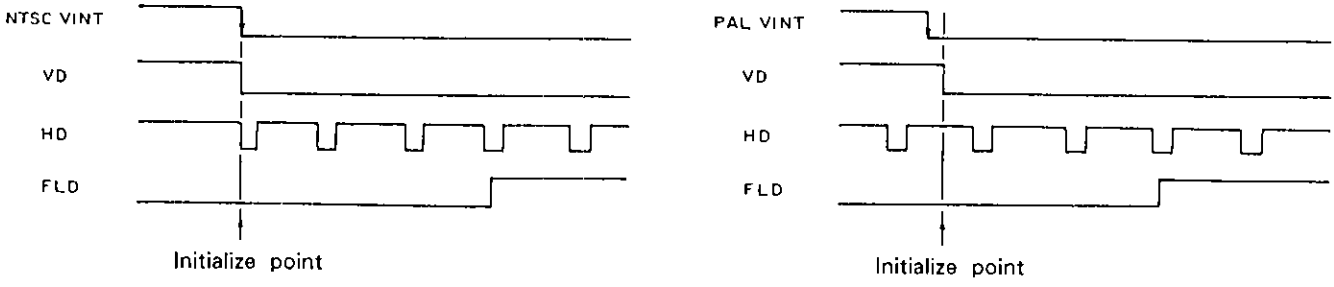
In either mode unused counters are stopped. When SC is not required, by setting SCOF to L all SC counters are stopped and SC is not output.

4. Initialization and Reset

In INT mode the circuit is initialized with the fall of VINT. At that time, H, V and LALT resets are not accepted. In EXT mode, VINT is not accepted, whereas H, V and LALT resets are.

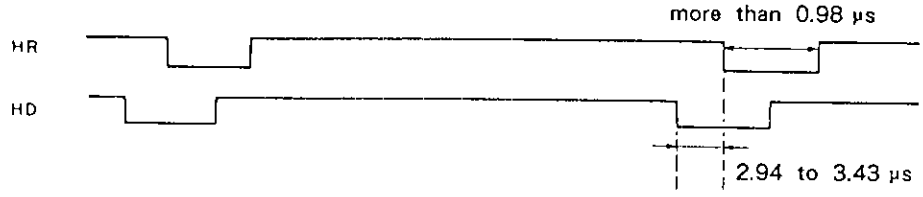
- Initialize (VINT)

  When EXT = L, VINT fall is detected and operation is started as the circuit is initialized at the VD fall position just before field 1. (Initialization is completed within 100ns after the fall is detected).



- H reset (HR)

  Reset is performed with the first fall. However reset is not done anymore unless there is a deviation of more than 2 clocks (0.98 µs) to the subsequent edges.
  The minimum reset pulse width is 0.98 µs.
  HD is reset 2.94 to 3.43 in advance of HR input.

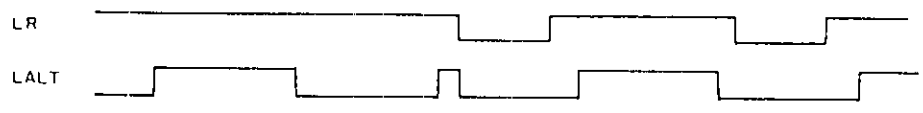


- V reset (VR)

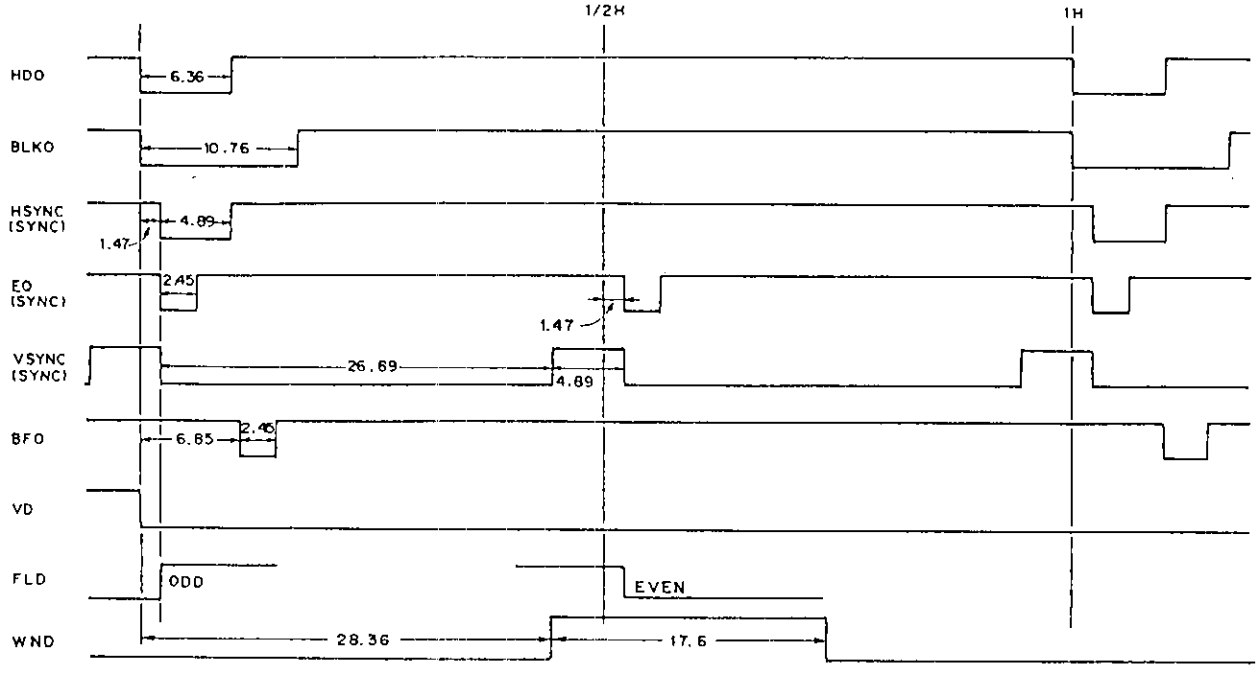
  VD is reset 3.5H in advance of VR input.
  The minimum reset pulse width is 32 µs.

- LALT reset (LR)

  LALT is reset in the same phase as LR input.
  The minimum reset pulse is 32 µs.

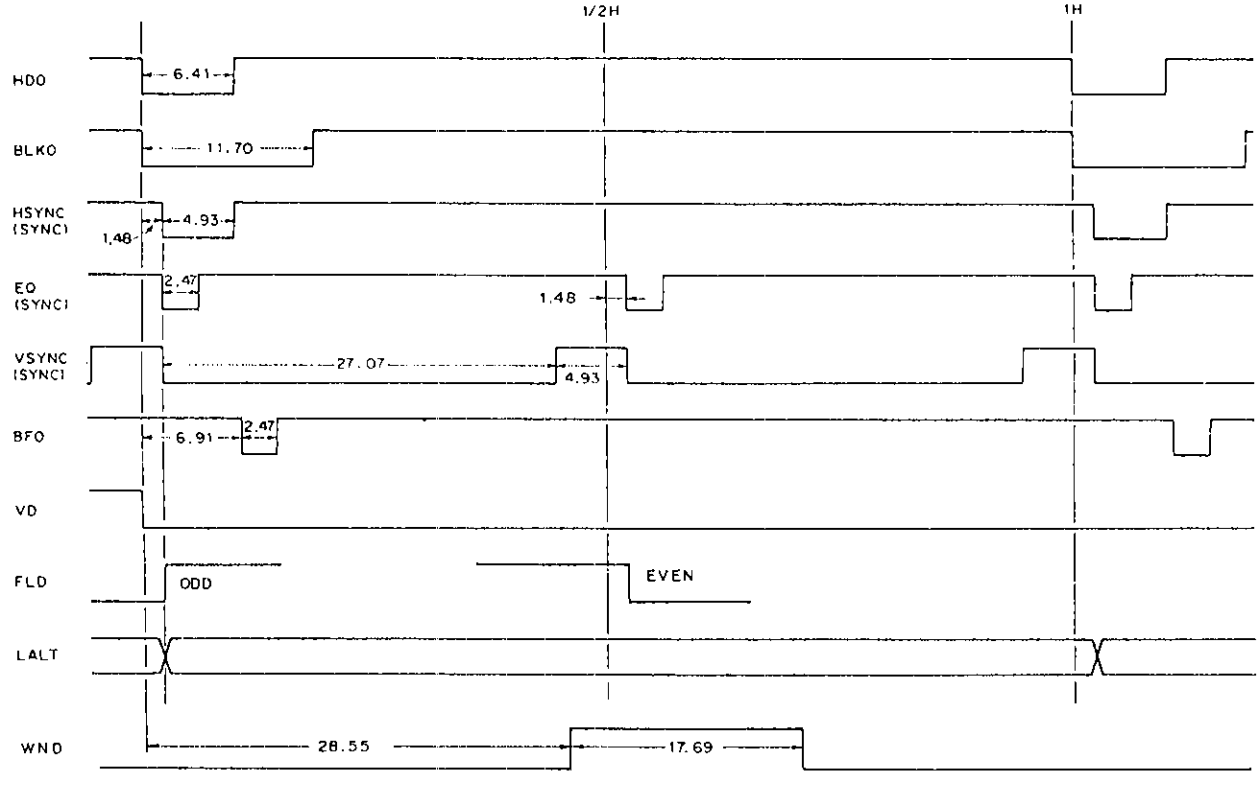


Timing Chart H (NTSC)



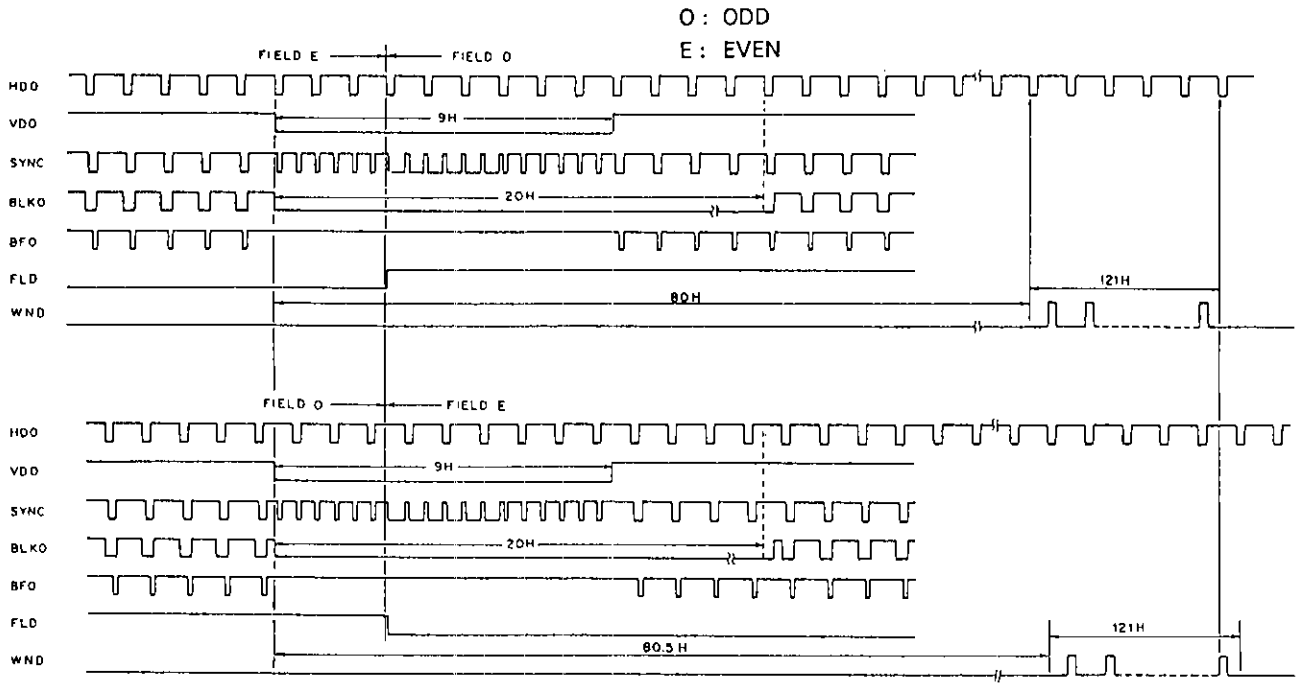
Unit : μs

Timing Chart H (PAL)

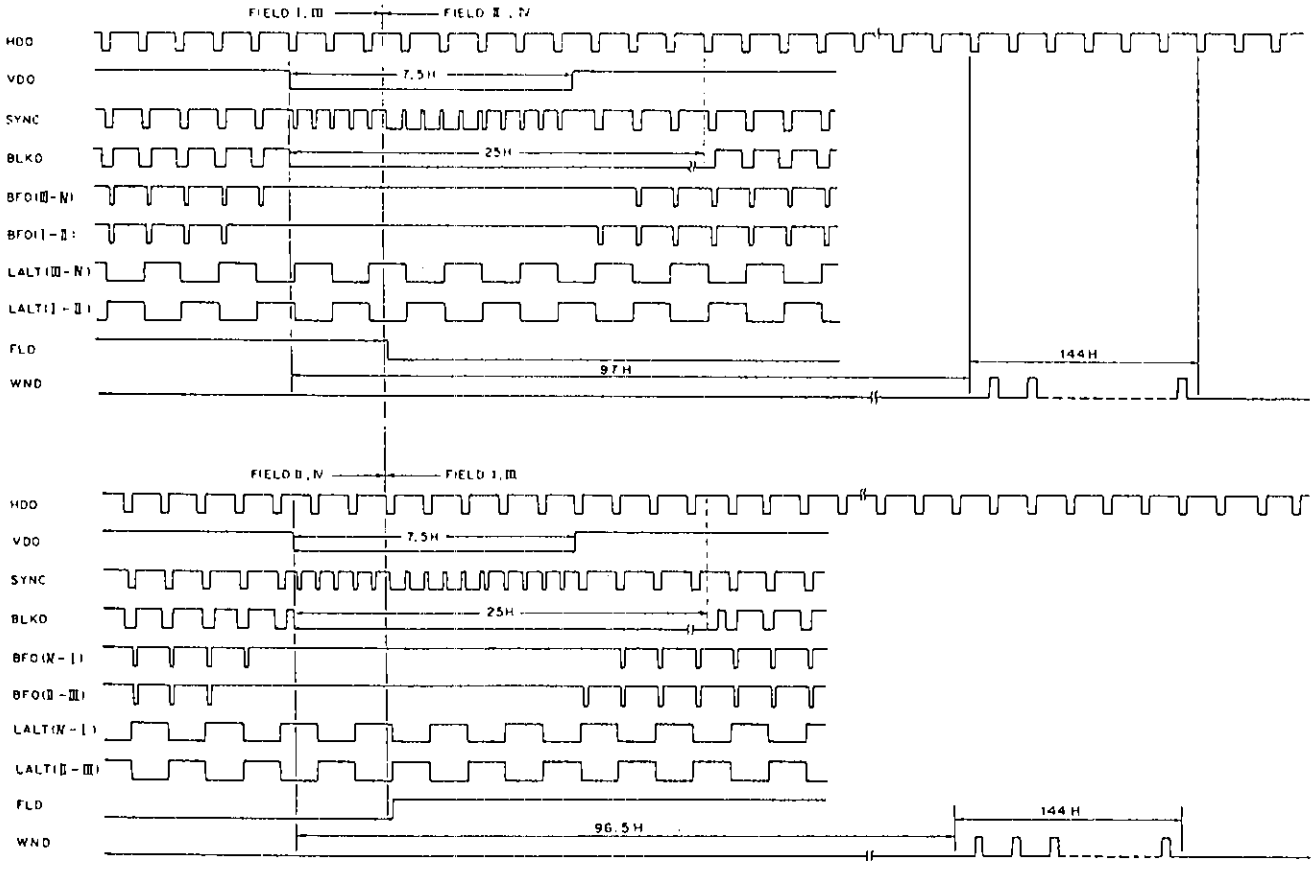


Unit : μs

Timing Chart V (NTSC)

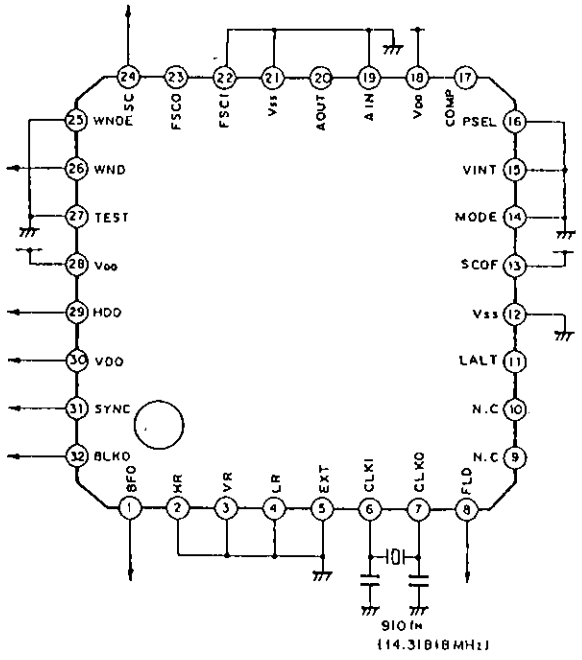


Timing Chart V (PAL)

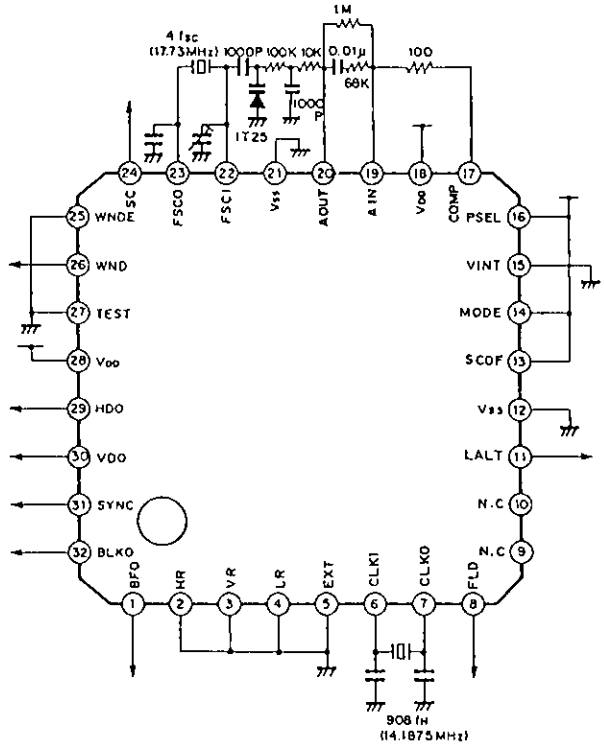


Application Circuit

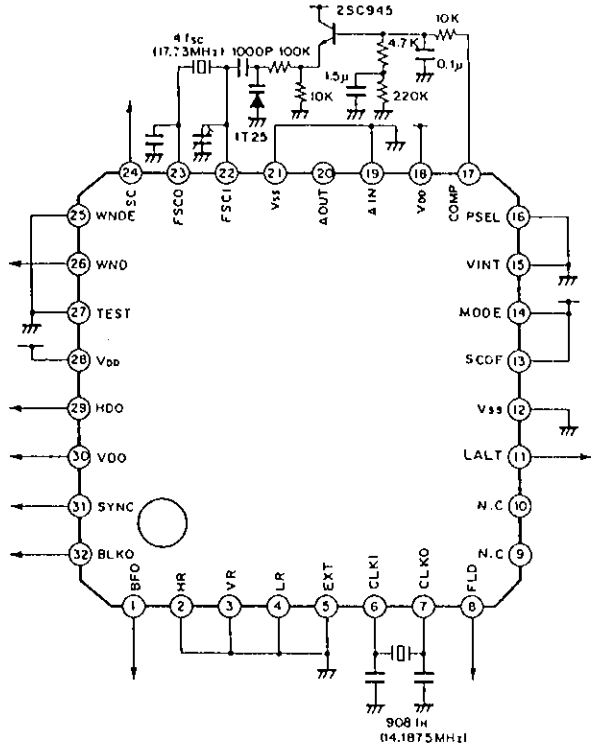
NTSC (Internal mode)



PAL (Filter configuration 2, Internal mode)

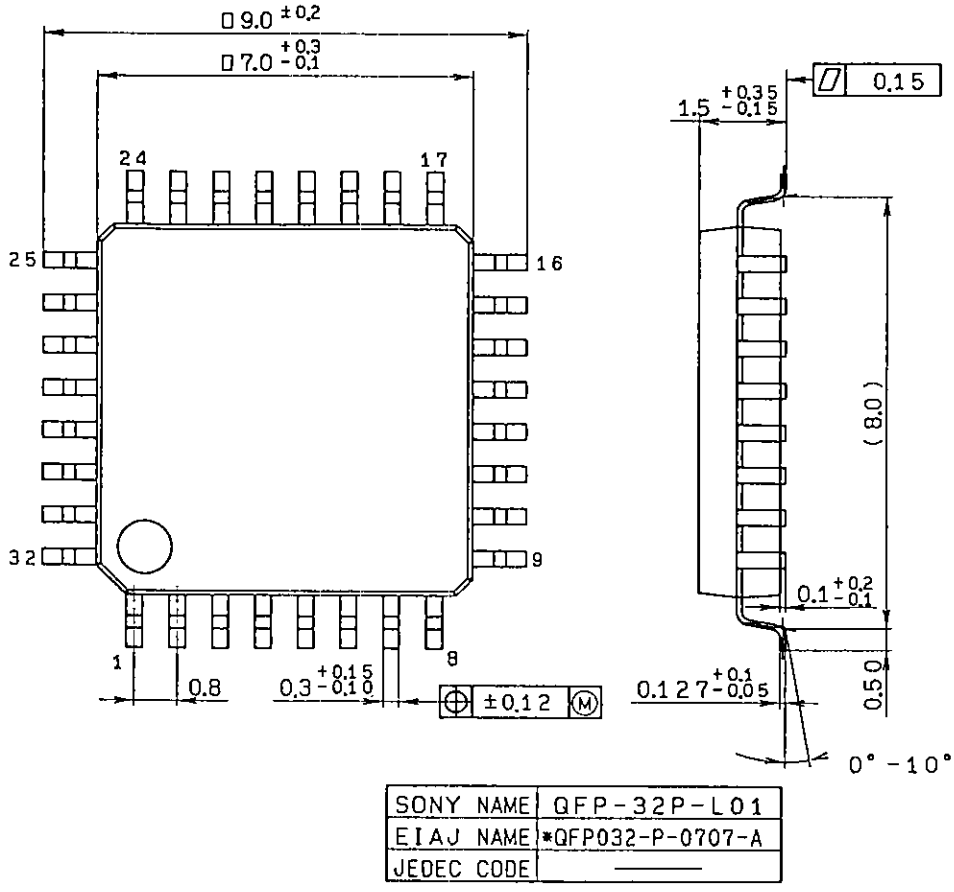


PAL (Filter configuration 1, Internal mode)



Package Outline Unit : mm

32pin QFP (Plastic) 0.2g



SONY NAME	QFP-32P-L01
EIAJ NAME	*QFP032-P-0707-A
JEDEC CODE	———