

# CLC5509

*CLC5509 Ultra Low Noise Preamplifier*



Literature Number: SNOS513C

# CLC5509

## Ultra Low Noise Preamplifier

### General Description

The CLC5509 is a high performance, ultra low noise preamplifier designed for applications requiring unconditional stability for wide ranges of complex input loads. Both input impedance and gain are externally adjustable, which make it simple to interface to piezoelectric ultrasound transducers. The CLC5509 preamplifier's low  $0.58\text{nV}/\sqrt{\text{Hz}}$  total input noise makes it ideal for noise sensitive front ends. The high repeatability in group delay over voltage and temperature translates into precision edge measurements for Doppler applications.

The IC consists of an emitter input, common base amplifier stage followed by a low distortion, closed loop buffer. The Noise Figure can be user programmed by controlling the emitter current ( $I_{\text{BIAS1}}$ ) which sets emitter resistance  $r_e$ . External negative feedback creates a well controlled input impedance to allow a near noiseless active input transmission line termination. The preamp is stable against changes in source impedance of 50 to  $200\Omega$  over temperature and supply variations, with gains from 14dB to 26dB. The CLC5509 preamp architecture is also well suited for use with magneto-resistive tape or disk drive heads. In these applications the head bias current can be reused to bias the preamp. The part is packaged in an 8-pin plastic SOIC, and runs off  $\pm 5\text{V}$  supplies. External biasing is required for the input signal path.

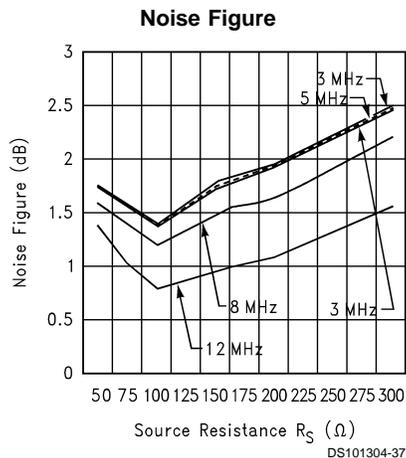
The CLC5509 is constructed using an advanced complementary bipolar process and National Semiconductor's proven high performance architectures.

### Features

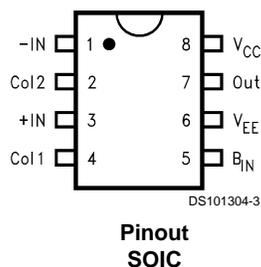
- $0.58\text{nV}/\sqrt{\text{Hz}}$  total input noise @ 12MHz
- $>3.0\text{dB}$  Noise figure advantage over shunt termination
- $<.5\text{ns}$  group delay repeatability
- High cutoff  $-3\text{dB}$  @ 33MHz
- Low cutoff  $-3\text{dB}$  @ 0.5MHz
- 2.0dB noise figure @  $50\Omega$
- $-60\text{dBc}$  intermod for  $2V_{\text{PP}}$  @ 5MHz
- Programmable noise figure vs.  $I_{\text{BIAS1}}$
- Supply current: 11mA
- Available in 8-pin SOIC

### Applications

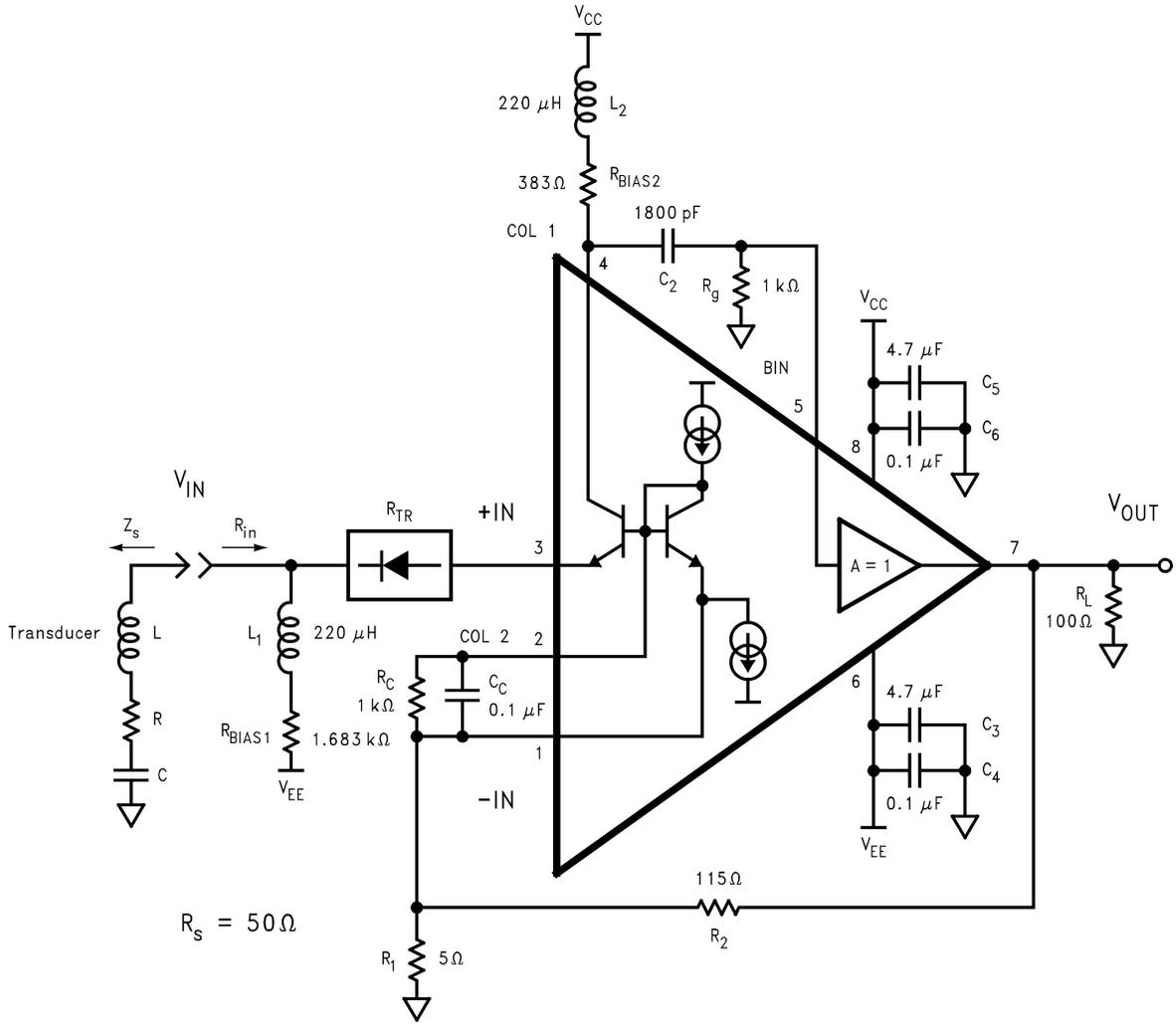
- Ultrasound preamp
- Tape drive preamp
- Disk drive preamp



### Connection Diagram



# Typical Application



DS101304-2

Ultrasound PreAmp

## Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	Transport Media	NSC Drawing
8-pin SOIC	0°C to 70°C	CLC5509CM	CLC5509CM	Rails	M08A
		CLC5509CMX	CLC5509CM	2.5k Tape and Reel	

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage  $\pm 5.5V$   
Output Current 70mA

Common-Mode Input Voltage  $\pm V_{CC}$   
Maximum Junction Temperature  $+150^{\circ}C$   
Storage Temperature Range  $-65^{\circ}C$  to  $+150^{\circ}C$   
Lead Temperature (soldering 10 sec)  $+300^{\circ}C$   
ESD Rating (human body model) 4000V

**Electrical Characteristics** (Note 3)

( $V_{CC}$ ,  $V_{EE}$  =  $\pm 5V$ ,  $R_S$  =  $50\Omega$ ,  $A_V$  =  $10V/V$ ,  $R_g$  =  $1k\Omega$ ,  $R_L$  =  $100\Omega$ ; unless specified)

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)	Units
	Ambient Temperature	CLC5509	$+25^{\circ}C$	$+25^{\circ}C$	
<b>Frequency Domain Response</b>					
	-3dB Bandwidth	$V_O < 2.0V_{PP}$			
	High Cutoff	-3dB	33	28 45	MHz
	Low Cutoff	-3dB	0.5	0.4 0.7	MHz
	Gain Flatness Inband	$2 < 12.5MHz$ , $V_O < 1.0V_{PP}$	-1.5 +1		dB
	Gain Accuracy @ 5MHz			$\pm 0.3$	dB
	Phase Variation	$3 < 9MHz$ , $V_O < .1V_{PP}$	1		Deg
	Gain Variation	$3 < 9MHz$ , $V_O < .1V_{PP}$	0.3		dB
<b>Time Domain Response</b>					
	Rise and Fall Time	2V step	10	10 15	ns
	Settling Time to 0.2%	2V step	1		$\mu s$
	Overshoot	2V step	0	5	%
	Group Delay	$2.5MHz < 10MHz$ , $V_{IN} = 10mV_{PP}$	5.5	3 7.5	ns
	Group Delay Repeatability		0.5		ns
<b>Distortion And Noise Response</b>					
	2nd Harmonic Distortion	$< 12.5MHz$ , $V_{IN} = 100mV_{PP}$	-51		dBc
	3rd Harmonic Distortion		-56		dBc
	Intermodulation Distortion	@ 5MHz	-65		dBc
	Equivalent Input Noise Voltage ( $e_{ni}$ )	$> 1MHz$ , $R_S = 50\Omega$ $12MHz$ , $R_S = 50\Omega$	0.7 0.58	0.78	$nV\sqrt{Hz}$
	Noise Figure	@ $50\Omega$	2	2.4	dB
	Optimum $R_S$		85	80 110	$\Omega$
<b>Static, DC Performance</b>					
	PSRR (preamp only)	$< 1MHz$	40		dB
	Supply Current (preamp only)	$R_L = \infty$	9	11	mA
<b>Miscellaneous Performance</b>					
	Output Impedance	DC $< 12MHz$	0.2	0.2 1	$\Omega$
	Output Voltage Range	$R_L = 100\Omega$	$\pm 2$	$\pm 1.7$	V
	Output Current		$\pm 45$	$\pm 35$	mA

## Electrical Characteristics (Note 3) (Continued)

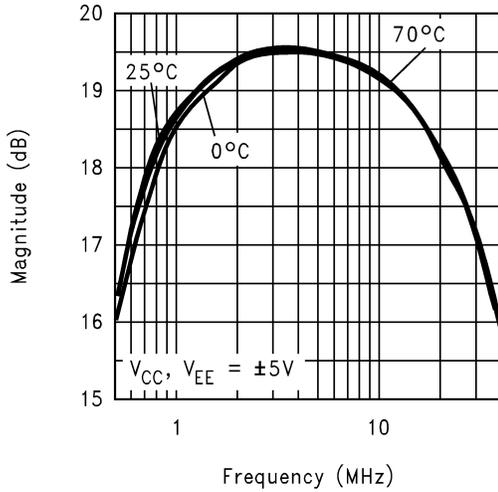
**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

**Note 3:** All data taken in circuit shown as typical application.

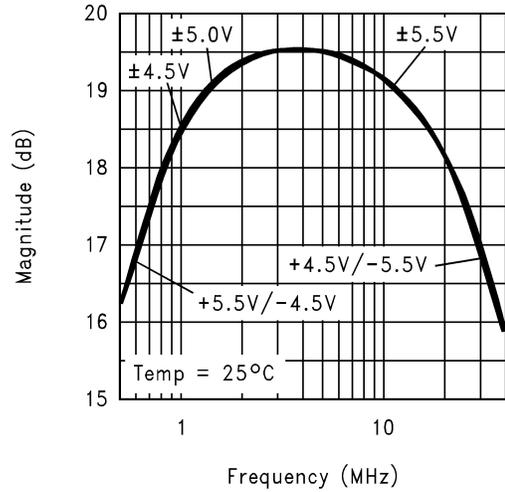
### Typical Performance Characteristics

Frequency Response



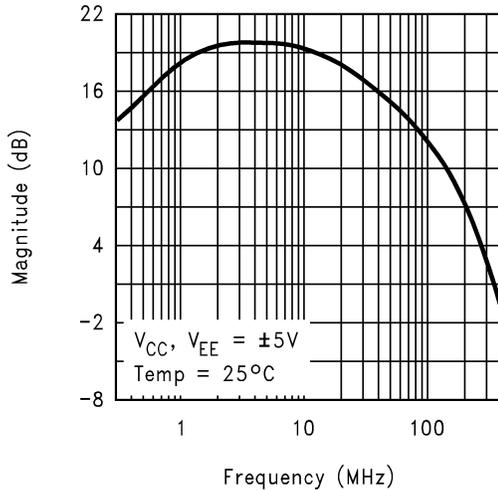
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Frequency Response



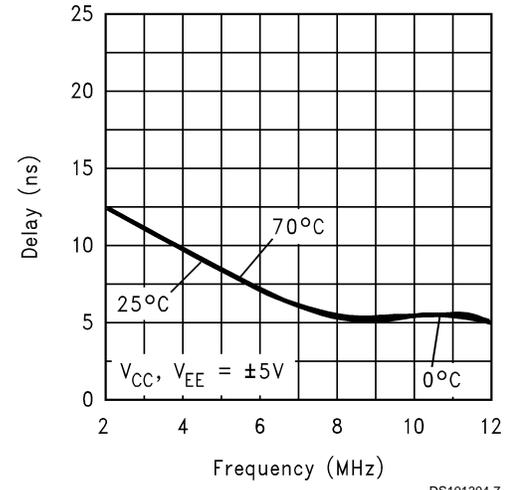
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Frequency Response



DS101304-6

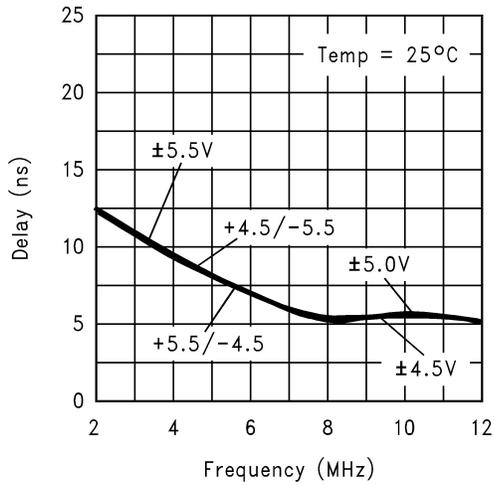
Group Delay



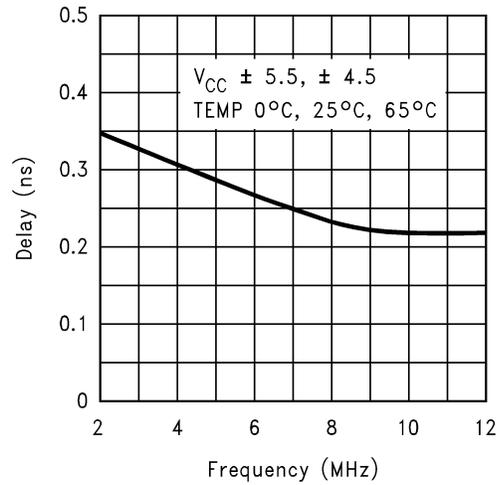
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## Typical Performance Characteristics (Continued)

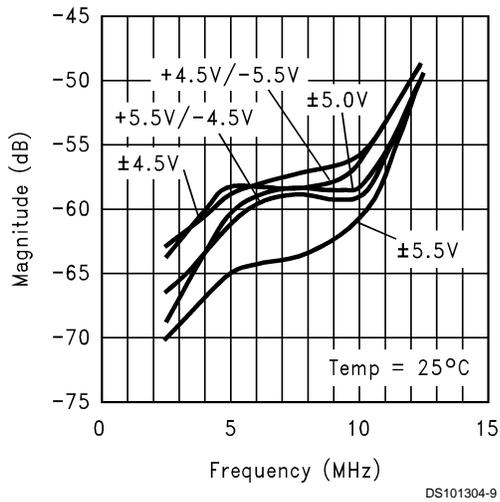
### Group Delay



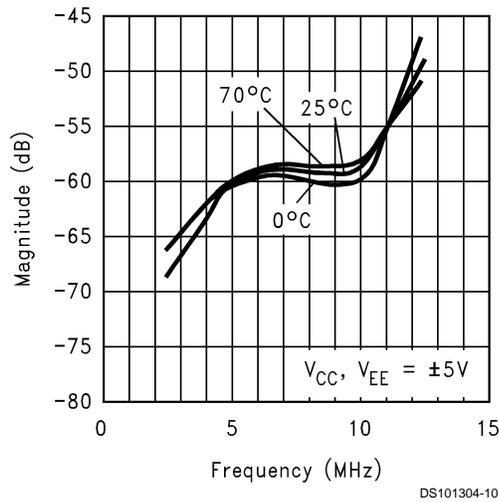
### Group Delay Repeatability



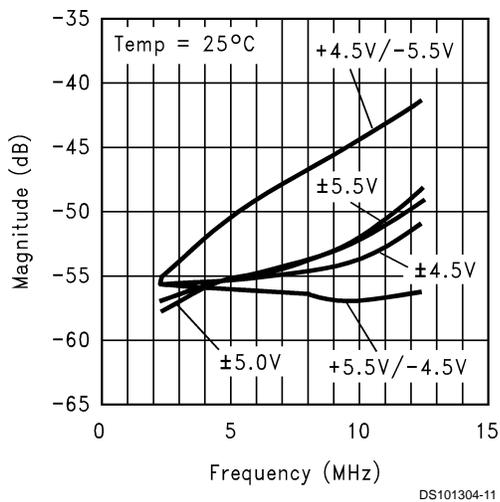
### 3rd Harmonic Distortion



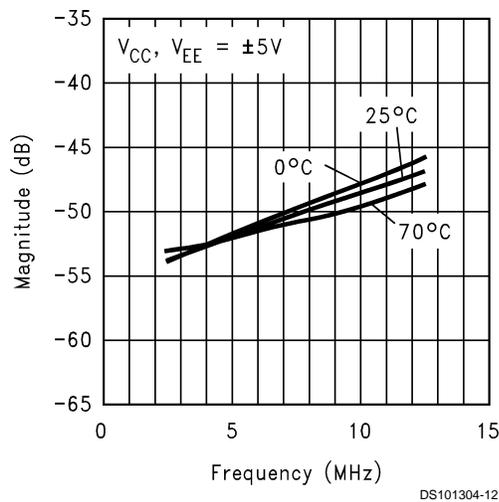
### 3rd Harmonic Distortion



### 2nd Harmonic Distortion

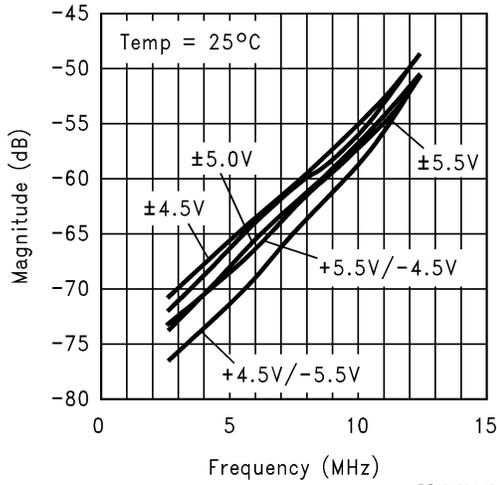


### 2nd Harmonic Distortion

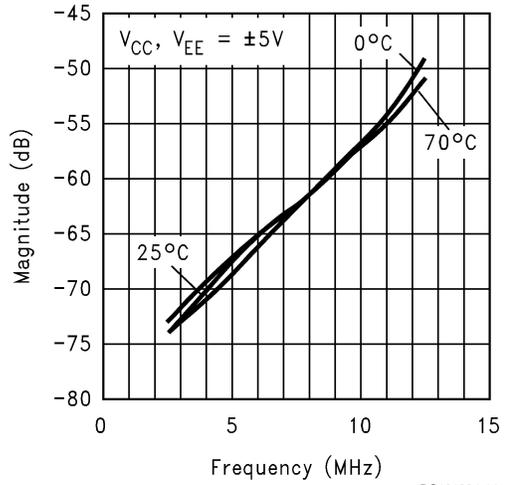


Typical Performance Characteristics (Continued)

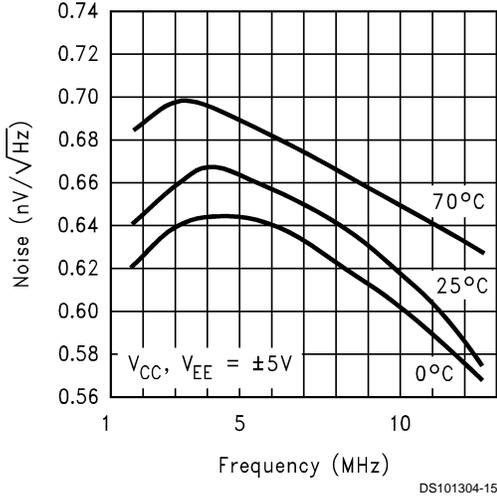
Intermodulation Distortion



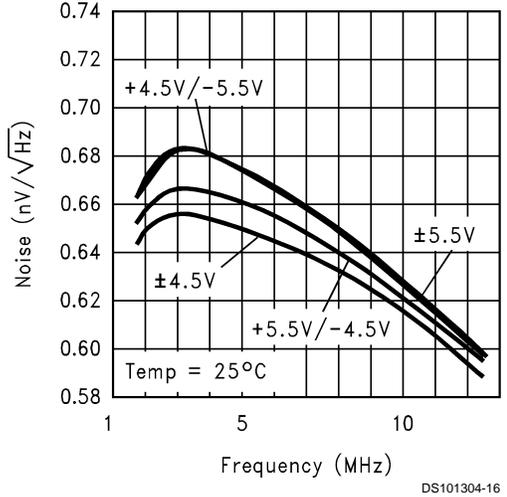
Intermodulation Distortion



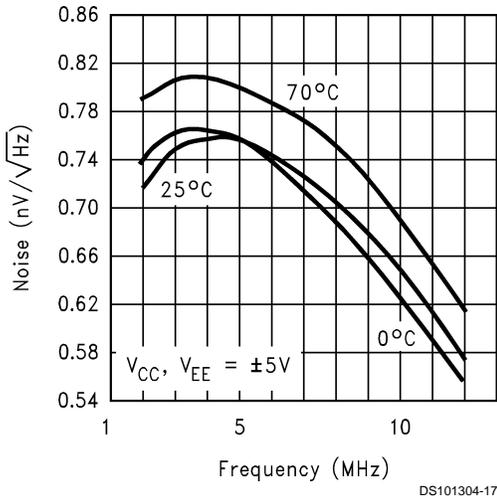
Total Input Referred Noise ( $R_S = 50\Omega$ )



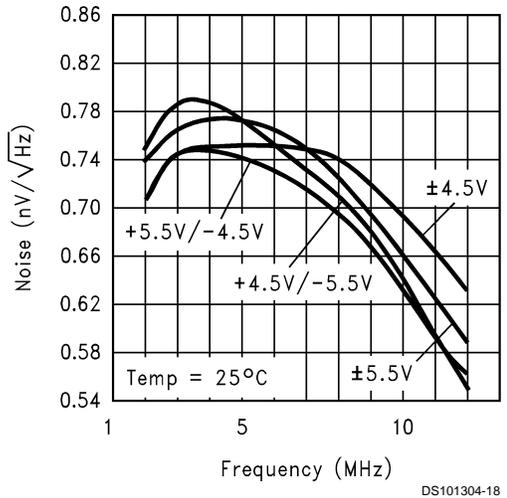
Total Input Referred Noise ( $R_S = 50\Omega$ )



Total Input Referred Noise ( $R_S = 100\Omega$ )

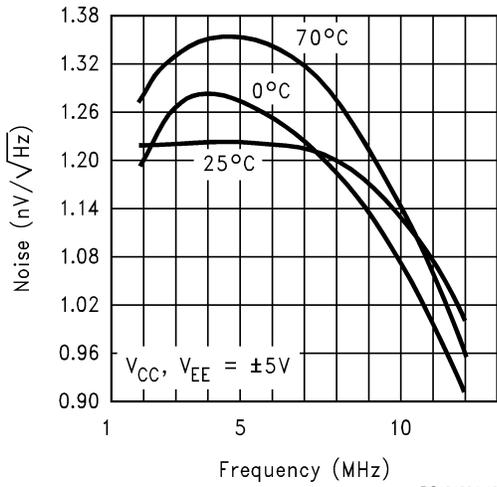


Total Input Referred Noise ( $R_S = 100\Omega$ )

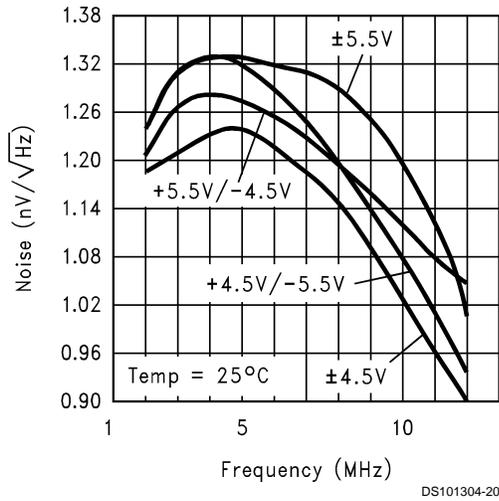


# Typical Performance Characteristics (Continued)

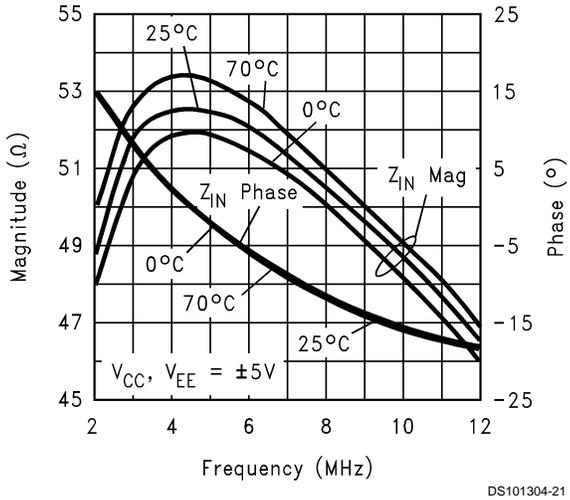
Total Input Referred Noise ( $R_S = 200\Omega$ )



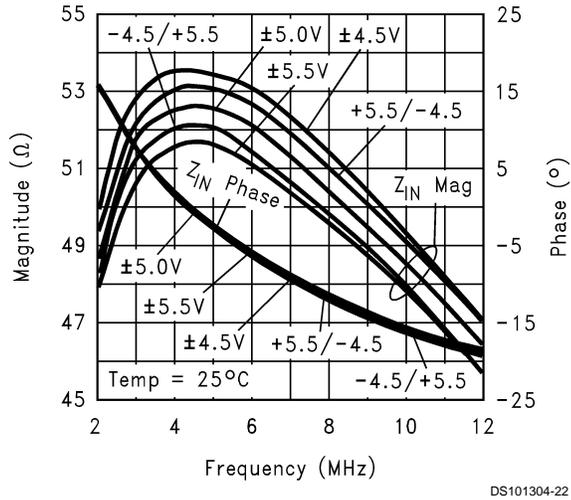
Total Input Referred Noise ( $R_S = 200\Omega$ )



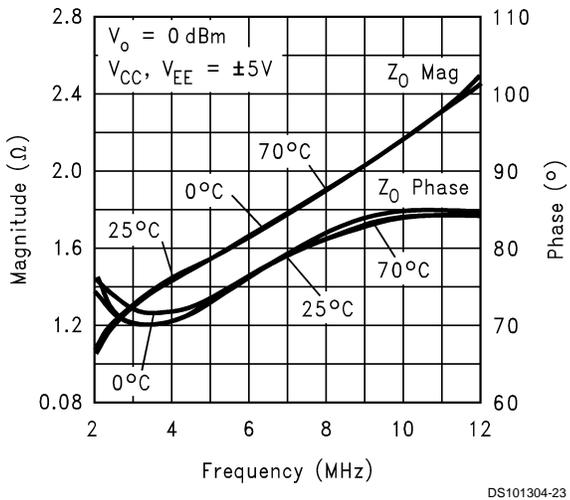
$Z_{in}$



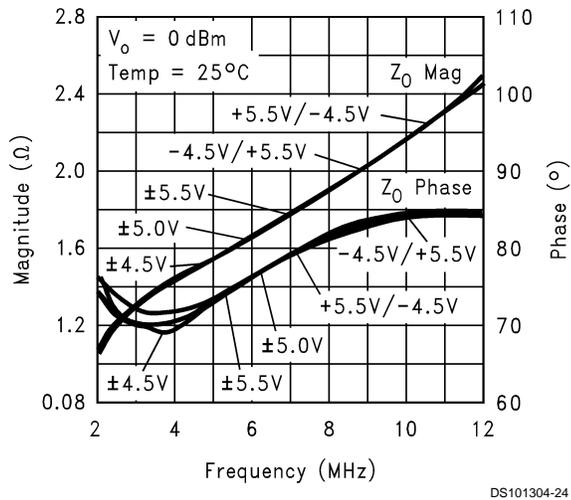
$Z_{in}$



$Z_o$

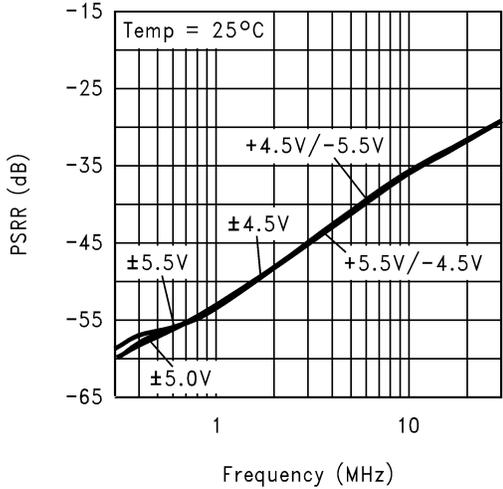


$Z_o$

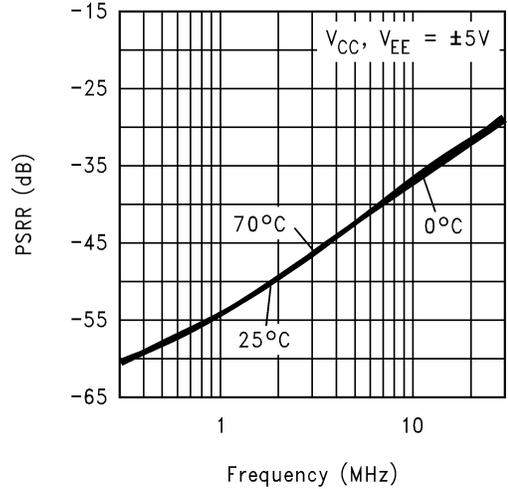


Typical Performance Characteristics (Continued)

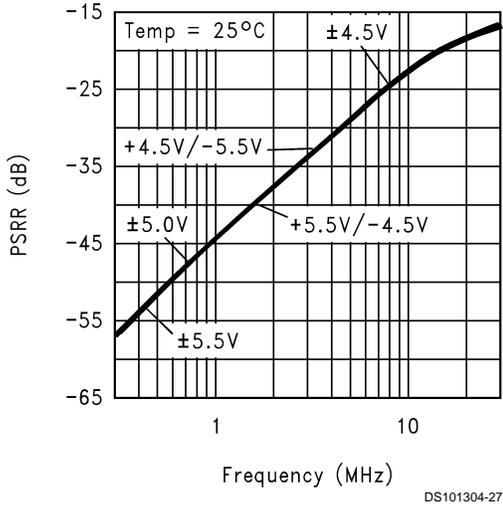
Positive PSRR ( $V_{CC}$ )



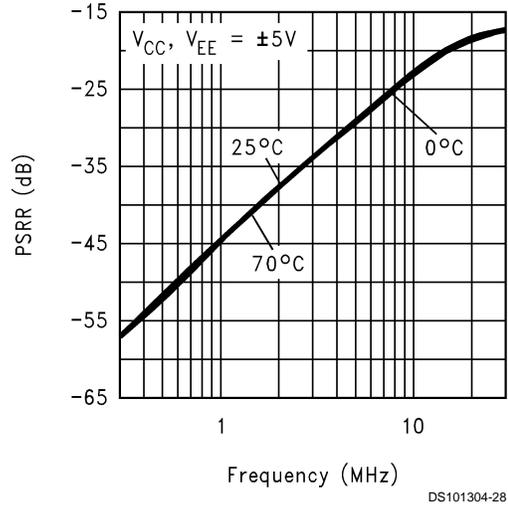
Positive PSRR ( $V_{CC}$ )



Negative PSRR ( $V_{EE}$ )



Negative PSRR ( $V_{EE}$ )



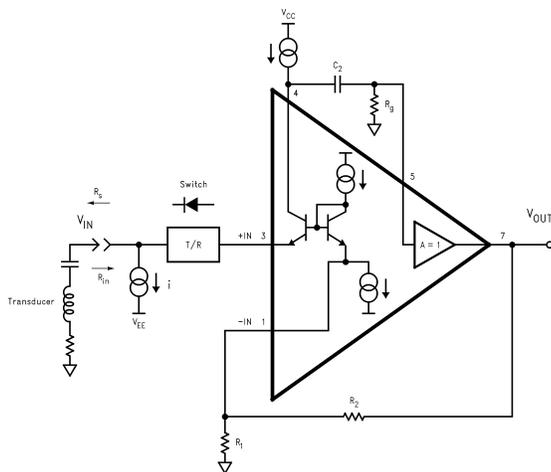
## Application Information

### Introduction

The CLC5509 is a two stage ultra-low noise preamplifier, with low distortion, and externally variable input impedance. The unusual emitter driven input stage remains stable for a wide range of transducer source loads. The input termination can be matched (for 50-200Ω source matching) to a wide range of complex loads ( $C_S$  up to 5000pF and  $C_P$  up to 10000pF,  $L_S$  up to 1μH). The IC was designed for low cost multiple channel ultrasound applications requiring flexible configurations for a variety of transmit/receive topologies. In a typical application, the CLC5509 is connected to a single element of an ultrasound transducer through a transmit/receive switch.

### Theory of Operation

The CLC5509 simplified circuit is shown in *Figure 1*. For analysis, the transmit/receive switch diode is modeled in the circuit as a series resistance  $R_{TR}$  with a voltage drop of  $V_{RT}$ . A piezo transducer generated, single-ended, positive voltage signal is applied to the emitter input of the 1st stage. The voltage signal is converted to a current ( $i$ ) that is passed through a high pass filter then restored back to a voltage signal at  $R_g$ . A high speed, low distortion, unity gain buffer, applies the signal to the load and feedback resistor. Negative feedback from the buffer output to the inverting input completes the signal path.



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**FIGURE 1. Simplified Circuit**

The input and output voltage can be expressed as shown:

$$V_{IN} = (R_{TR} + r_e) i + V_O (R_1 / (R_1 + R_2))$$

$$V_O = -(i \times R_g) \quad \text{for } \alpha = 1$$

The input resistance is calculated

$$R_{IN} = \frac{V_{IN}}{I_i} = R_{TR} + r_e + R_g (R_1 / (R_1 + R_2))$$

The current  $I_{BIAS1}$  is the input stage emitter current that sets  $r_e$ .

$$I_{BIAS1} = (V_{EE} - V_{TR}) / R_{BIAS1} \quad \text{for } V_{EE} = V_{TR} = .65V$$

$$r_e = 26mV / I_{BIAS1}$$

Combining terms, then solving for close loop gain  $V_O / V_{in}$  results in

$$A_{CL} \approx \frac{R_g}{R_{IN}}$$

### Choosing External Component Values

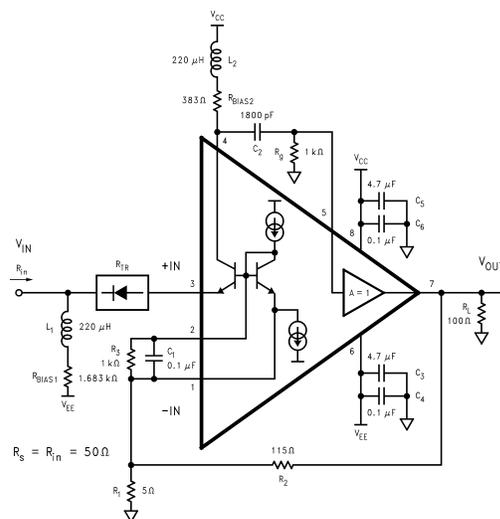
There are three key parameters to consider in the design: Noise, signal bandwidth, and gain. Refer to *Figure 2*.

The best noise performance for a given transmit/receive switch  $R_{TR}$  is obtained by: choosing  $R_S$  between 50Ω and 200Ω; selecting the matching termination resistance  $R_{in}$ ; and by reducing  $I_{BIAS1}$  (by increasing  $R_{BIAS1}$ ) to increase  $r_e$  which optimizes the Noise Figure (NF). For this circuit, with  $R_{TR} = 6\Omega$ , the optimum NF is achieved at  $R_S \sim 95\Omega$  when  $R_{in}$  is set to 50Ω and  $R_S \sim 145\Omega$  when  $R_{in}$  is set to 200Ω.

The signal bandwidth is determined by the selection of  $L_1$ ,  $L_2$ ,  $R_{BIAS1}$  and  $R_{BIAS2}$  which set the open loop gain roll-off of the first stage.  $R_g$  and  $C_2$  form a desirable signal path filter that introduces an additional highpass pole. The filter values can be chosen to create a sharper high frequency roll off of the closed loop gain. For  $R_g = 1k$ ,  $C_2 \sim 470pF$  the small signal ( $V_{in} < 25mV$ ), wide bandwidth performance can be observed. By increasing  $C_2$  (to  $> 1500pF$ ) and increasing output series resistance with a small resistor, the stability and harmonic distortion performance can be improved for large signals. This filter can also be designed as a multi-pole Butterworth filter but care must be taken to ensure stability with the desired load over the operating temperature range.

The passband gain is customer selected by setting  $R_g$  and  $R_{in}$ . Note that using  $R_1$  to reduce or increase the gain allows for minimal interaction with other parameters.

Capacitor  $C_C$  and resistor  $R_C$  are used for local compensation of the gm input stage with values of  $C_C = 0.1\mu F$  and  $R_C = 1k$  for the applications described below.



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**FIGURE 2. Complete Circuit**

### Calculating and Measuring the Noise

The circuit input referred noise is best calculated using a SPICE model where the external components can be optimized for the transducer source impedance and transmit/receive switch impedance. The SPICE model for the CLC5509 is available on the NSC web site. Refer to the figures for total noise performance over temperature and

## Application Information (Continued)

supply at 3mA. Once the noise is modeled and circuit parameters chosen the evaluation board can be used to measure actual noise performance.

To measure the CLC5509 input referred noise vs. other noise sources, several key steps should be followed. The bench setup is fairly simple using the evaluation board and a spectrum analyzer. (If a noise figure meter is available that is even easier yet.) The procedure requires calibrating out the spectrum analyzer background noise, and other noise sources from the CLC5509 noise. Since the thermal noise of a resistor is well known, add a series resistor  $R_4$  between the signal source  $V_{in}$  and the  $L_1$ ,  $R_{BIAS1}$  bias network for these noise measurements. Several  $R_4$  resistor values are used as "reference" noise sources. The values chosen depend on the  $R_{in}$  of the system. For  $R_{in} = 50\Omega$ , resistor ( $R_4$ ) with values of 0, 12.5, 25, 50 $\Omega$  should be used. If  $R_{in} = 200\Omega$ , resistors ( $R_4$ ) with values of 0, 25, 50, 100, 200 $\Omega$  should be used. Start by connecting the analyzer input to the evaluation board output. Remove  $R_4$  from the signal source and connect  $R_4$  to GND. Now take at least 10 measurements and average them for each  $R_4$  reference value. Be sure to divide the result by the analyzer and circuit gain to make the noise power input referred. Subtract the  $R_4 = 0\Omega$  results from the data for each value using an RMS difference. Compare the result to the theoretical noise values. They should agree closely over the  $R_4 = 0$  to  $R_{in}$  range. This verifies the test method. The CLC5509 noise is the  $R_4 = 0\Omega$  data point.

The optimum  $R_S$  value for best noise figure can be adjusted from  $R_S \sim 80$  to  $R_S \sim 120\Omega$  by changing  $I_{BIAS1}$  from 12mA to 3mA. The  $I_{BIAS1}$  current could be made programmable to optimize the NF for different transducer source impedances. A similar procedure can be used to remove the T/R switch noise by varying the T/R bias current  $I_{BIAS1}$ . The total circuit noise performance can now be optimized for  $R_{in}$  as described above.

### Evaluation Board

Evaluation boards are available for customer product evaluation for the 8-pin SOIC. Evaluation kits that contain an

The CLC5509 system dynamic range performance is enhanced by using the CLC5523 variable gain amplifier as a post amplifier. See *Figure 4* below.

The signal gain range is divided between the CLC5509 preamplifier and the post amplifier to allow wider dynamic range and better performance for high crest factor signals. There are two common ways the CLC5523 variable gain could be controlled. The first, *Figure 5*, uses a DAC to digitally increase the gain in discrete steps. The second *Figure 6* uses an AGC loop to maintain the maximum system input signal-to-noise. Refer to the CLC5523 data sheet applications for the implementation details.

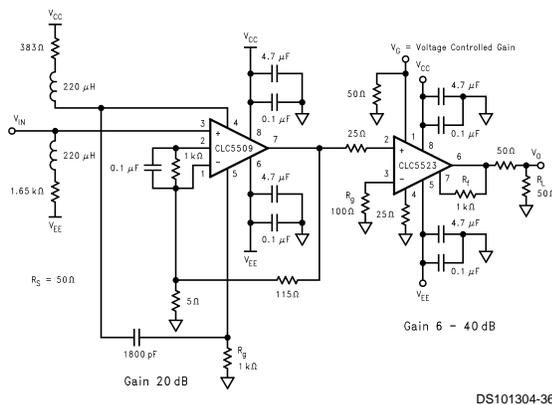


FIGURE 4. Low Noise Pre Amp with Variable Gain Amplifier Circuit

evaluation board and CLC5509 samples can be obtained by calling **National Semiconductor's Customer Service Center**. The evaluation kit number is CLC730101. The evaluation board utilizes surface mount components. The corner frequencies are set to  $\sim 0.9\text{MHz}$  to  $12.5\text{MHz}$  with a passband gain set at 20dB. The highpass filter is set at  $R_g = 1\text{k}$ ,  $C_2 = 470\text{pF}$  to view small signal ( $V_{in} < 25\text{mV}$ ) performance. Increasing  $C_4$  (to  $> 1500\text{pF}$ ) reduces the bandwidth and improves distortion for large signals.  $R_g$  is a back match resistor that terminates the output and isolates cable capacitance, for minimum distortion, over the frequency band of interest. An  $R_{in} \sim 50.2\Omega$  was chosen for  $R_s = 50\Omega$  (this source resistor  $R_s$  is open) and  $R_{TR} = 0$ , with  $I_{BIAS1}$  set to 3mA. The expected input referred noise based on bench measurements on similar boards is  $\sim 0.6\text{nV}/\sqrt{\text{Hz}}$  or a NF of 2dB. The noise can be optimized with slight variations in  $R_2$ ,  $R_g$  and  $R_{BIAS1}$ . If transmit/receive switches are added to the evaluation board both the voltage drop and  $R_{TR}$  should be compensated for. The  $R_{in}$ , gain and noise will be affected by the addition of the T/R switch. The  $V_{TR}$  drop can be removed, to a first order, by adding a second switch in series with the feedback gain setting resistor  $R_1$  to ground. This will restore the input DC level to  $\sim 0\text{V}$ . This T/R switch diode should be biased with a resistor ( $\sim R_{BIAS2}$ ) to  $V_{CC}$  and bypassed with a  $0.1\mu\text{F}$  cap to maintain the same AC performance as the evaluation board without the switches.

### CLC5509 Applications

The signal path for a typical ultrasound transceiver is shown in *Figure 3*.

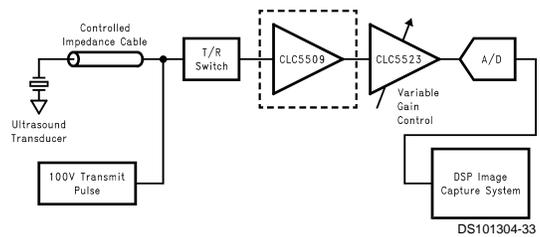
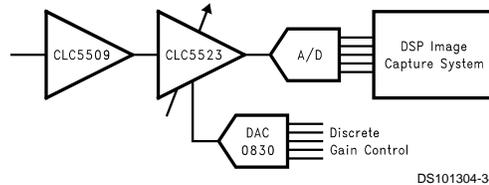
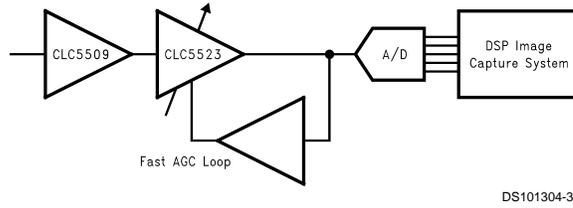


FIGURE 3.

## Application Information (Continued)

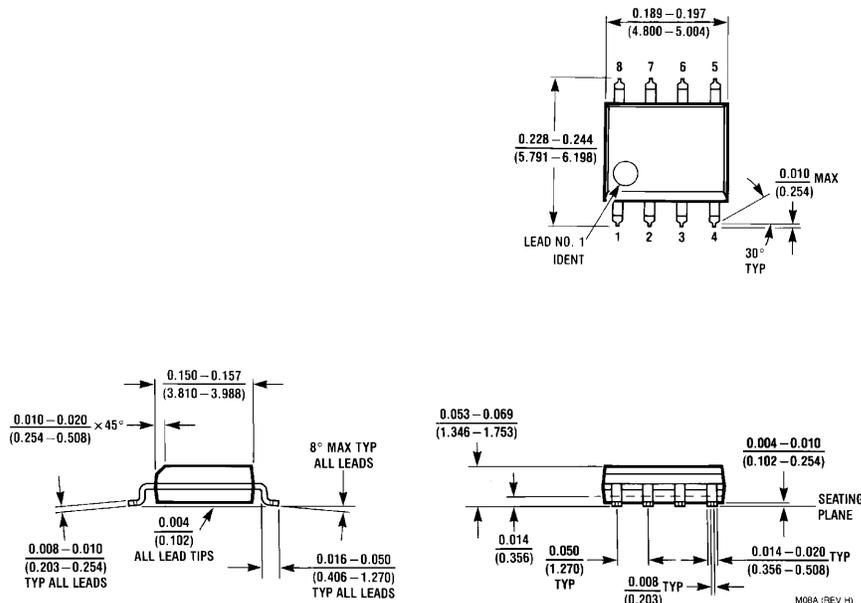


**FIGURE 5.  $V_G$  Controlled by DAC in Discrete Steps**



**FIGURE 6.  $V_G$  Controlled by AGC Loop**

**Physical Dimensions** inches (millimeters) unless otherwise noted



**8-pin SOIC  
NS Package Number M08A**

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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