CLC431,CLC432

CLC431/432 Dual Wideband Monolithic Op Amp with Disable

Literature Number: SNOS824C

National Semiconductor

February 2001

CLC431/432
Dual Wideband Monolithic Op Amp with Disable

General Description

The CLC431 and CLC432 current-feedback amplifiers provide wide bandwidths and high slew rates for applications where board density and power are key considerations. These amplifiers provide DC-coupled small signal bandwidths exceeding 92MHz while consuming only 7mA per channel. Operating from ±15V supplies, the CLC431/432's enhanced slew rate circuitry delivers large-signal bandwidths without out voltage swings up to $28V_{pp}$. A wide range of bandwidth insensitive gains are made possible by virtue of the CLC431 and CLC432's current-feedback topology.

The large common-mode input range and fast settling time (70ns to 0.05%) make these amplifiers well suited for CCD & data telecommunication applications. The disable of the CLC431 can accommodate ECL or TTL logic levels or a wide range of user definable inputs. With its fast enable/disable time (0.2µs/1µs) and high channel isolation of 70dB at 10MHz, the CLC431 can easily be configured as a 2:1 MUX. Many high performance video applications requiring signal gain and/or switching will be satisfied with the CLC431/432 due to their very low differential gain and phase errors (less than 0.1% and 0.1°; A_V = +2V/V at 4.43MHz into 150Ω load).

Quick 8ns rise and fall times on 10V pulses allow the CLC431/432 to drive either twisted pair or coaxial transmission lines over long distances.

The CLC431/432's combination of low input voltage noise, wide common-mode input voltage range and large output voltage swings make them especially well suited for wide dynamic range signal processing applications

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-94725

*Space level versions also available.

*For more information, visit http://www.national.com/mil

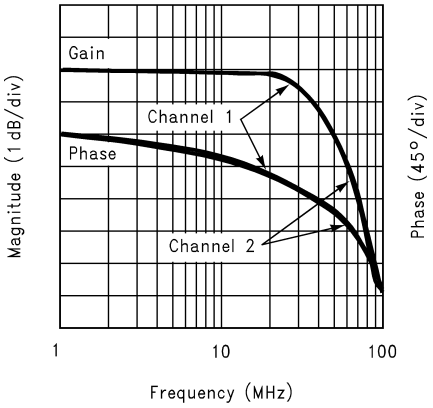
Features

- Wide bandwidth: 92MHz(A_V =+1), 62MHz(A_V=+2)
- Fast slew rate: 2000V/µs
- Fast disable: 1µs to high-Z output
- High channel isolation: 70dB at 10MHz
- Single or dual supplies: ±5V to ± 16.5V

Applications

- Video signal multiplexing
- Twisted-pair differential driver
- CCD buffer & level shifting
- Discrete gain-select amplifier
- Transimpedance amplifier

CLC431/CLC432 Channel Matching



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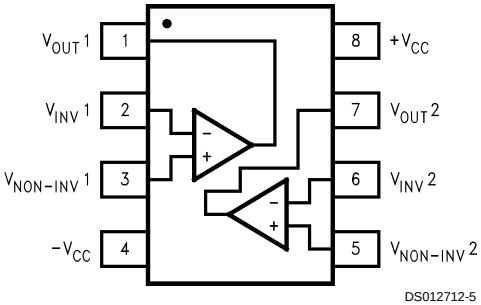
Connection Diagrams



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Pinout
CLC432 DIP & SOIC

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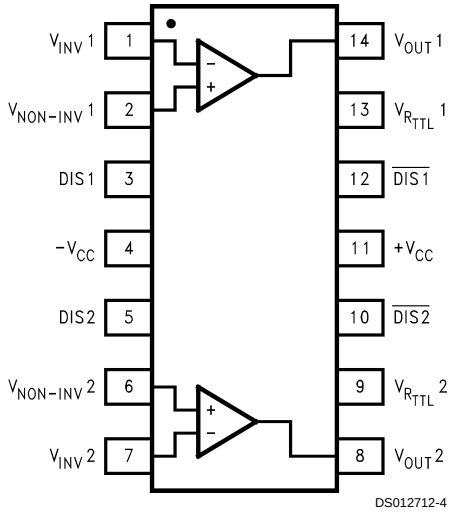
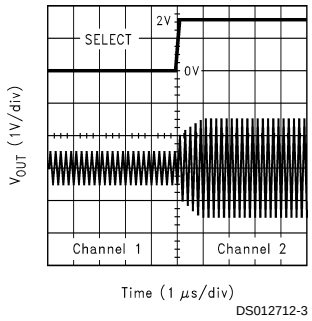
Connection Diagrams (Continued)

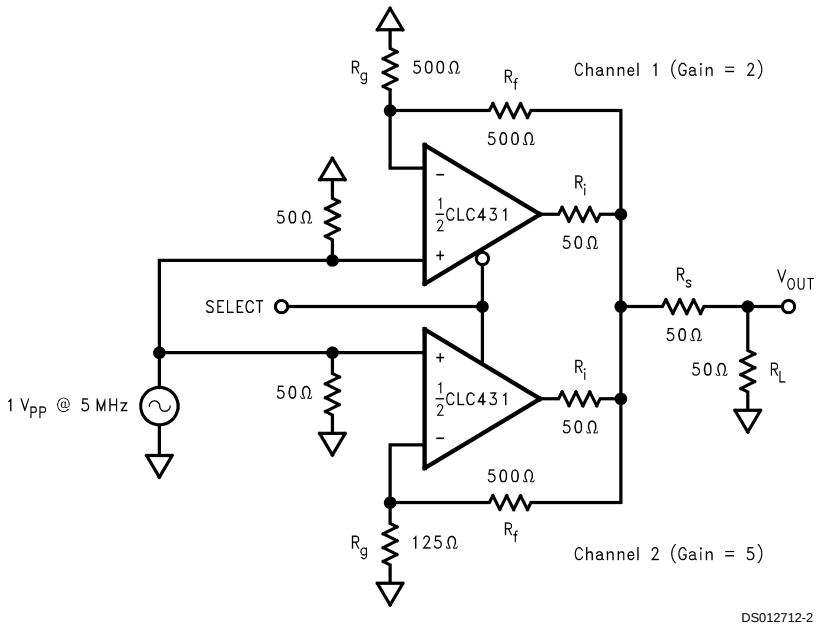


Pinout
CLC431 DIP & SOIC

Typical Application



CLC431 Gain-Select Amplifier



Discrete Gain-Select Amplifier

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
14-Pin Plastic DIP	−40˚C to +85˚C	CLC431AJP	CLC431AJP	N14A
14-Pin Plastic SOIC	−40˚C to +85˚C	CLC431AJE	CLC431AJE	M14A,B
8-Pin Plastic DIP	−40˚C to +85˚C	CLC432AJP	CLC432AJP	N08E
8-Pin Plastic SOIC	−40˚C to +85˚C	CLC432AJE	CLC432AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±16.5V
Short Circuit Current	100mA
Common-Mode Input Voltage	$\pm V_{CC}$
Differential Input voltage	±10V
Maximum Junction Temperature	150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering 10 sec)	+300˚C

Operating Ratings

Thermal Resistance Package	(θ_{JC})	(θ_{JA})
14-Pin MDIP	55˚C/W	100˚C/W
14-Pin SOIC	35˚C/W	105˚C/W
8-Pin MDIP	55˚C/W	110˚C/W
8-Pin SOIC	40˚C/W	115˚C/W

Electrical Characteristics

V_{CC} = ±15V; A_V = +2; R_f = R_g = 750Ω; R_L = 100Ω; unless noted

(Note 3)	Parameters	Conditions	Typ	Max/Min Ratings (Note 2)			Units
	Ambient Temperature	**CLC431 & CLC432**	**+25**	**+25**	**0 to +70**	**−40 to +85**	**˚C**
Frequency Domain Response							
	-3dB Bandwidth	V_{OUT} < $4.0V_{PP}$	62	42	37	36	MHz
		V_{OUT} < $4.0V_{PP}$, V_{CC} = ±5V	62				MHz
(Note 4)		V_{OUT} < $10V_{PP}$	28	21	20	20	MHz
	Gain Flatness	V_{OUT} < $4.0V_{PP}$					
	Peaking	DC to 100MHz	0.05	0.5	0.7	0.7	dB
	Rolloff	DC to 20MHz	0.0	0.8	0.8	0.8	dB
	Linear Phase Deviation	DC to 30MHz	0.3	1.8	2.0	2.1	deg
	Differential Gain	R_L = 150Ω,4.43MHz	0.12	0.18	0.2	0.2	%
	Differential Phase	R_L = 150Ω, 4.43MHz	0.12	0.18	0.23	0.25	deg
Time Domain Response							
(Note 4)	Rise and Fall Time	10V Step	8	12	13	13	ns
	Overshoot	2V Step	5	10	12	12	%
	Settling Time	2V Step to 0.05%	70	100	110	110	ns
(Note 4)	Slew Rate	V_{OUT} = ±10V	2000	1500	1450	1400	V/ms
Distortion And Noise Response							
(Note 8)	2nd Harmonic Distortion	$2V_{PP}$, 1MHz	−65				dBc
(Note 8)	3rd Harmonic Distortion	$2V_{PP}$, 1MHz	−75				dBc
	Equivalent Input Noise						
	Voltage	>1MHz	3.3	4.2	4.4	4.5	$nV/\sqrt{Hz}$
	Current, Inverting	>1MHz	13	16	17	18	$pA/\sqrt{Hz}$
	Current, Non-Inverting	>1MHz	2.0	2.5	2.6	2.8	$pA/\sqrt{Hz}$
Static, DC Performance							
(Note 9)	Input Offset Voltage		3	6	7	7	mV
	Average Drift		20	-	50	50	µV/˚C
(Note 9)	Input Bias Current, Non-Inverting		2	8	10	16	µA
	Average Drift		25	-	100	150	nA/˚C
(Note 9)	Input Bias Current, Inverting		2	6	6	8	µA
	Average Drift		8	-	25	40	nA/˚C
	Power Supply Rejection Ratio	DC	64	59	59	59	dB
	Common-Mode Rejection Ratio	DC	63	58	57	56	dB
(Note 9)	Supply Current	R_L = ∞, Per Channel	7.1	7.9	8.5	9.6	mA

Electrical Characteristics (Continued)

V_{CC} = ±15V; A_V = +2; R_f = R_g = 750Ω; R_L = 100Ω; unless noted

(Note 3)	Parameters	Conditions	Typ	Max/Min Ratings (Note 2)			Units
	Ambient Temperature	**CLC431 & CLC432**	**+25**	**+25**	**0 to +70**	**−40 to +85**	**˚C**
Static, DC Performance							
(Note 9)	CLC431 Disabled	R_L = ∞, Per Channel	0.8	1.2	1.3	1.45	mA
Miscellaneous Performance							
	Input Voltage Range	Common Mode	± 12.2	± 12.0	± 11.8	± 11.6	V
	Input Resistance	Non-Inverting	24	16	10	6	MΩ
	Input Capacitance	Non-Inverting	0.5	1	1	1	pF
	Output Current		±60	±38	±35	±30	mA
	Output Voltage Range	R_L ≥ 5kΩ	± 14.0	± 13.6	± 13.4	± 13.2	V
		R_L = 100Ω	± 6.0	± 3.7	± 3.7	± 2.9	V
Switching Performance (CLC431)							
	Switching Time	Turn On	0.1	0.15	0.155	0.165	µs
		Turn Off	0.7	1.0	1.2	1.2	µs
(Note 5)	DIS Logic Levels	Single-Ended Mode					
	High Input Voltage (V_{IH})		>2.0	>2.0	>2.0	>2.0	V
	Low Input Voltage (V_{IL})		<0.8	<0.8	<0.8	<0.8	V
	Maximum Current Input	V_{IH} > DIS > V_{IL}	150	180	190	205	µA
(Note 6)	DIS-$\overline{\text{DIS}}$	Differential Mode					
	Minimum Differential Voltage		0.3	0.4	0.4	0.4	V
Isolation							
	Crosstalk, Input Referred	10MHz	70	64	64	64	dB
(Note 7)	Off Isolation	10MHz	64	60	60	60	dB

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: Tested and guaranteed with R_f = 866Ω. CLC432 tested and guaranteed with R_f = 750Ω

Note 4: Spec is guaranteed for R_L ≥ 500Ω

Note 5: V_{RTTL} = 0, See text for single-ended mode of operation.

Note 6: V_{RTTL} = NC, See text for differential mode operation.

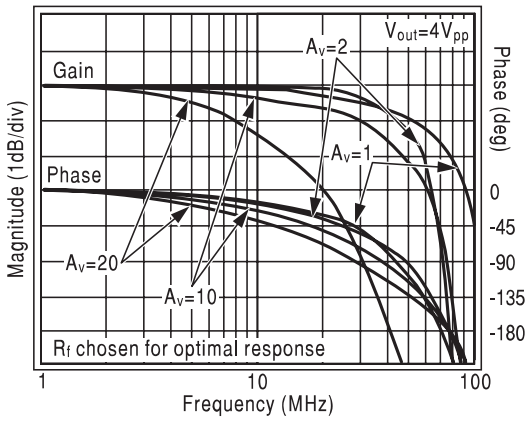
Note 7: Spec is guaranteed for AJE & AJP yield 7dB lower

Note 8: Spec is tested with $2V_{PP}$, 10MHz and R_L = 100Ω

Note 9: J-level: spec is 100% tested at +25˚C

Typical Performance Characteristics (T_A = +25˚C, A_V = +2, V_{CC} = ±15V, unless specified)

Non-Inverting Frequency Response



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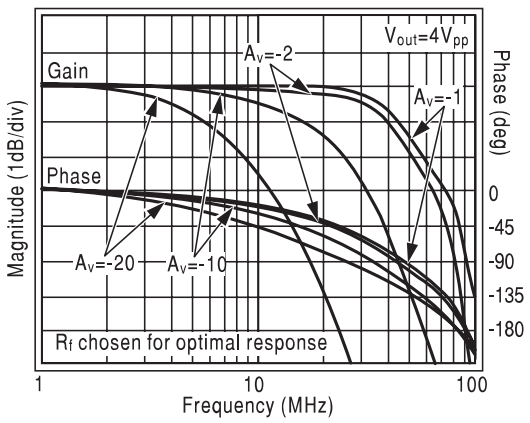
Inverting Frequency Response



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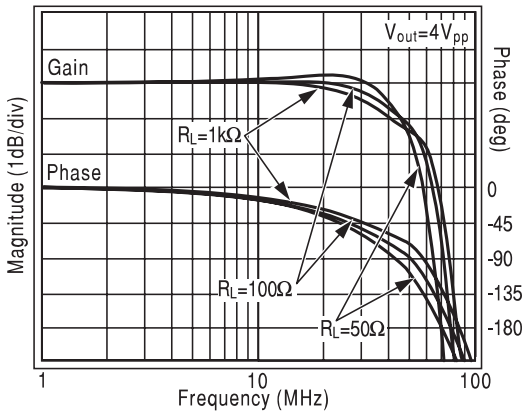
Typical Performance Characteristics (T_A = +25°C, A_V = +2, V_{CC} = ±15V, unless specified) (Continued)

Frequency Response vs. Load Resistance



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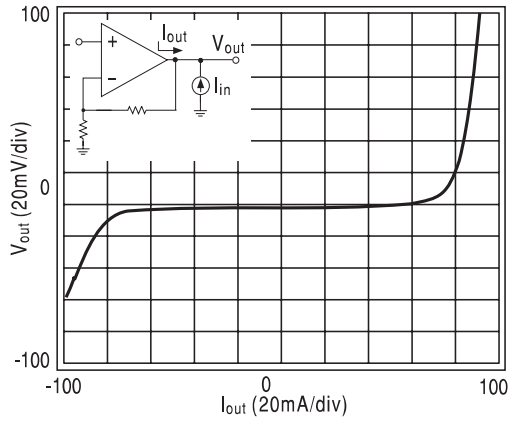
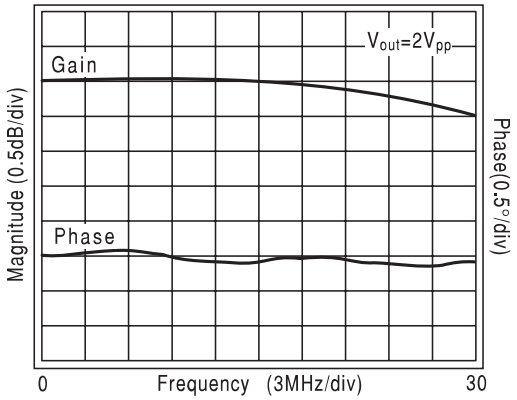
Output Current



DS012712-9

Gain Flatness & Linear Phase Deviation



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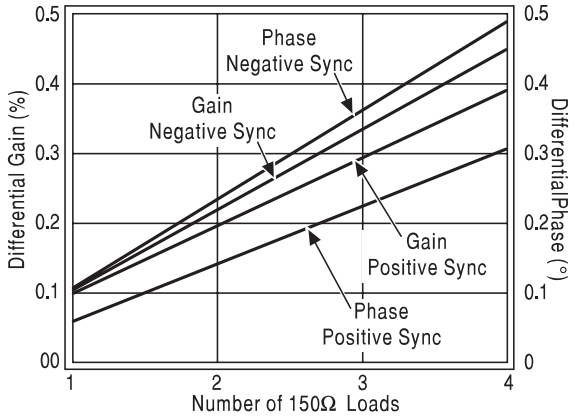
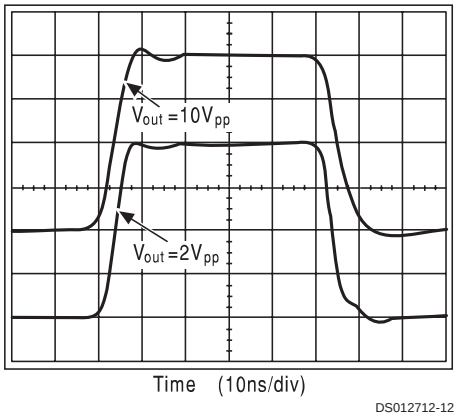
Differential Gain and Phase at 3.58MHz



DS012712-11

Pulse Response



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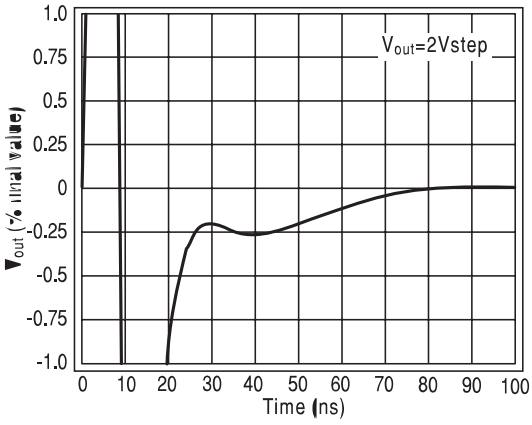
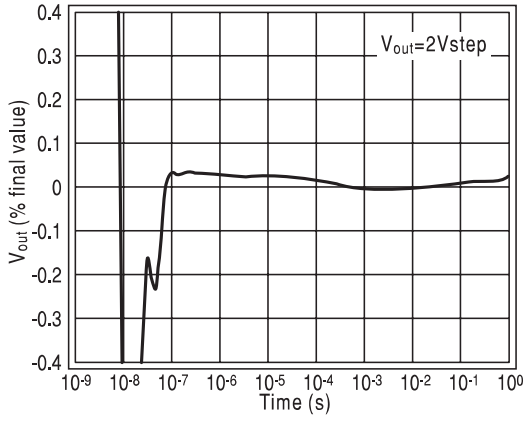
Short-Term Settling Time



DS012712-13

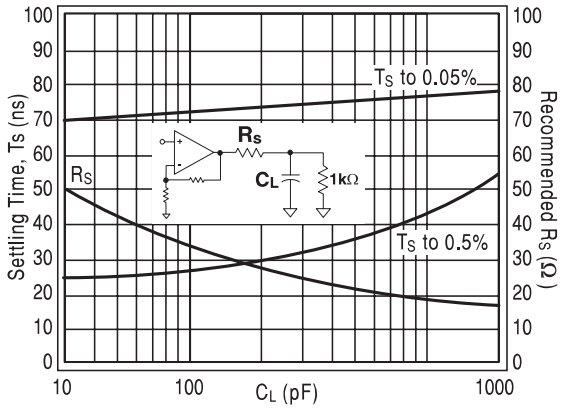
Typical Performance Characteristics (T_A = +25°C, A_V = +2, V_{CC} = ±15V, unless specified) (Continued)

Long-Term Settling Time



DS012712-14

Settling Time vs. Capacitive Load



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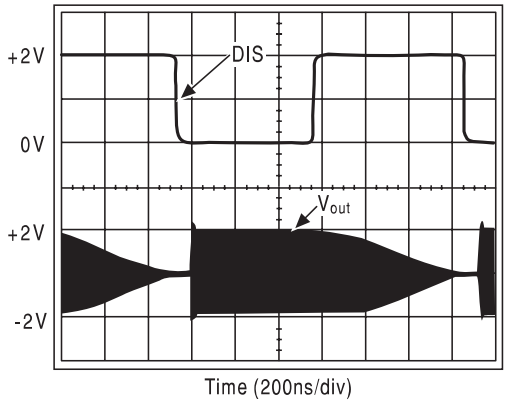
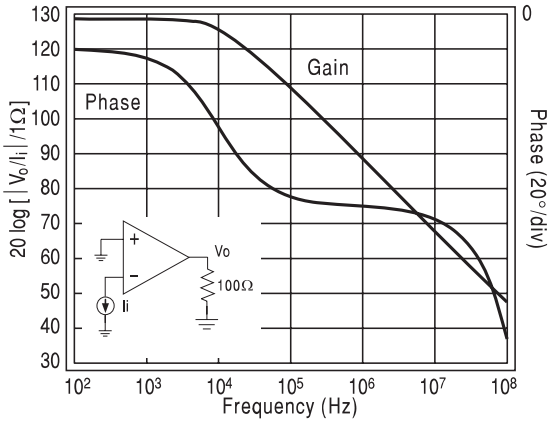
Turn-Off/ On Time (CLC431)



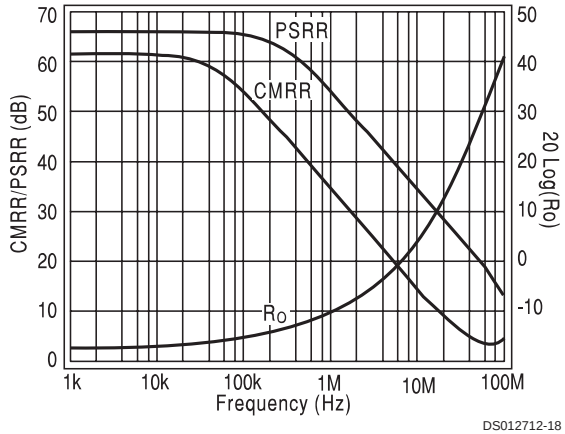
DS012712-16

Open-Loop Transimpedance



DS012712-17

CMRR, PSRR and Closed-Loop R_O



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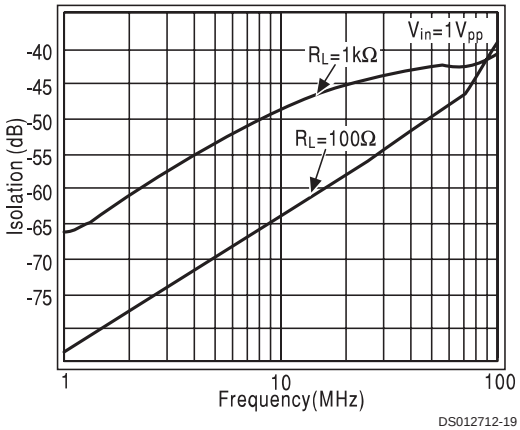
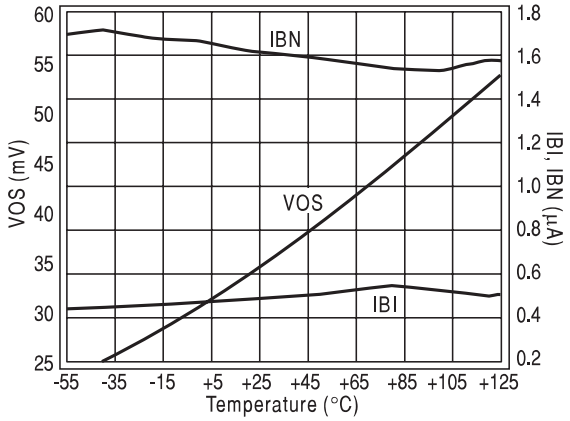
Off-Isolation during Disable (CLC431)



DS012712-19

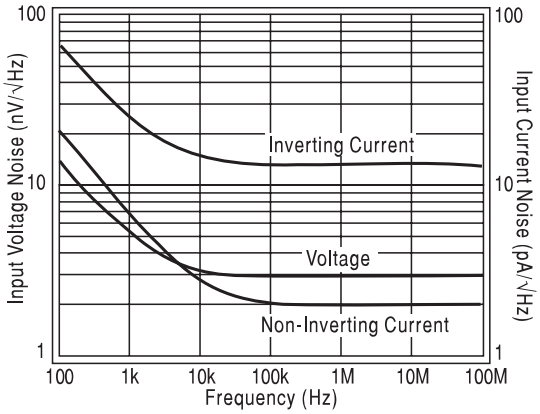
Typical Performance Characteristics (T_A = +25˚C, A_V = +2, V_{CC} = ±15V, unless specified) (Continued)

Typical DC Errors vs. Temperature



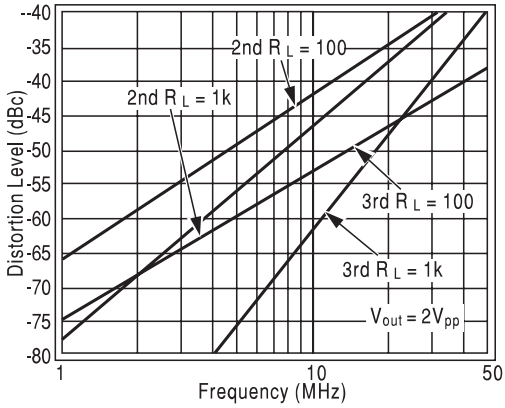
DS012712-20

Equivalent Input Noise



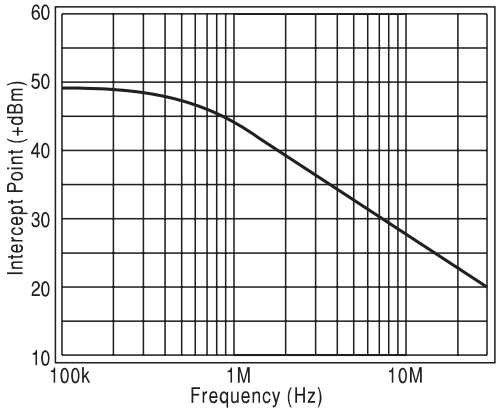
DS012712-21

2nd and 3rd Harmonic distortion



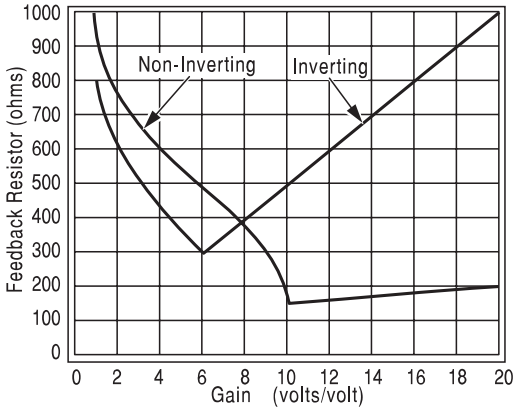
DS012712-22

2-Tone, 3rd-Order Intermod. Intercept



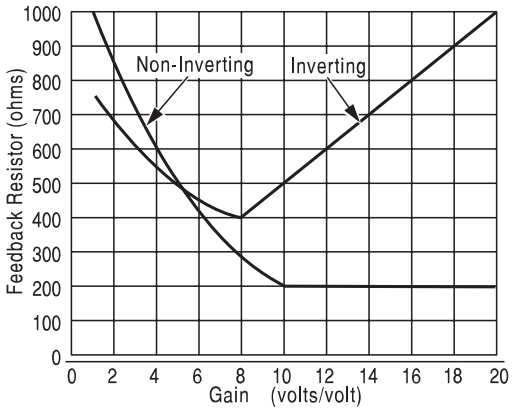
DS012712-23

Recommended $R_f$vs. Gain (CLC432)



DS012712-24

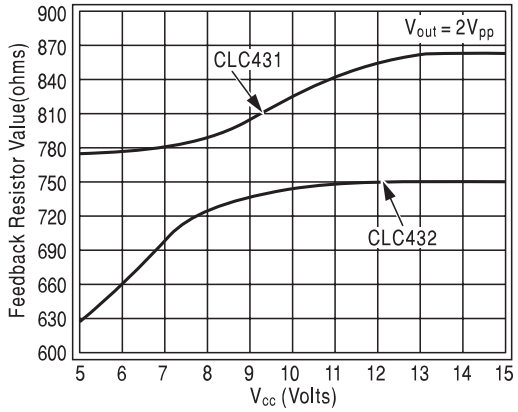
Recommended $R_f$vs. Gain (CLC431)



DS012712-25

Typical Performance Characteristics (T_A = +25˚C, A_V = +2, V_{CC} = ±15V, unless specified) (Continued)

Recommended R_f vs. V_{CC} (A_V = +2)



DS012712-26

Application Division

Introduction

The CLC431 and the CLC432 are dual wideband current-feedback op amps that operate from single (+10V to +33V) or dual (±5V to ±16.5) power supplies. The CLC431 is equipped with a disable feature and is offered in 14-dip DIP and SOIC packages. The CLC432 is packaged in a standard 8-pin dual pinout and is offered in an 8-pin DIP and SOIC. Evaluation boards are available for each version of both devices. The evaluation boards can assist in the device and/or application evaluation and were used to generate the typical device performance plots on the preceding pages.

Each of the CLC431/CLC432's dual channels provide closely matched DC & AC electrical performance characteristics making them ideal choices for wideband signal processing. The CLC431, with its disable features, can easily be configured as a 2:1 mux or several can be used to form a 10:1 mux without performance degradation. The two closely-matched channels of the CLC432 can be combined to form composite circuits for such applications as filter blocks, integrators, transimpedance amplifiers and differential line drives and receivers.

Feedback Resistor Selection

The loop gain and frequency response for a current-feedback operational amplifier is determined largely by the feedback resistor (R_f). Package parasitic also influence ac response. Since the package parasitics of the CLC431 and the CLC4332 are different, the optimum frequency and phase response are obtained with different values of feedback resistor (for A_V= +2; CLC431: R_f = 866Ω, CLC432: R_f = 750Ω). The Electrical Characteristics and Typical Performance plot are valid for both devices under the specified conditions. Generally, lowering R_f from its recommended value will peak the frequency response and extended the bandwidth while increasing its value will roll off the response. Reducing the value of R_f too far below its recommended value will cause overshoot, ringing and eventually oscillation. For more information see Application Note OA-20 and OA-13.

In order to minimize the devices' frequency and phase response for gains other than +2V/V it is recommended to adjust the value of the feedback resistor. The two plots found in the Typical Performance section entitled "Recommended R_f vs. Gain" provide the means of selecting the feedback-resistor value that optimizes frequency and phase response over the CLC431/CLC432's gain range. Both pots show the value of R_f approaching a nonzero minimum at high non-inverting gains, which is characteristic of current-feedback op amps and yields best results. The linear portion of the two R_f vs. Inverting-gain curves results from the limitation placed on R_g (i.e. $R_g \geq 50\Omega$) in order to maintain an adequate input impedance for the inverting configuration. It should be noted that for stable operation a non-inverting gain of +1 requires an R_f equal to 1kΩ for both the CLC431 and the CLC4332.

CLC431 Disable Feature

The CLC431 disable feature can be operated either single-endedly or differentially thereby accommodating a wide range of logic families. There are three pins associated with the disable feature of each of the CLC431's two amplifiers: DIS,$\overline{DIS}$ and V_{RTTL} (please see pinout on front page). Also note that both amplifiers are guaranteed to be enabled if all three of these pins are unconnected.

Figure 1 illustrates the single-ended mode of the CLC431's disable feature for logic families such as TTL and CMOS. In order to operate properly, V_{RTTL} must be grounded, thereby biasing $\overline{DIS}$ to approximately +1.4V through the two internal series diodes. For single-ended operation, $\overline{DIS}$ should be left floating. Applying a TTL or CMOS logic "high" (i.e.>2.0Volts) to DIS will switch the tail current of the differential pair to Q1 and "shut down" Q2 which results in the disabling of that channel of the CLC431. Alternatively, applying a logic "low" (i.e. <0.8Volts) to DIS will switch the tail current from Q1 to Q2 effectively enabling that channel. If DIS is left floating under single-ended operation, then the associated amplifier is guaranteed to be disabled.

Application Division (Continued)

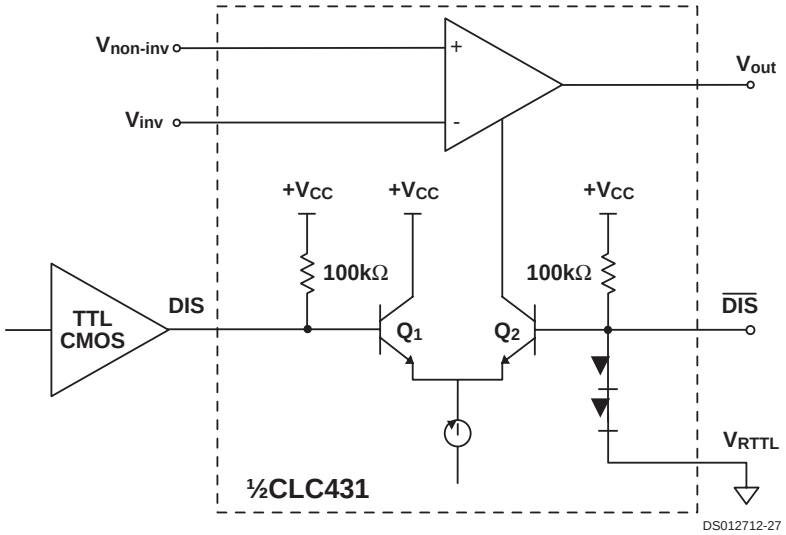


FIGURE 1.

The disable feature of the CLC431 is such that DIS and $\overline{DIS}$ have common-mode input voltage ranges of ($+V_{CC}$) to ($-V_{CC}+3V$) and are so guaranteed over the commercial temperature range. Internal clamps (not shown) protect the DIS input from excessive input voltages that could otherwise cause damage to the device. This condition occurs when enough source current flows into the node so as to allow DIS to rise to V_{CC}. This clamp is activated once DIS exceeds $\overline{DIS}$ by 1.5Volts and guarantees that V_{DIS}(ground referenced) does not exceed 4.7Volts.

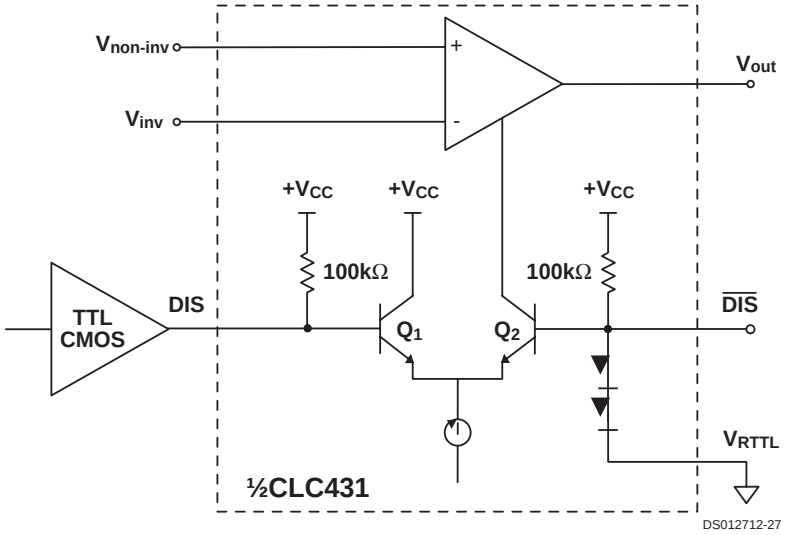


FIGURE 2.

Figure 2 illustrates the differential mode of the CLC431's disable feature for ECL-type logic. In order for this mode to operate properly, V_{RTTL} must be left floating while DIS and $\overline{DIS}$ are to be connected directly to the ECL gate as illustrated. Applying a differential logic "high" (DIS - $\overline{DIS} \geq$ 0.4Volts) switches the tail current of the differential pair from Q2 to Q1 and results in the disabling of that CLC431 channel. Alternatively, applying a differential logic "low" (DIS - $\overline{DIS} \leq -0.4$Volts) switches the tail current of the differential pair from Q1 to Q2 and results in the enabling of that same channel. The internal clamp, mentioned above, also protects against excessive differential voltages up to 30 Volts while limiting input currents to <3mA.

DC Performance

A current-feedback amplifier's input stage does not have equal nor correlated bias currents, therefore they cannot be cancelled and each contributes to the total DC offset voltage at the output by the following equation:

$$V_{offset} = \pm \left(I_{bn} * R_s \left(1 + \frac{R_f}{R_g} \right) + V_{io} \left(1 + \frac{R_f}{R_g} \right) + I_{bi} * R_f \right) \quad (1)$$

The input resistor R_s is that resistance seen when looking from the non-inverting input back towards the source. For inverting DC-offset calculations, the source resistance seen

Application Division (Continued)

by the input resistor R_g must be included in the output offset calculation as a part of the non-inverting gain equation. Application note OA-7 gives several circuits for DC offset correction.

Layout Considerations

It is recommended that the decoupling capacitors (0.1µF ceramic and 6.8µF electrolytic) should be placed as close as possible to the power supply pins to insure a proper high-frequency low impedance bypass. Careful attention to circuit board layout is also necessary for best performance. Of particular importance is the control of parasitic capacitances (to ground) at the output and inverting input pins. See CLC431/CLC432 Evaluation Board literature for more information.

Applications Circuit

2:1 Video Mux (CLC431)

Figure 3 illustrates the connections necessary to configure the CLC431 as a 2:1 multiplexer in a 75Ω. Each of the two CLC431's amplifiers is configured with a non-inverting gain of +2V/V using 634Ω feedback (R_f) and gain-setting (R_g) resistors . The feedback resistor value is lower than that recommended in order to compensate for the reduction of loop-gain that results from the inclusion of the 50Ω resistor (R_j) in the feedback loop. The 50Ω resistor serves to insolate the output of the active channel from the impedance of inactive channel yet does not affect the low output impedance channel. Notice that for proper operation V_{RTTL} 1(pin 13) is grounded and V_{RTTL}2 (pin 9) is unconnected. The pins associated with the disable feature are to be connected as follows: DIS1 and $\overline{\text{DIS2}}$ ($\overline{\text{pins}}$ 3 & 10) are connected together as well as DIS2 and $\overline{\text{DIS1}}$ (pins 5 & 12). Channel 1 is selected with the application of a logic "low" to SELECT while a logic "high" selects Channel 2.

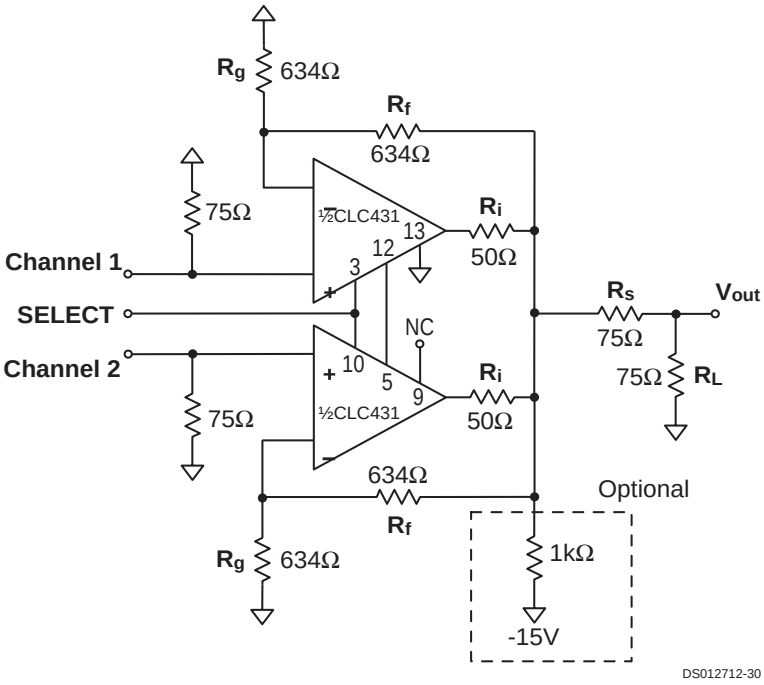


FIGURE 3.

The optional 1kΩ pull-down resistor connected from the output of the 2:1 mux to the negative power supply ($-V_{CC}$) results in improved differential gain and phase performance (0.02% and 0.01˚) at PAL video levels.

Switched Gain Amplifier (CLC431)

As seen from the front page, the CLC431 can also be configured as a switched-gain amplifier that is similar to the 2:1 mux. Configuring each of the two CLC431's amplifiers with different non-inverting gains and tying the two inputs together (eliminating one of the input-terminating resistors) allows the CLC431 to switch an input signal between two different gains.

Inactive Channel Impedances (CLC431)

The impedance that is seen when looking into the output of a disabled CLC431 is typically represented as 1MΩ‖16pF. The inverting input impedance becomes very high, essentially open. Therefore, the impedance presented by a disabled channel is (R_f+ R_g)‖ (R_j + (1MΩ‖16pF)) as illustrated in *Figure 4*. Its should also be noted that any trace capacitance that is associated with the common output connection will add in parallel to that presented by the CLC431's inactive channel.

Application Division (Continued)

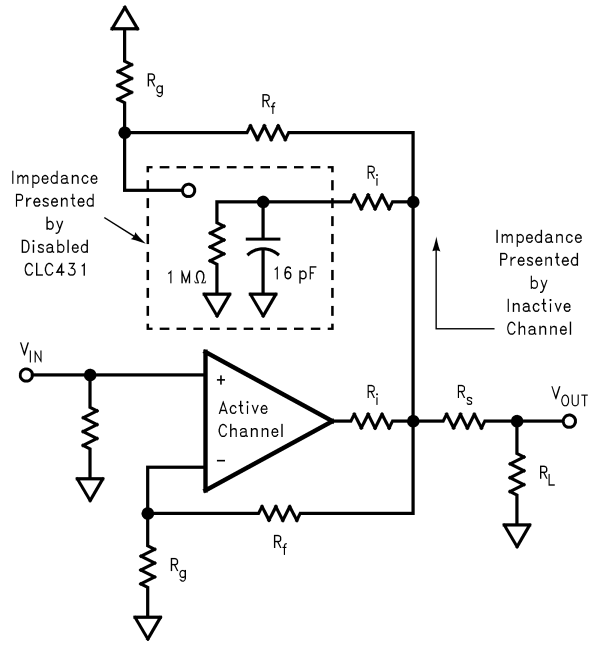


FIGURE 4.

Twisted-Pair Driver

Twisted-pair cables are used in many applications such as telephony, video and data communications. The CLC432's two matched channels make it well suited for such applications and is illustrated in *Figure 5*

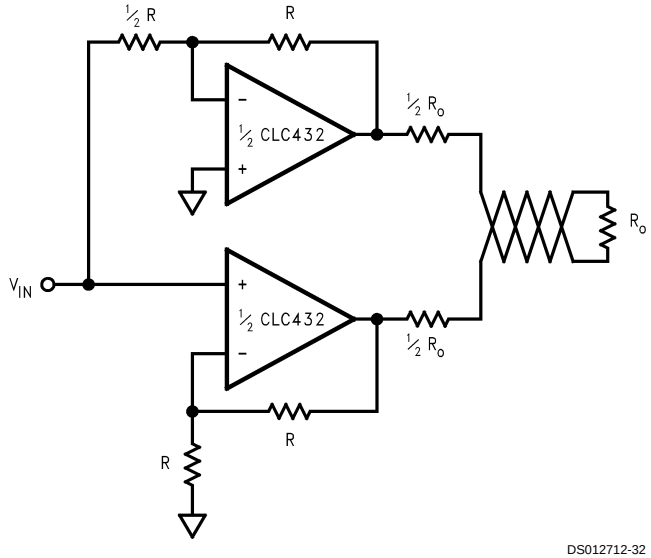


FIGURE 5.

Application Division (Continued)

CCD Amplifier

The CLC432 can easily be configured as 10MSPS CCD amplifier with DC level shifting as illustrated in *Figure 6*. Notice that one of the CLC432's channels buffers the CCD output while the other channel is configured with both an inverting DC gain and an AC gain in order to achieve the overall transfer function shown in *Figure 6*

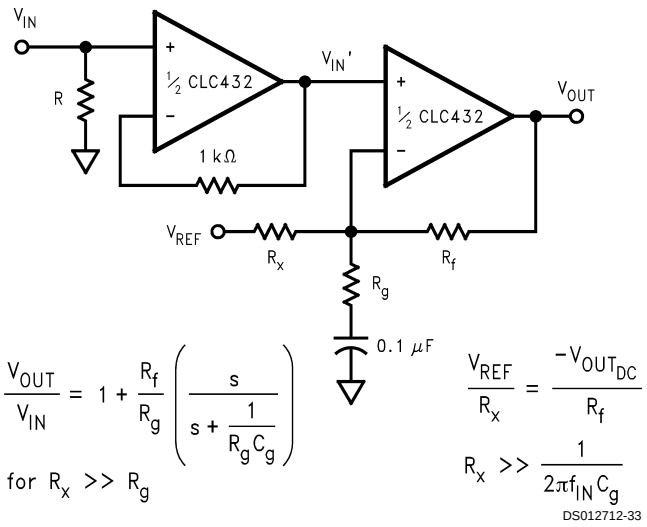
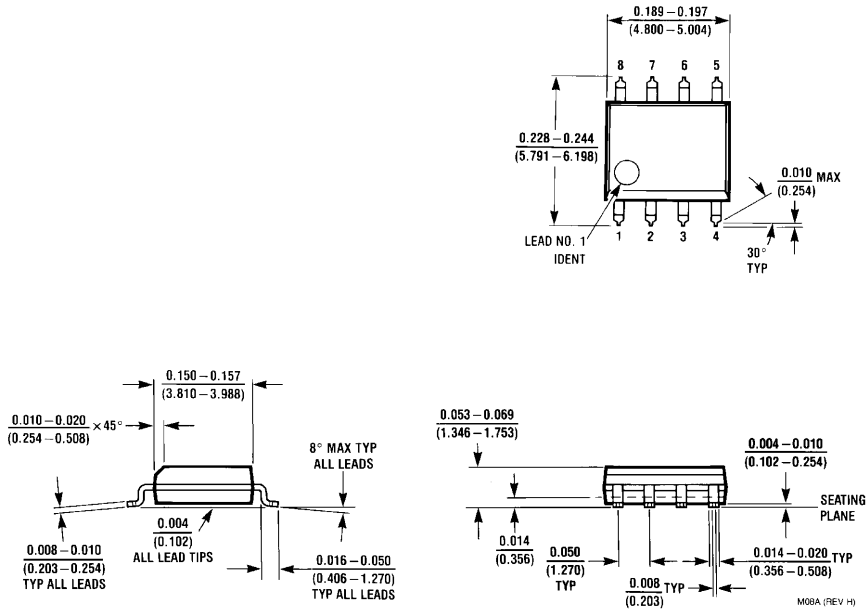
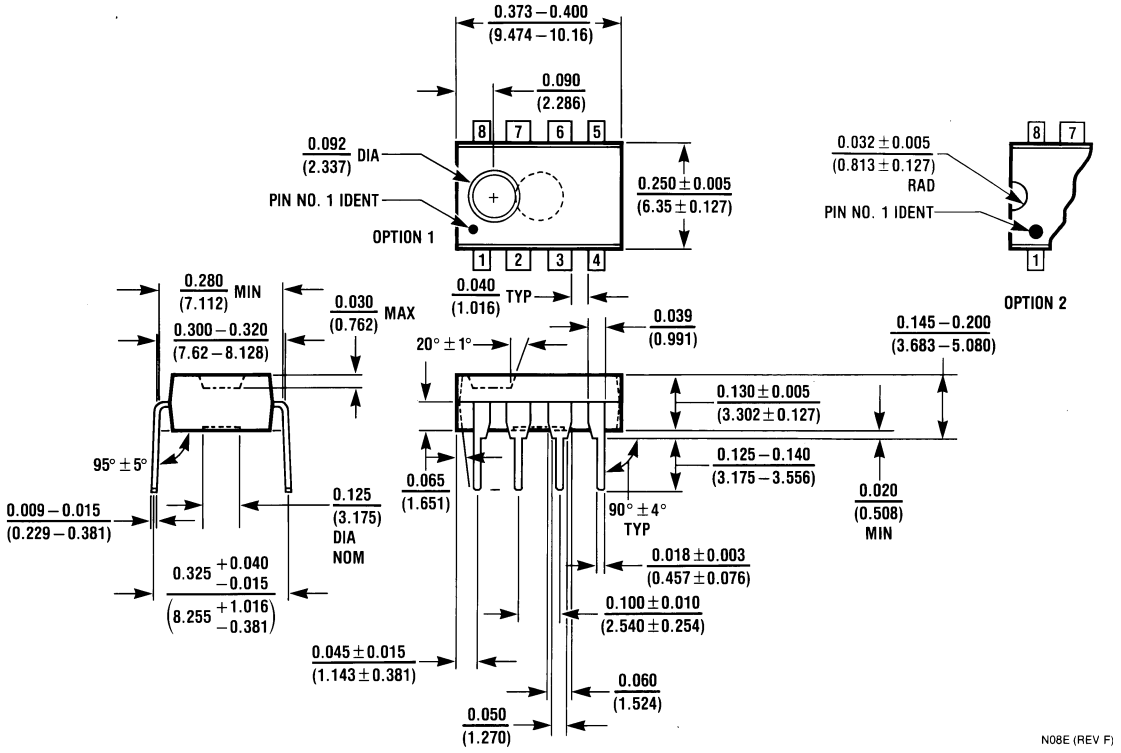


FIGURE 6.

Physical Dimensions inches (millimeters) unless otherwise noted

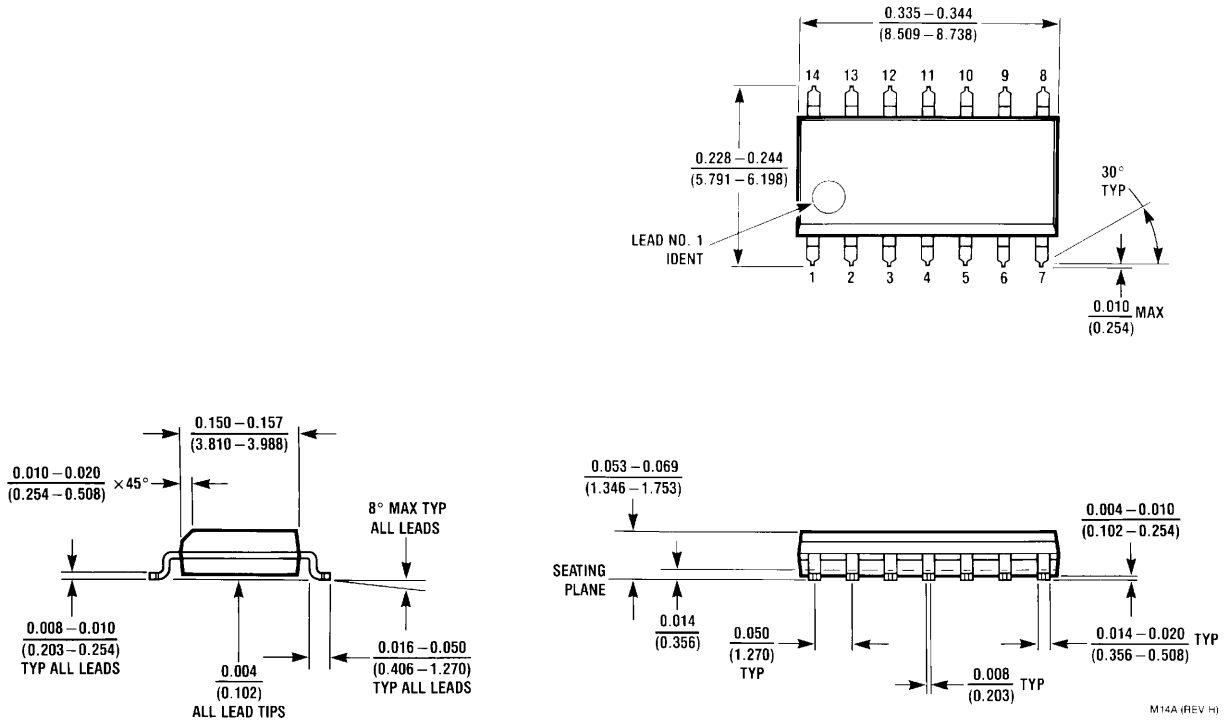


8-Pin SOIC
NS Package Number M08A

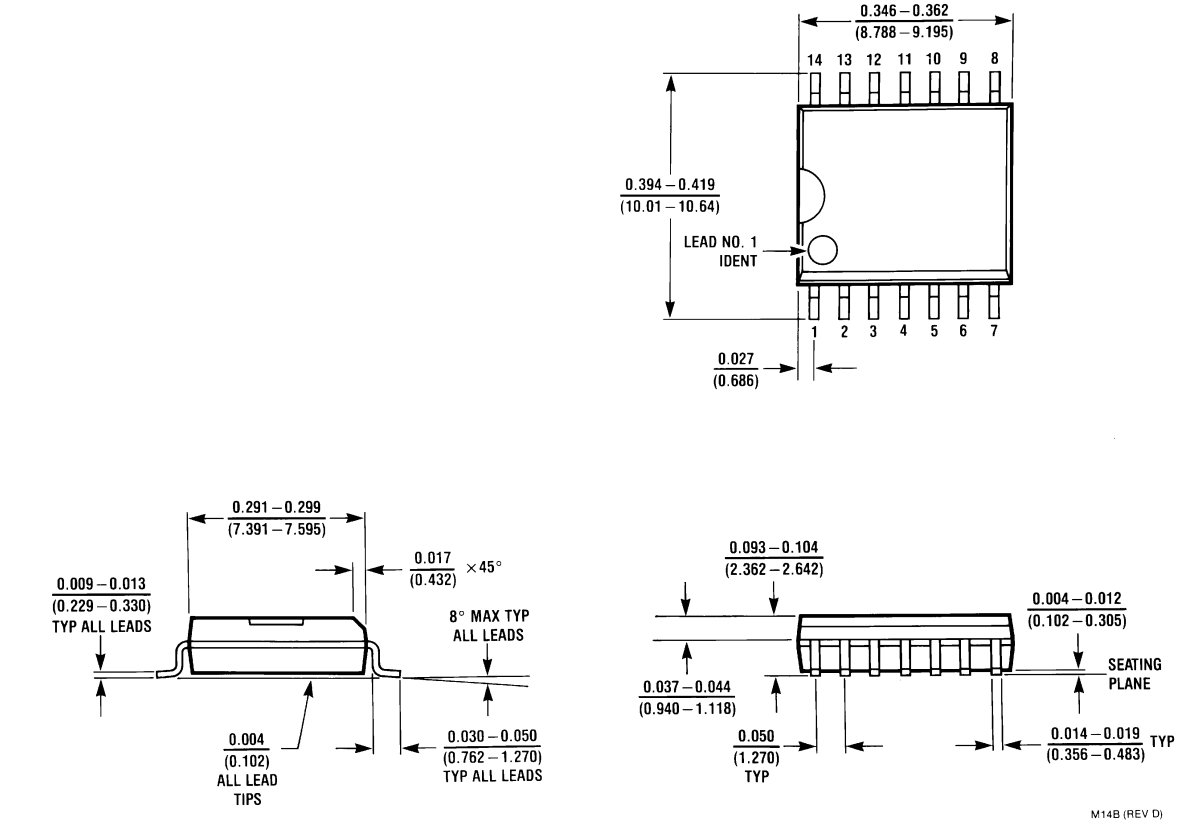


8-Pin MDIP
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

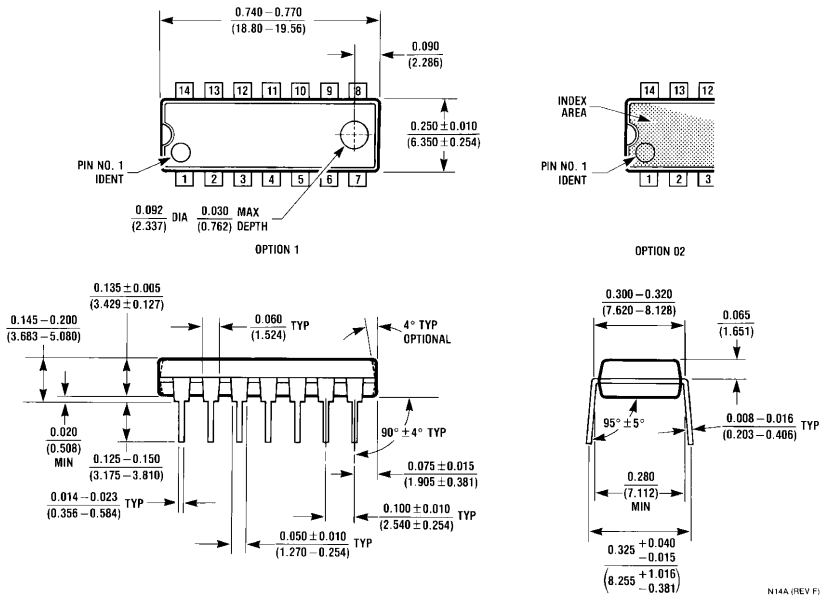


14-Pin SOIC
NS Package Number M14A



14-Pin SOIC
NS Package Number M14B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Pin MDIP
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