CGS2535V/CGS2535TV Commercial Quad 1 to 4 Clock Drivers/Industrial Quad 1 to 4 Clock Drivers

Check for Samples: CGS2535TV, CGS2535V

FEATURES

- **Guaranteed:**
  - **1.0 ns rise and fall times while driving 12 inches of 50Ω microstrip terminated with 25 pF**
  - **350 ps pin-to-pin skew (t_{OSLH} and t_{OSHL})**
- **650 ps part-to-part variation on positive or negative transition @ 5V V_{CC}**
- **Operates with either 3.3V or 5.0V supply**
- **Inputs 5V tolerant with V_{CC} in 3.3V range**
- **Symmetric output current drive: 24 mA I_{OH}/I_{OL}**
- **Industrial temperature range −40°C to +85°C**
- **Symmetric package orientation**
- **Large fanout for memory driving applications**
- **Guaranteed 2 kV ESD protection**
- **Implemented on National's ABT family process**
- **28-pin PLCC for optimum skew performance**

DESCRIPTION

These Clock Generation and Support clock drivers are specifically designed for driving memory arrays requiring large fanouts while operating at high speeds.

The CGS2535 is a non-inverting 4 to 16 driver with CMOS I/O structures. The CGS2535 specification guarantees part-to-part skew variation.

Connection Diagram

Figure 1. Pin Assignment for 28-Pin PLCC

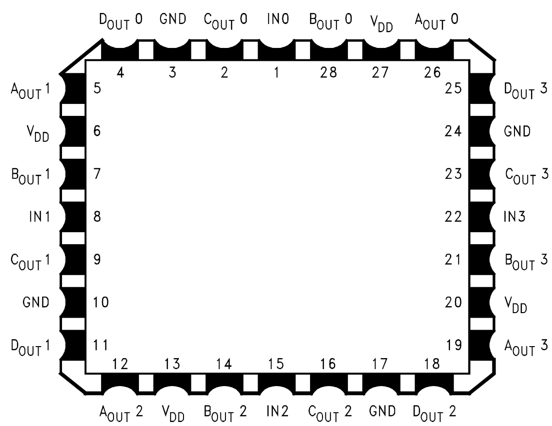

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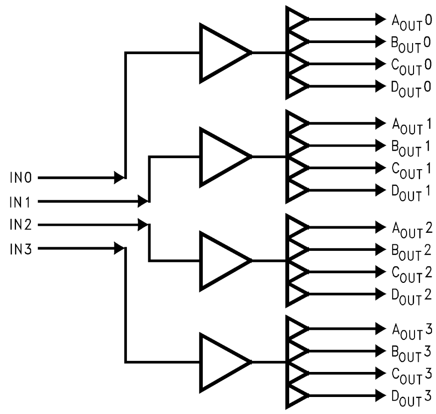
Figure 2. CGS2535



Truth Table

Input	Output
In (0–3)	ABCD Out (0–3)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{CC})	7.0V
Input Voltage (V_I)	7.0V
Input Current	−30 mA
Current Applied to Output	
(High/Low)	Twice the Rated I_{OH}/I_{OL}
Operating Temp. Industrial grade	−40°C to +85°C
Comm. grade	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Airflow	Typical θ_{JA}
0 LFM	62°C/W
225 LFM	43°C/W
500 LFM	34°C/W
900 LFM	27°C/W

(1) The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage	V_{CC} 4.75V to 5.25V
	V_{CC} 3.0V to 3.6V
Maximum Input Rise/Fall Time	
(0.8V to 2.0V)	5 ns
Free Air Operating Temperature	
Commercial	0°C to + 70°C
Industrial	−40°C to + 85°C

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Typ	Max	Units
V_{IH}	Input High Level Voltage		3.0	2.1			V
			4.5	3.15			
			5.5	3.85			
V_{IL}	Input Low Level Voltage		3.0			0.9	V
			4.5			1.35	
			5.5			1.65	
V_{IK}	Input Clamp Voltage	I_I = −18 mA	4.5			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −50 μA	3.0	2.9			V
			4.5	4.4			
			5.5	5.4			
		I_{OH} = −24 mA	3.0	2.46			V
			4.5	3.76			
			5.5	4.76			
V_{OL}	Low Level Output Voltage	I_{OL} = 50 μA	3.0			0.1	V
			4.5			0.1	
			5.5			0.1	
		I_{OL} = 24 mA	3.0			0.44	V
			4.5			0.44	
			5.5			0.44	
I_I	Input Current @ Max Input Voltage	V_{IH} = 7V	5.5			7	μA
		V_{IH} = V_{CC}	3.6			1	
I_{IH}	High Level Input Current	V_{IH} = V_{CC}	5.5			5	μA
I_{IL}	Low Level Input Current	V_{IL} = 0V	5.5	−5			μA
I_{OLD}	Minimum Dynamic Output Current (1)	V_{OLD} = 1.65V (max)	5.5	75			mA
		V_{OLD} = 0.9V (max)	3.0 (2)	36			
I_{OHD}	Minimum Dynamic Output Current (1)	V_{OHD} = 3.85V (min)	5.5	−75			mA
		V_{OHD} = 2.1V (min)	3.0 (2)	−25			
I_{CC}	Supply Current		3.6			75	μA
			5.5			235	
C_{IN}	Input Capacitance		5.0		5		pF

(1) Maximum test duration 2.0 ms, one output loaded at a time.
(2) At V_{CC} = 3.3V, I_{OLD} = 55 mA min; @ V_{CC} = 3.6V, I_{OLD} = 64 mA min At V_{CC} = 3.3V, I_{OHD} = −58 mA min; @ V_{CC} = 3.6V, I_{OHD} = −66 mA min

AC Electrical Characteristics [1] [2] [3]

Over recommended operating free air temperature specified. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V_{CC} (V) [5]	CGS2535 T_A = +25°C C_L = 50 pF, R_L = 500Ω			T_A = −40°C to +85°C [4] C_L = 50 pF, R_L = 500Ω			Units
			Min	Typ	Max	Min	Typ	Max	
f_{max}	Frequency Maximum	3.0					100		MHz
		5.0					125		
t_{PLH}	Low-to-High Propagation Delay	3.3			4.5	2.5		4.5	ns
	CK to O_n @ 1 MHz [6]	5.0			3.5	2.0		3.5	
t_{PHL}	High-to-Low Propagation Delay	3.3			4.5	2.5		4.5	ns
	CK to O_n @ 1 MHz [6]	5.0			3.5	2.0		3.5	
t_{PLH}	Low-to-High Propagation Delay	3.3			5.0	2.5		5.0	ns
	CK to O_n @ 66.67 MHz [6] [7]	5.0			4.5	2.0		4.5	
t_{PHL}	High-to-Low Propagation Delay	3.3			5.0	2.5		5.0	ns
	CK to O_n @ 66.67 MHz [6] [7]	5.0			4.5	2.0		4.5	
t_{OSLH}	Maximum Skew Common Edge	3.3		150	350		300	350	ps
	Output-to-Output Variation	5.0		150	350		300	350	
	[1] [3]								
t_{OSHL}	Maximum Skew Common Edge	3.3		150	350		300	350	ps
	Output-to-Output Variation	5.0		150	350		300	350	
	[1] [3]								
t_{rise},	Rise/Fall Time	3.3			3.5			3.5	ns
t_{fall}	(from 0.8V/2.0V to 2.0V/0.8V) [8]	5.0			3.0			3.0	
t_{rise},	Rise/Fall Time	3.3			0.8			1.0	ns
t_{fall}	(from 0.8V/2.0V to 2.0V/0.8V) [9] [7]	5.0			0.4			0.6	
t_{rise},	Rise/Fall Time	3.3			1.0			1.0	ns
t_{fall}	(from 0.8V/2.0V to 2.0V/0.8V) [10] [7]	5.0			0.7			0.9	
t_{High}	Pulse Width Duration High	3.3	4.0			4.0			ns
	[2] [3] [7]	5.0	4.0			4.0			
t_{Low}	Pulse Width Duration Low	3.3	4.0			4.0			
	[2] [3] [7]	5.0	4.0			4.0			
t_{PVLH}	Part-to-Part Variation of	3.3			650			1.0	ns
	Low-to-High Transitions	5.0			650			650	ps
	@ 1 MHz [6]								
t_{PVHL}	Part-to-Part Variation of	3.3			650			1.0	ns
	High-to-Low Transitions	5.0			650			650	ps
	@ 1 MHz [6]								

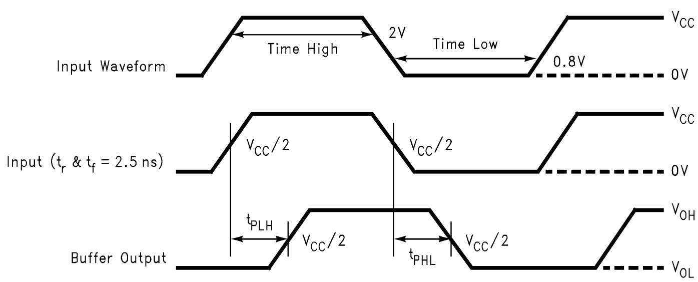
(1) Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device and output bank. The specifications apply to any outputs switching in the same direction either LOW to HIGH (t_{OSLH}) or HIGH to LOW (t_{OSHL}).
(2) Time high is measured with outputs at 2.0V or above. Time low is measured with outputs at 0.8V or below. Input waveform characteristics for t_{High}, t_{Low} measurement: f = 66.67 MHz, duty cycle = 50%.
(3) The input waveform has a rise and fall time transition time of 2.5 ns (10% to 90%).
(4) Industrial range (−40°C to +85°C) limits apply to the commercial temperature range (0°C to +70°C).
(5) Voltage Range 5.0 is 5.0V ± 0.25V, 3.3 is 3.3V ± 0.3V.
(6) All 16 outputs switching simultaneously.
(7) Guaranteed by design.
(8) These Rise and Fall times are measured with C_L = 50 pF, R_L = 500Ω (see Figure 3).
(9) These Rise and Fall times are measured with C_L = 25 pF, R_L = 500Ω (see Figure 3), and are guaranteed by design.
(10) These Rise and Fall times are measured driving 12 inches of 50Ω microstrip terminated with equivalent C_L = 25 pF (see Figure 4), and are guaranteed by design.

AC Electrical Characteristics (1) (2) (3) (continued)

Over recommended operating free air temperature specified. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V_{CC} (V) (5)	CGS2535 T_A = +25°C, C_L = 50 pF, R_L = 500Ω			CGS2535 T_A = −40°C to +85°C (4), C_L = 50 pF, R_L = 500Ω			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PVLH}	Part-to-Part Variation of	3.3			1.0			1.0	ns
	Low-to-High Transitions	5.0			1.0			1.0	
	@ 66.67 MHz (6) (7)								
t_{PVHL}	Part-to-Part Variation of	3.3			1.0			1.0	
	High-to-Low Transitions	5.0			1.0			1.0	
	@ 66.67 MHz (6) (7)								

Timing Information



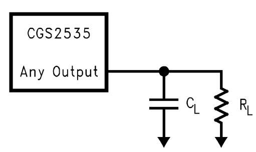


Figure 3. A.C. Load (11) (12)
C_L = Total Load Including Probes

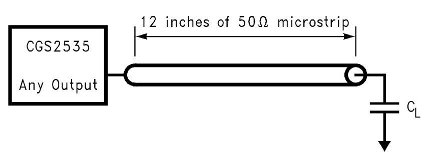


Figure 4. A.C. Load (13)
C_L = Total Load Including Probes

CGS2534/35/36/37

MEMORY ARRAY DRIVING

In order to minimize the total load on the address bus, quite often memory arrays are driven by buffers while having the inputs of the buffers tied together. Although this practice was feasible in the conventional memory designs, in today's high speed, large buswidth designs which require address fetching at higher speeds, this technique produces many undesired results such as cross-talk and over/undershoot.

(11) These Rise and Fall times are measured with C_L = 50 pF, R_L = 500Ω (see Figure 3).
(12) These Rise and Fall times are measured with C_L = 25 pF, R_L = 500Ω (see Figure 3), and are guaranteed by design.
(13) These Rise and Fall times are measured driving 12 inches of 50Ω microstrip terminated with equivalent C_L = 25 pF (see Figure 4), and are guaranteed by design.

CGS2534/35/36/37 Quad 1 to 4 clock drivers were designed specifically to address these application issues on high speed, large memory arrays systems.

These drivers are optimized to drive large loads, with 3.5 ns propagation delays. These drivers produce less noise while reducing the total capacitive loading on the address bus by having only four inputs tied together (see the diagram below, point A). This helps to minimize the overshoot and undershoot by having only four outputs being switched simultaneously.

Also this larger fan-out helps to save board space since for every one of these drivers, two conventional buffers were typically being used.

Another feature associated with these clock drivers is a 350 ps pin-to-pin skew specification. The minimum skew specification allows high speed memory system designers to optimize the performance of their memory sub-system by operating at higher frequencies without having concerns about output-to-output (bank-to-bank) synchronization problems which are associated with driving high capacitive loads (Point B).

The diagram below depicts a “2534/35/36/37” a memory subsystem operating at high speed with large memory capacity. The address bus is common to both the memory and the CPU and I/Os.

These drivers can operate beyond 125 MHz, and are also available in 3V–5V TTL/CMOS versions with large current drive .

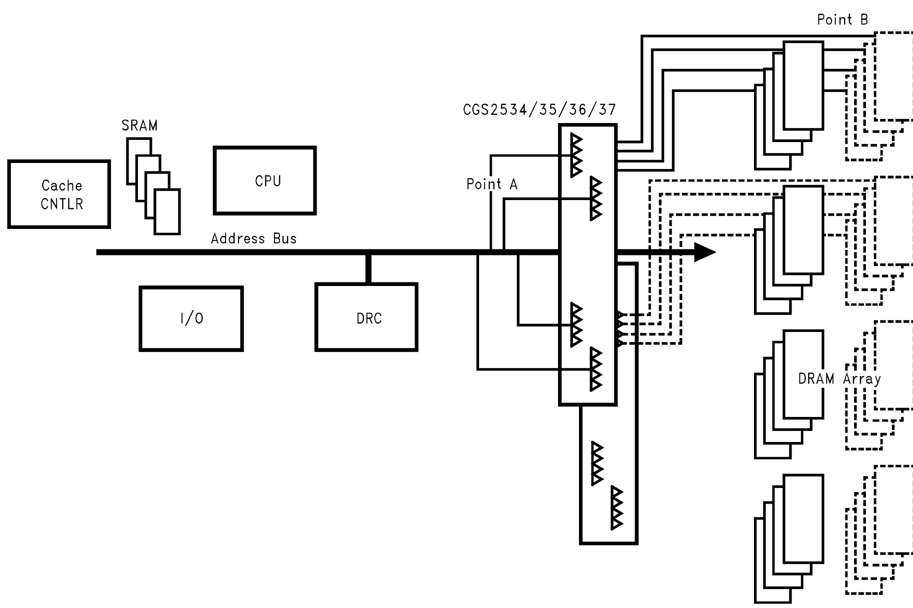


Figure 5. “2534/35/36/37"

Device	V_{CC}	I/O	Output Configuration
2534	5	TTL	Inverting quad 1–4
2535	3 or 5	CMOS	Non-inverting quad 1–4
2536	3 or 5	CMOS	Inverting, Non-inverting, ÷2
2537	5	TTL	Inverting quad 1–4 with series 8Ω output resistors

Part Numbering Information