

## High-Reliability CMOS 32-Word x 8-Bit Static Random-Access Memory

March 1997

### Features

- Access Time
  - 610ns..... at  $V_{DD} = 5V$
  - 320ns..... at  $V_{DD} = 10V$
- No Precharge or Clock Required

### Ordering Information

5V	10V	PACK-AGE	TEMP. RANGE	PKG. NO.
CDP1824CD3	CDP1824D3	SBDIP	-55°C to +125°C	D18.3

### Description

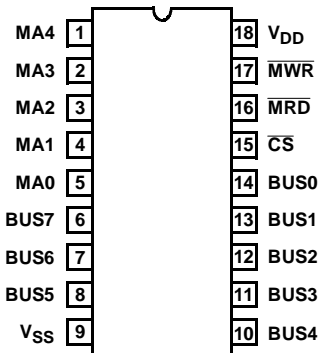
The CDP1824/3 and CDP1824C/3 types are high-reliability CMOS 32-word x 8-bit fully static random-access memories for use in CDP1800-series microprocessor systems. These parts are compatible with the CDP1802 microprocessor and will interface directly without additional components.

The CDP1824/3 is fully decoded and does not require a pre-charge or clocking signal for proper operation. It has common input and output and is operated from a single voltage supply. The MRD signal (output disable control) enables the three-state output drivers, and overrides the MWR signal. A  $\overline{CS}$  input is provided for memory expansion.

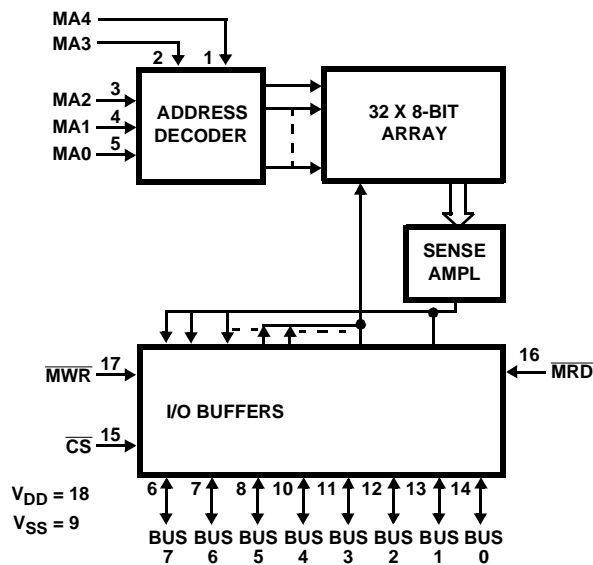
The CDP1824C/3 is functionally identical to the CDP1824/3. The CDP1824/3 has a recommended operating voltage range of 4V to 10.5V, and the CDP1824C/3 has an operating voltage range of 4V to 6.5V.

### Pinout

CDP1824/3, CDP1824C/3 (SBDIP)  
TOP VIEW



### Functional Diagram



### OPERATIONAL MODES

FUNCTION	$\overline{CS}$	$\overline{MRD}$	$\overline{MWR}$	DATA PINS STATUS
READ	0	0	X	Output: High/Low Dependent on Data
WRITE	0	1	0	Input: Output Disabled
Not Selected	1	X	X	Output Disabled: High-Impedance State
Standby	0	1	1	Output Disabled: High-Impedance State

Logic 1 = High Logic 0 = Low X = Don't Care

## CDP1824/3, CDP1824C/3

### Absolute Maximum Ratings

DC Supply Voltage Range, ( $V_{DD}$ ) (All Voltages Referenced to $V_{SS}$ Terminal)	
CDP1824/3	-0.5V to +11V
CDP1824C/3	-0.5 to +7V
Input Voltage Range, All Inputs	-0.5V to $V_{DD}$ +0.5V
DC Input Current, Any One Input	$\pm 10$ mA

### Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}$ C/W)	$\theta_{JC}$ ( $^{\circ}$ C/W)
SBDIP Package	75	20
Device Dissipation Per Output Transistor		
$T_A$ = Full Package Temperature Range (All Package Types)	100mW	
Operating Temperature Range ( $T_A$ )		
Package Type D	-55 $^{\circ}$ C to +125 $^{\circ}$ C	
Storage Temperature Range ( $T_{STG}$ )	-65 $^{\circ}$ C to +150 $^{\circ}$ C	
Lead Temperature (During Soldering)		
At distance 1/16" $\pm$ 1/32 In. (1.59 $\pm$ 0.79mm)		
from case for 10s max.	+265 $^{\circ}$ C	

### Recommended Operating Conditions

$T_A$  = Full Package-Temperature Range. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	LIMITS				UNITS
	CDP1824/3		CDP1824C/3		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	$V_{SS}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	V

### Static Electrical Specifications

PARAMETER	SYMBOL	CONDITIONS			LIMITS				UNITS
		$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55 $^{\circ}$ C, +25 $^{\circ}$ C		+125 $^{\circ}$ C		
					MIN	MAX	MIN	MAX	
Quiescent Device Current (Note 1)	$I_{DD}$	-	0, 5	5	-	50	-	500	$\mu$ A
		-	0, 10	10	-	500	-	1000	$\mu$ A
Output Voltage Low-Level (Note 2)	$V_{OL}$	-	0, 5	5	-	0.1	-	0.2	V
		-		10	-	0.1	-	0.2	V
Output Voltage High-Level (Note 2)	$V_{OH}$	-	0, 5	5	4.9	-	4.8	-	V
		-	-	10	9.9	-	4.8	-	V
Input Low Voltage	$V_{IL}$	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	-	V
Input High Voltage	$V_{IH}$	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
Output Low Drive (Sink) Current	$I_{OL}$	0.4	0, 5	5	4	-	1.5	-	mA
		0.5	0, 10	10	4	-	2.9	-	mA
Output High Drive (Source) Current	$I_{OH}$	4.6	0, 5	5	-	-1	-	-0.75	mA
		9.5	0, 10	10	-	-2	-	-1.5	mA
Input Current	$I_{IN}$	Any Input	0, 5	5	-	$\pm 1$	-	$\pm 5$	$\mu$ A
			0, 10	10	-	$\pm 1$	-	$\pm 5$	$\mu$ A
Three-State Output Leakage Current	$I_{OUT}$	0, 5	0, 5	5	-	$\pm 2$	-	$\pm 5$	$\mu$ A
		0, 10	0, 10	10	-	$\pm 2$	-	$\pm 5$	$\mu$ A
Input Capacitance	$C_{IN}$	(Note 2)			-	10	-	10	pF
Output Capacitance	$C_{OUT}$	(Note 2)			-	15	-	15	pF

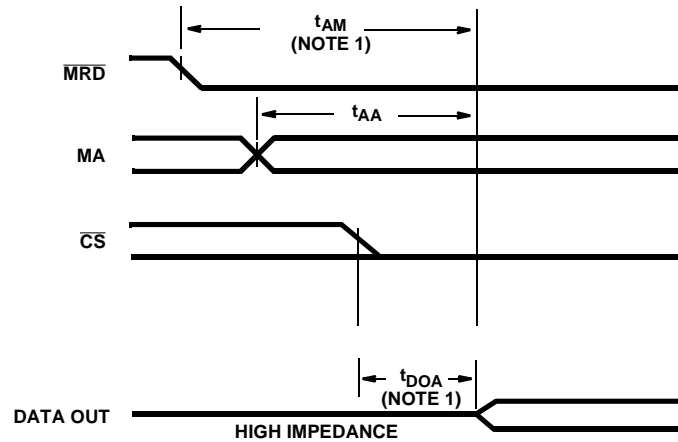
#### NOTES:

- The CDP1824C/3 meets all 5V Static Electrical Characteristics of the CDP1824/3 except Quiescent Device Current for which the limits are  $I_{DD} = 200\mu$ A at +25 $^{\circ}$ C/-55 $^{\circ}$ C;  $I_{DD} = 1000\mu$ A at +125 $^{\circ}$ C.
- Guaranteed, but not tested.

## CDP1824/3, CDP1824C/3

### Read Cycle Dynamic Electrical Specifications Input $t_R, t_F \leq 15\text{ns}$ , $C_L = 50\text{pF}$

PARAMETER	SYMBOL	TEST CONDITIONS $V_{DD}$ (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			MIN	MAX	MIN	MAX	
Access Time From Address Change	$t_{AA}$	5	-	610	-	825	ns
		10	-	320	-	375	ns
Access Time From Chip Select	$t_{DOA}$	5	-	610	-	825	ns
		10	-	320	-	375	ns
Output Active From $\overline{\text{MRD}}$	$t_{AM}$	5	-	610	-	825	ns
		10	-	320	-	375	ns



**NOTE:**

1. Minimum timing for valid data output longer times will initiate an earlier, but invalid output.

**FIGURE 1. READ CYCLE TIMING DIAGRAM**

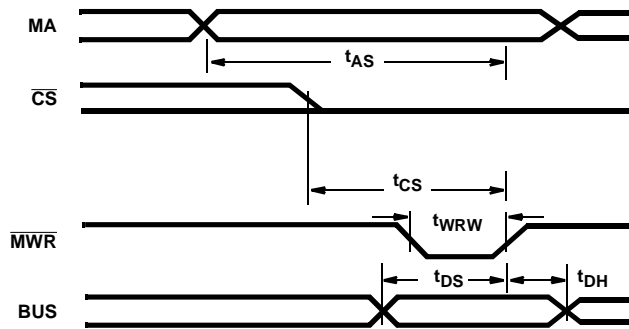
## CDP1824/3, CDP1824C/3

### Write Cycle Dynamic Electrical Specifications Input $t_R, t_F \leq 15\text{ns}$ , $C_L = 50\text{pF}$

PARAMETER	SYMBOL	TEST CONDITIONS $V_{DD}$ (V)	LIMITS				UNITS
			-55°C, +25°C		+125°C		
			(NOTE 1) MIN	MAX	(NOTE 1) MIN	MAX	
Write Pulse Width	$t_{WRW}$	5	350	-	475	-	ns
		10	180	-	220	-	ns
Data Setup Time	$t_{DS}$	5	400	-	560	-	ns
		10	190	-	260	-	ns
Data Hold Time	$t_{DH}$	5	70	-	90	-	ns
		10	35	-	45	-	ns
Chip Select Setup Time	$t_{CS}$	5	550	-	775	-	ns
		10	340	-	475	-	ns
Address Setup Time	$t_{AS}$	5	550	-	775	-	ns
		10	340	-	475	-	ns

**NOTE:**

1. Time required by a device to allow for the indicated function.



**FIGURE 2. WRITE CYCLE TIMING DIAGRAM**

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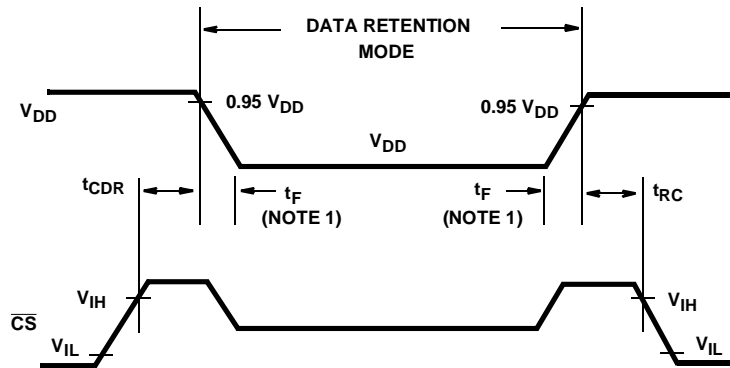
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## CDP1824/3, CDP1824C/3

### Data Retention Specifications At $T_A = +25^\circ\text{C}$

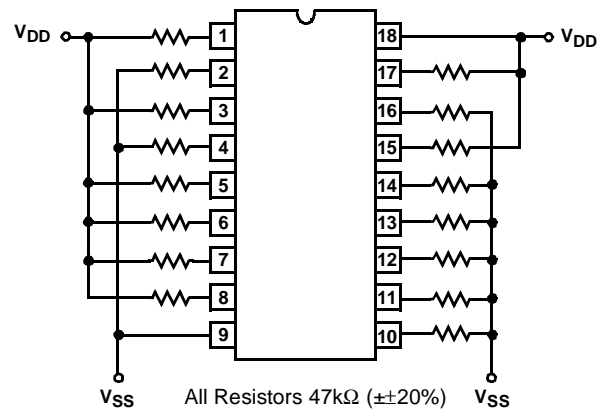
PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS				UNITS
				CDP1824/3		CDP1824C/3		
		$V_{DR}$ (V)	$V_{DD}$ (V)	MIN	MAX	MIN	MAX	
Data Retention Voltage	$V_{DR}$	-	-	2.5	-	2.5	-	V
Data Retention Quiescent Current	$I_{DD}$	2.5	-	-	10	-	40	$\mu\text{A}$
Chip Deselect to Data Retention Time	$t_{CDR}$	2.5	5	600	-	600	-	ns
		2.5	10	300	-	-	-	ns
Recovery to Normal Operation Time	$t_{RC}$	2.5	5	600	-	600	-	ns
		2.5	10	300	-	-	-	ns



NOTE:  $t_r, t_f > 1\mu\text{s}$ .

FIGURE 3. LOW  $V_{DD}$  DATA RETENTION WAVEFORMS AND TIMING DIAGRAM

### Static Burn-In Circuit



TYPE	$V_{DD}$	TEMPERATURE	TIME
CDP1824	11V	+125 $^\circ\text{C}$	160 Hrs., Min.
CDP1824C	7V	+125 $^\circ\text{C}$	160 Hrs., Min.