



ADVANCE INFORMATION

**CDC1607F-E**  
**Automotive Controller**  
**Specification**

Edition March 31, 2003  
6251-608-2A1

 **MICRONAS**

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# 1. Introduction

**Release Note:** Revision bars indicate significant changes to the previous edition.

The IC is a single-chip controller for use in automotive applications. The CPU on the chip is an upgrade of the 65C02 with 16-bit internal data and 24-bit address bus. The chip consists of timer/counters, an interrupt controller, a multichannel A/D converter, a stepper motor and LCD driver, CAN interfaces and PWM outputs. This document provides MCM Flash hardware-specific information. General information on operating the IC can be found in the document "CDC16xxF-E Automotive Controller Family User Manual" (6251-606-2A1).

## 1.1. Features

**Table 1-1:** CDC16xxF Family Feature List

**This Document:**

Item	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E MASK ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
<b>Core</b>								
CPU	16-bit 65C816, featuring software compatibility with its 8-bit NMOS and CMOS 6500-series predecessors							
CPU-Active Operation Modes	FAST, SLOW and DEEP SLOW			FAST and SLOW				
Power Saving Modes (CPU Inactive)	WAKE and IDLE			-				
EMI Reduction Mode	selectable in FAST mode							
Oscillators	4 MHz to 12 MHz Quartz, RC			4 MHz to 12 MHz Quartz				
RAM	6 KB		2 KB	6 KB		2.75 KB	4 KB	6 KB
ROM	ROMless, external program storage with up to 16 MB, internal 2 KB Boot ROM	256 KB Flash, bottom boot configuration, internal 2 KB Boot ROM	64 KB	ROMless, external program storage with up to 16 MB, internal 2 KB Boot ROM	256 KB Flash, bottom boot configuration, internal 2 KB Boot ROM	90 KB	128 KB	216 KB

Table 1–1: CDC16xxF Family Feature List, continued

Item	This Document:							
	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E MASK ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Multiplier, 8 by 8 bit	✓			-				
Digital Watchdog	✓							
Central Clock Divider	✓							
Interrupt Controller expanding NMI	16 inputs, 16 priority levels							
Port Interrupts including Slope Selection	4 inputs							
Port Wake-Up Inputs including Slope / Level Selection	✓			-				
Patch Module	10 ROM locations		5 ROM locations	10 ROM locations		5 ROM locations	6 ROM locations	
Boot System	allows in-system downloading of code and data into RAM via serial link		-	allows in-system downloading of code and data into RAM via serial link		-	-	-
<b>Analog</b>								
Reset/Alarm	Combined Input for Regulator Input Supervision							
Clock and Supply Supervision	✓							
10-bit ADC, charge balance type	9 channels (5 channels selectable as digital input)							
ADC Reference	VREF Pin							
Comparators	P06COMP with 1/2 AVDD reference							
LCD	Internal processing of all analog voltages for the LCD driver							

**Table 1–1:** CDC16xxF Family Feature List, continued

**This Document:**

Item	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E MASK ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
<b>Communication</b>								
DMA	1 DMA Channel for serving the Graphics Bus interface		-	1 DMA Channel for serving the Graphics Bus interface		-	1 DMA Channel for serving the Graphics Bus interface	
UART	3: UART0, UART1 and UART2		1: UART0	3: UART0, UART1 and UART2		1: UART0	3: UART0, UART1 and UART2	
Synchronous Serial Peripheral Interfaces	2: SPI0 and SPI1		1: SPI0	2: SPI0 and SPI1		1: SPI0	2: SPI0 and SPI1	
Full CAN modules V2.0B	3: CAN0, CAN1 and CAN2 with 256-byte object RAM each (LCAN000F)		1: CAN0 with 256-byte object RAM (LCAN000F)	3: CAN0, CAN1 and CAN2 with 256-byte object RAM each (LCAN0009)		1: CAN0 with 256-byte object RAM (LCAN0009)	2: CAN0 and CAN1 with 256-byte object RAM each (LCAN0009)	
DIGITbus	1 master module		-	1 master module		-	1 master module	
<b>Input &amp; Output</b>								
Universal Ports selectable as 4:1 mux LCD Segment/Backplane lines or Digital I/O Ports	up to 52 I/O or 48 LCD segment lines (=192 segments), in groups of two, configurable as I/O or LCD							
Universal Port Slew Rate	HW preselectable							
Stepper Motor Control Modules with High-Current Ports	5 Modules, 24 di/dt controlled ports							
8-bit PWM Modules	5 Modules: PWM0, PWM1, PWM2, PWM3 and PWM4		3 Modules: PWM0, PWM1, PWM2	5 Modules: PWM0, PWM1, PWM2, PWM3 and PWM4		2 Modules: PWM0, PWM1	5 Modules: PWM0, PWM1, PWM2, PWM3 and PWM4	
Audio Module with auto-decay	✓							
SW selectable Clock outputs	2							

**Table 1–1:** CDC16xxF Family Feature List, continued

Item	This Document:							
	CDC1605F-E EMU	CDC1607F-E MCM Flash	CDC1631F-E MASK ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Polling / Flash Timer Output	1 High-Current Port output operable in Power Saving Mode			-				
<b>Timers &amp; Counters</b>								
16-bit free running counters with Capture/ Compare modules	CCC0 with 3CAPCOM							
16-bit timers	1: T0							
8-bit timers	2: T1 and T2							
Real Time Clock, Delivering Hours, Minutes and Seconds	✓			-				
<b>Miscellaneous</b>								
Scalable layout in CAN, RAM and ROM	-	✓		-	✓			
Various randomly selectable HW options	Most options SW programmable, copy from user program storage during system start-up		Mask programmed according to user specification	Most options SW programmable, copy from user program storage during system start-up				
Core Bond-Out	✓	-		✓	-			
Supply Voltage	4.5 V to 5.5 V							
Temperature Range	T <sub>case</sub> : -40 to +105C			T <sub>amb</sub> : -40 to +85C				
<b>Package</b>								
Type	Ceramic 177PGA	Plastic 100QFP 0.65mm pitch		Ceramic 177PGA	Plastic 100QFP 0.65mm pitch			
Bonded Pins	176	100		176	100			

## 1.2. Abbreviations

AM	Audio Module
CAN	Controller Area Network Module
CAPCOM	Capture/Compare Module
CPU	Central Processing Unit
DMA	Direct Memory Access Module
ERM	EMI Reduction Module
IR	Interrupt Controller
LCD	Liquid Crystal Display Module
P06COMP	P0.6 Alarm Comparator
PINT	Port Interrupt Module
PSM	Power Saving Module
PWM	8-Bit Pulse Width Modulator Module
RTC	Real-time Clock
SM	Stepper Motor Control Module
SPI	Serial Synchronous Peripheral Interface
T0	16-Bit Timer 0
T1, T2	8-Bit Timers 1 and 2
UART	Universal Asynchronous Receiver Transmitter

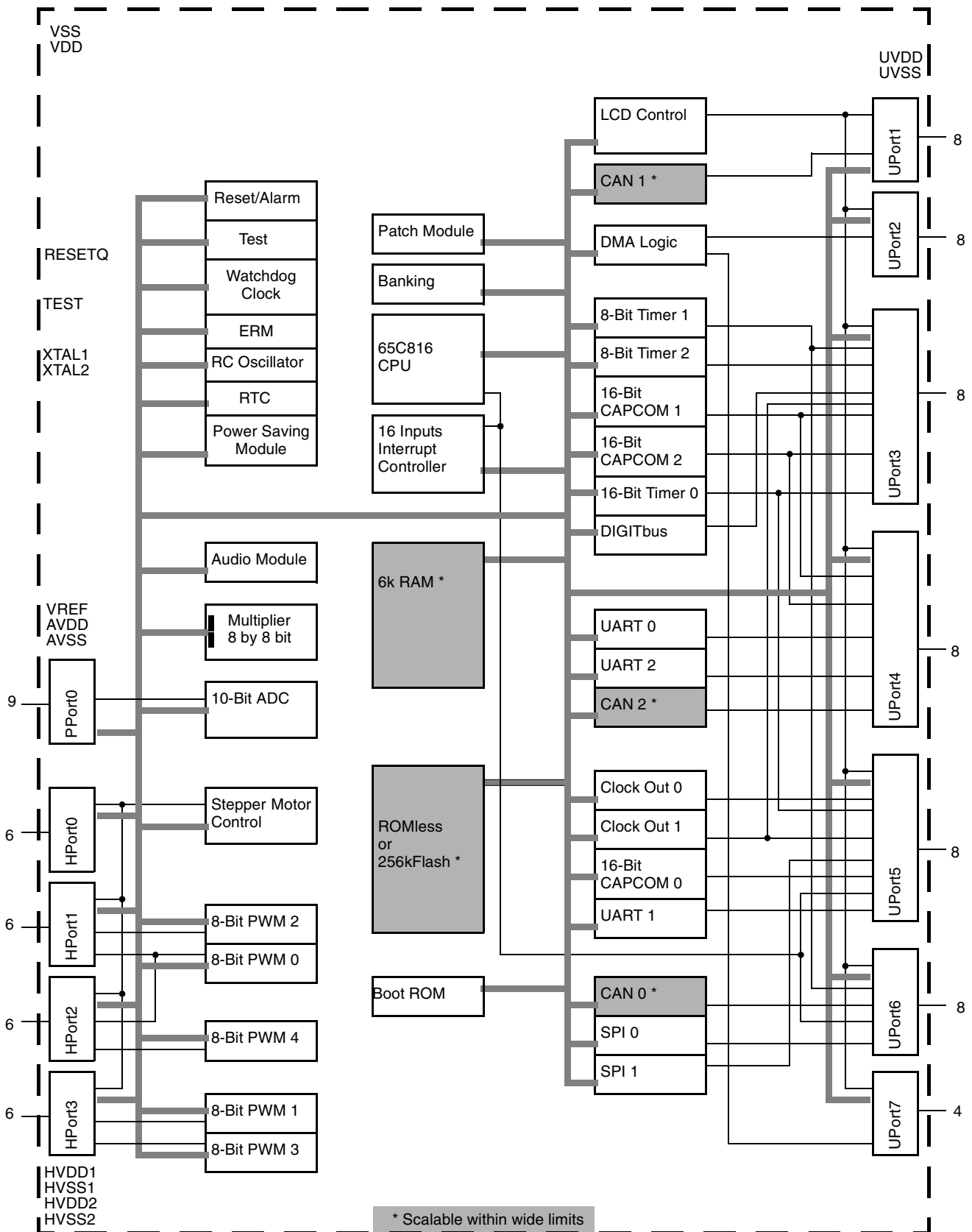
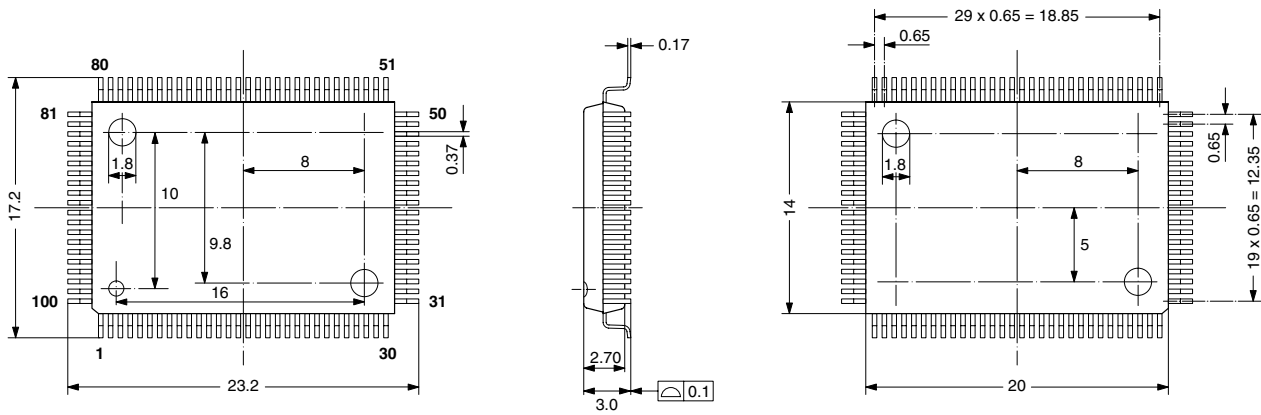


Fig. 1-1: Block diagram of CDC1605F-E/CDC1607F-E



## 2. Package and Pins

### 2.1. Package Outline Dimensions



SPGS0025-2/P100/1F

**Fig. 2-1:** PQFP100 Plastic Quad Flat Pack 100-Pin (Weight approx. 1.61 g)

2.2. Pin Assignment

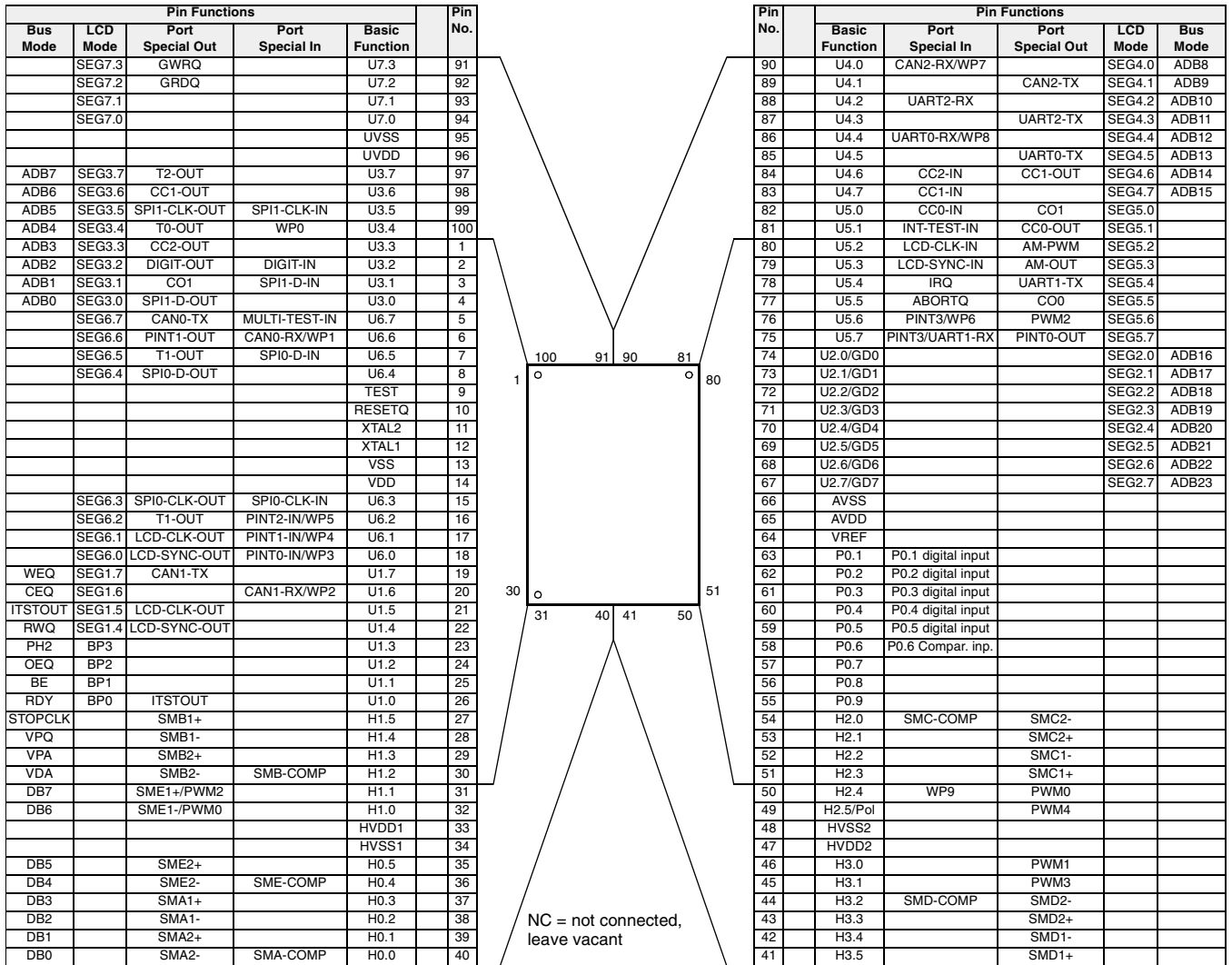


Fig. 2-2: Pin Assignment for PQFP100 Package

2.3. External Components

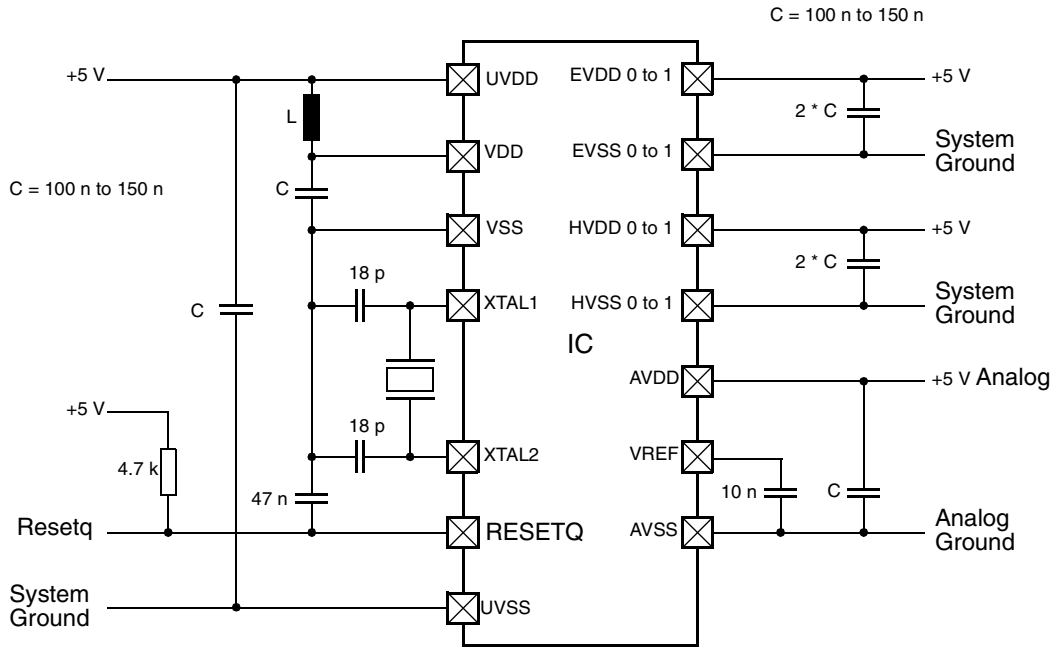


Fig. 2-3: Recommended external supply and quartz connection for low electromagnetic interference (EMI)

To provide effective decoupling and to improve EMC behavior, the small decoupling capacitors must be located as close to the supply pins as possible. The self-inductance of these capacitors and the parasitic inductance and capacitance of the interconnecting traces determine the self-resonant frequency of the decoupling network. A frequency too low will reduce decoupling effectiveness, increase RF emissions and may affect device operation adversely.

XTAL1 and XTAL2 quartz connections are especially sensitive to capacitive coupling from other PC board signals. It is strongly recommended to place quartz and oscillation capacitors as close to the pins as possible and to shield the XTAL1 and XTAL2 traces from other signals by embedding them in a VSS trace.

The RESETQ pin adjacent to XTAL2 should be supplied with a 47 nF capacitor, to prevent fast RESETQ transients from being coupled into XTAL2, to prevent XTAL2 from coupling into RESETQ, and to guarantee a time constant of  $\geq 200 \mu\text{s}$ , sufficient for proper Wake Reset functionality.

### 3. Electrical Characteristics

#### 3.0.1. Absolute Maximum Ratings

**Table 3–1:**  $UV_{SS} = HV_{SS1} = HV_{SS2} = AV_{SS} = 0\text{ V}$

Symbol	Parameter	Pin Name	Min.	Max.	Unit
$V_{SUP}$	Core Supply Voltage Port Supply Voltage Analog Supply Voltage SM Supply Voltage 1 SM Supply Voltage 2	VDD UVDD AVDD HVDD1 HVDD2	-0.3	6.0	V
$\Delta V_{DD}$	Voltage Difference between VDD and AVDD, resp. UVDD	VDD, AVDD UVDD	-0.5	0.5	V
$I_{SUP}$	Core Supply Current Port Supply Current	VDD, VSS UVDD, UVSS	-100	100	mA
$I_{ASUP}$	Analog Supply Current	AVDD, AVSS	-20	20	mA
$I_{HSUP}$	SM Supply Current @ $T_j=105\text{C}$ , Duty Factor = 0.71 <sup>1)</sup>	HVDD1, HVSS1 HVDD2, HVSS2	-380	380	mA
$V_{in}$	Input Voltage	U-Ports, XTAL, RESETQ, TEST	$UV_{SS}-0.5$	$UV_{DD}+0.7$	V
		P0-Ports VREF	$UV_{SS}-0.5$	$AV_{DD}+0.7$	V
		H-Ports	$HV_{SS}-0.5$	$HV_{DD}+0.7$	V
$I_{in}$	Input Current	all Inputs	0	2	mA
$I_o$	Output Current	U-Ports	-5	5	mA
		H-Ports	-60	60	mA
$t_{oshsl}$	Duration of Short Circuit in Port SLOW Mode to UVSS or UVDD	U-Ports except U3.2 in DP Mode		indefinite	s
$T_j$	Junction Temperature under Bias		-45	115	°C
$T_s$	Storage Temperature		-45	125	°C
$P_{max}$	Maximum Power Dissipation			0.8	W

<sup>1)</sup> This condition represents the worst case load with regard to the intended application

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

### 3.0.2. Recommended Operating Conditions

Table 3–2: UVSS = HVSS1= HVSS2 = AVSS = 0 V

Symbol	Parameter	Pin Name	Min.	Typ <sup>1)</sup>	Max.	Unit
V <sub>DD</sub>	Supply Voltage Port Supply Voltage Analog Supply Voltage	VDD UVDD AVDD	4.5	5	5.5	V
HV <sub>DD</sub>	SM Supply Voltage 1 SM Supply Voltage 2	HVDD1 HVDD2	4.75	5	5.25	V
ΔV <sub>DD</sub>	Voltage Difference between VDD and AVDD resp. UVDD	VDD, AVDD UVDD	–0.2		0.2	V
dAV <sub>DD</sub>	AVDD Ripple, Peak to Peak	AVDD			200	mV
f <sub>XTAL</sub>	XTAL Clock Frequency	XTAL1	4		12	MHz
	XTAL Clock Frequency using ERM	XTAL1	4		10	MHz
T <sub>j</sub>	Junction Temperature		–40		110	C
V <sub>il</sub>	Low Input Voltage	U-Ports H-Ports P0-Ports TEST			0.51*V <sub>DD</sub>	V
V <sub>ih</sub>	High Input Voltage	U-Ports H-Ports P0-Ports TEST	0.86*V <sub>DD</sub>			V
RV <sub>il</sub>	Reset Active Input Voltage	RESETQ			0.9	V
WRV <sub>il</sub>	Reset Active Input Voltage during Power Saving Modes and Wake Reset	RESETQ			0.6	V
RV <sub>im</sub>	Reset Inactive and Alarm Active Input Voltage	RESETQ	1.6		2.1	V
RV <sub>ih</sub>	Reset Inactive and Alarm Inactive Input Voltage	RESETQ	2.9			V
WRV <sub>ih</sub>	Reset Inactive during Power Sav- ing Modes	RESETQ	UV <sub>DD</sub> - 0.4V			V
V <sub>REFi</sub>	ADC Reference Input Voltage	VREF	2.56		AV <sub>DD</sub>	V
POV <sub>i</sub>	P0 ADC Input Port Input Voltage	P0-Ports	0		V <sub>REFi</sub>	V
<b>Clock Input from External Generator</b>						
XV <sub>il</sub>	Clock Input Low Voltage	XTAL1			0.2*V <sub>DD</sub>	V
XV <sub>ih</sub>	Clock Input High Voltage	XTAL1	0.8*V <sub>DD</sub>			V
D <sub>XTAL</sub>	Clock Input High-to-Low Ratio	XTAL1	0.45		0.55	
<b><sup>1)</sup> Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).</b>						

**3.0.3. Characteristics differing from Characteristics described in document “CDC16xxF-E Automotive Controller Family User Manual”**

**Table 3–3:**  $UV_{SS} = HV_{SS1} = HV_{SS2} = AV_{SS} = 0\text{ V}$ ,  $4.5\text{ V} < V_{DD} = AV_{DD} = UV_{DD} < 5.5\text{ V}$ ,  $4.75\text{ V} < HV_{DD1} = HV_{DD2} < 5.25\text{ V}$ ,  $T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$ ,  $f_{XTAL} = 10\text{ MHz}$

Symbol	Parameter	Pin Name	Min.	Typ <sup>1)</sup>	Max.	Unit	Test Conditions
<b>Package</b>							
R <sub>thjc</sub>	Thermal Resistance from Junction to Case			25		C/W	
R <sub>thja</sub>	Thermal Resistance from Junction to Ambient			60		C/W	
<b>Supply Currents</b>							CMOS levels on all Inputs, no Loads on Outputs, difference between any two VDDs within $\pm 0.2\text{ V}$
I <sub>DDF</sub>	VDD FAST Mode Supply Current	VDD			60	mA	Flash Read <sup>6)</sup>
					80		Flash Write/Erase <sup>6)</sup>
I <sub>DDS</sub>	VDD SLOW Mode Supply Current	VDD			1.8	mA	all Modules OFF <sup>2)</sup> , <sup>6)</sup>
I <sub>DDD</sub>	VDD DEEP SLOW Mode Supply Current	VDD			1.5		all Modules OFF <sup>2)</sup> , <sup>6)</sup>
I <sub>DDI</sub>	VDD IDLE Mode Supply Current	VDD		50	75	$\mu\text{A}$	$f_{xtal} = 4\text{ MHz}$ <sup>6)</sup>
				60	90	$\mu\text{A}$	$f_{xtal} = 10\text{ MHz}$ <sup>6)</sup>
				70	100	$\mu\text{A}$	internal RC oscill.
I <sub>DDW</sub>	VDD WAKE Mode Supply Current	VDD		30	50	$\mu\text{A}$	
U <sub>IDDa</sub>	UVDD Active Supply Current	UVDD			0.3	mA	no Output Activity, LCD Module ON
A <sub>IDDa</sub>	AVDD Active Supply Current	AVDD		0.2	0.4	mA	ADC ON, ERM OFF
				1	2	mA	ERM ON, $f_{XTAL}=8.4\text{MHz}$
A <sub>DDq</sub>	Quiescent Supply Current	AVDD		1	10	$\mu\text{A}$	ADC and ERM OFF
U <sub>DDq</sub>		UVDD		1	10	$\mu\text{A}$	no Output Activity, LCD Module OFF
E <sub>DDq</sub>		EVDD1 EVDD2		1	10	$\mu\text{A}$	no Output Activity, LCD Module OFF
H <sub>DDq</sub>		Sum of all HVDD1 HVDD2		1	20	$\mu\text{A}$	no Output Activity, SM Module OFF
<sup>1)</sup> <b>Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).</b>							

<sup>2)</sup> Value may be exceeded with unusual Hardware Option setting

<sup>3)</sup> Design value only, the actually observable hysteresis may be lower due to system activity and related supply noise

<sup>4)</sup> When the ERM is active, this time value is increased by  $0.121/f_{XTAL}$ , e.g. 15.125 ns at 8 MHz.

<sup>5)</sup> When the ERM is active, this time value is decreased by  $0.121/f_{XTAL}$ , e.g. 15.125 ns at 8 MHz.

<sup>6)</sup> Measured with external clock. Add 170  $\mu\text{A}$  at 4 MHz, 200  $\mu\text{A}$  at 10 MHz for operation on typical quartz with SR3.XTAL = 0 (Oscillator RUN mode).

### 3.0.4. Recommended Crystal Characteristics

**Table 3–4:**  $UV_{SS} = HV_{SS1} = HV_{SS2} = AV_{SS} = 0\text{ V}$ ,  $4.5\text{ V} < V_{DD} = AV_{DD} = UV_{DD} < 5.5\text{ V}$ ,  
 $4.75\text{ V} < HV_{DD1} = HV_{DD2} < 5.25\text{ V}$ ,  $T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $+105\text{ }^{\circ}\text{C}$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$f_p$	Parallel Resonance Frequency @ $C_L = 12\text{ pF}$	4		12	MHz	
$R_1$	Series Resonance Res. for 50 ms Oscillation Start-Up time @ $C_L = 12\text{ pF}$ @ $f_p = 4\text{ MHz}$			380 320	Ohm	START-UP RUN
	@ $f_p = 6\text{ MHz}$			230 160	Ohm	START-UP RUN
	@ $f_p = 8\text{ MHz}$			150 95	Ohm	START-UP RUN
	@ $f_p = 10\text{ MHz}$			100 60	Ohm	START-UP RUN
$C_{EXT}$	External Oscillation Capacitances for $C_L = 12\text{ pF}$ , connected to VSS		18		pF	

### 4. CPU, RAM, ROM and Banking

MCM PQFP100 Bottom Boot Config.		Alternative	Native
phys.addr.		log.addr.	log.addr.
000000	6K RAM	0000	000000
001800	Reserved		
001900	CAN2-RAM		
001A00	CAN1-RAM		
001B00	CAN0-RAM		
001C00	CAN-Regs		
001D00	Ext. I/O		
001E00	I/O-Reg1	Bank 0	
001F00	I/O-Reg0		Bank 0
002000	Sector 0, upper 8 KB		Bank 0
004000	Sector 1, 8 KB		
006000	Sector 2, 8 KB		
008000	Sector 3, 32 KB	7FFF 8000	
010000	<div style="border: 1px dashed black; padding: 2px;">                     F800                      Boot ROM                 </div> Boot ROM	Bank 1 FFFF	00FFFF
018000	Sector 4, 64 KB  <b>256 KB Flash EEPROM</b>	Bank 2 8000 Bank 3 FFFF	010000 Bank 1
020000	Sector 5, 64 KB	Bank 4 8000 Bank 5 FFFF	01FFFF 020000
028000	Sector 6, 64 KB	Bank 6 8000 Bank 7 FFFF	Bank 2 02FFFF
030000	Sector 6, 64 KB	Bank 8 8000 9FFF	030000
038000			Bank 3
040000	Sector 0, lower 8 KB		03FFFF 040000
042000			Bank 4 041FFF
FFFFF	mirrored Flash EEPROM		

The device contains a 256 KB Flash EEPROM of the AMD Am29F200BT type (bottom boot configuration). This device exhibits electrical byte program and sector erase functions. Refer to the AMD data sheet for details.

Fig. 4-1: Address Map



## 5. Core Logic

### 5.1. Control Register CR

The Control Register CR serves to configure the ways by which certain system resources are accessed during operation. The main purpose is to obtain a variable system configuration during IC test.

Upon each HIGH transition on the RESETQ pin, internal hardware reads data from the address location 00FFF3h and stores it to the CR. The state of the TEST and ESTOPCLK pins at this timepoint specifies which program storage source is accessed for this read:

**Table 5-1:** Control byte source

TEST	Control byte source
0 or NC	internal BOOT ROM (standard for stand-alone operation)
1	external, via multifunction pins in Bus mode (for test purposes only)

The system will thus start up according to the configuration defined in address location 00FFF3h, automatically copied to register CR.

CR		Control Register								
		7	6	5	4	3	2	1	0	
r/w	RESLNG	TSTTOG	x	MFM	TSTROM	IROM	IRAM	ICPU	ROM	
r/w	RESLNG	TSTTOG	EBTRI	MFM	FLASH	IROM	IRAM	ICPU	Emu	
Value of 00FFF3h										Res

**RESLNG**      **Reset Pulse Length**

r/w1:            Pulse length is  $4095/F_{XTAL}$   
 r/w0:            Pulse length is  $16/F_{XTAL}$

This bit specifies the length of the reset pulse which is output at pin RESETQ following an internal reset. If pin TEST is 1 the first reset after power on is short. The following resets are as programmed by RESLNG. If pin TEST is 0, all resets are long.

**TSTTOG**      **TEST Pin Toggle** (Tables 5-2 and 5-3)

This bit is used for test purposes only. If TSTTOG is true in IC active mode, pin TEST can toggle the multifunction pins between Bus mode and normal mode.

**EBTRI**        **Emulator Data Bus Tristate** (Table 5-3)

**MFM**            **Multifunction Pin Mode**  
 (Tables 5-2 and 5-3)

**Table 5-2:** TSTTOG and MFM usage in mask ROM parts

TSTTOG	MFM	TEST pin	Multifunction Pins
0	0	x	Bus mode
1	0	0	Bus mode
		1	normal mode
x	1	x	normal mode

**Table 5-3:** TSTTOG, EBTRI and MFM usage in Flash and EMU parts

TST-TOG	EBTRI	MFM	TEST pin	Multi-function Pins	Emulator Bus Pins
0	x	0	x	Bus mode	Flash mode
1	x	0	0	Bus mode	Flash mode
			1	normal mode	
x	0	1	x	normal mode	Emulator mode
	1				Flash mode

**TSTROM**      **TestROM** (Table 5-4)

**FLASH**        **FLASH EEPROM** (Table 5-5)

**IROM**         **Internal ROM** (Tables 5-4 and 5-5)

**Table 5-4:** TSTROM and IROM usage in mask ROM parts

TSTROM	IROM	selected program storage
1	1	internal ROM
0		internal TestROM
x	0	external via Multifunction pins in Bus mode

**Table 5–5:** FLASH and IROM usage in FLASH and EMU parts

FLASH	IROM	selected program storage
1	1	internal FLASH EEPROM resp. Emulator Bus
0		internal BOOT ROM
x	0	external via Multifunction pins in Bus mode

**IRAM Internal RAM**  
 r/w1: Enable internal RAM.  
 r/w0: Disable internal RAM.

**ICPU Internal CPU**  
 r/w1: Enable internal CPU.  
 r/w0: Disable internal CPU.

**Table 5–6:** Some commonly used settings for address location 00FFF3h. A copy is automatically transferred to the CR during IC start-up.

Code	TEST Pin	Operation Mode
FFh	0	Stand-alone with internal ROM or Flash
ABh	1	External program storage connected to multifunction pins in Bus mode
DFh	0	Emulator mode (CPGA177 package)

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## 6. Hardware Options

### 6.1. Functional Description

Hardware Options are available in several areas to adapt the IC function to the host system requirements:

- clock signal selection for most of the peripheral modules from  $f_{osc}$  to  $f_{osc}/2^{17}$  plus some internal signals. (see table in Chapter Hardware Options of document “CDC16xxF-E Automotive Controller Family User Manual”.)
- interrupt source selection for interrupt inputs 5, 6, 7, 13, 14 and 15
- Special Out signal selection for some U and H-ports
- Rx/Tx polarity selection for SPI and UART modules
- U-port Port Slow Mode selection

Hardware Option setting requires two steps:

1. selection is done by programming dedicated address locations with the desired options' code
2. activation is done by a read access to these dedicated address locations at least once after each reset.

Address locations 00FFB8h through 00FFBFh do not allow random setting. Their respective Hardware Options are hard-wired and can only be altered by changing a production mask for this IC. By default, the Port Slow Option is set for all U-Ports, with the exception of U1.0 to U1.3 (Port Fast Option is set). The Watchdog and Clock Monitor are activated via software by default.

Future mask ROM derivatives of this IC will not require (but will tolerate) activation of option settings by read accesses, as the ROM as well as the options will be hard-wired. Instead, the manufacturer will automatically process the setting of the dedicated address locations, as given in the ROM code file, to set the required mask changes.

To ensure compatible option settings in this IC and mask ROM derivatives when run with the same ROM code, it is recommended to always read locations 00FFA0h through 00FFC3h directly after reset. Please note that the non-programmable locations 00FFB8h through 00FFBFh may not be compatible within this IC and the mask ROM derivative.

## 7. Differences

This chapter describes differences of this document to predecessor document "CDC1607F-E Automotive Controller Specification", Feb. 17, 2003, 6251-606-1A1.

#	Section	Description
1	Introduction	Table 1-1: "CDC16xxF Family Feature List" on page 3: Name and features of "Example E-Family" changed into "CDC1631F-E", Multiplier, 8 by 8 bit added.
		Fig. 1-1: "Block diagram of CDC1605F-E/CDC1607F-E" on page 8: Multiplier, 8 by 8 bit added
2	External Components	Value of C at RESETQ changed from 47 $\mu$ to 47 n, value of C at VREF changed from 10 $\mu$ to 10 n and text added.
3	Core Logic	Table 5-1: "Control byte source" on page 17: Updated / minimized
4	CPU, RAM, ROM and Banking	Fig. 4-1: "Address Map" on page 16: Layout format corrected.
5	Differences	New Chapter



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## 8. Data Sheet History

1. Advance Information: "CDC1607F-E Automotive Controller Specification", Feb. 17, 2003, 6251-608-1AI. First release of the advance information. Originally created for the HW version CDC1607F-E1.

2. Advance Information: "CDC1607F-E Automotive Controller Specification", March 31, 2003, 6251-608-2AI. Second release of the advance information. Originally created for the HW version CDC1607F-E2.

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