



# CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer

## CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer

## CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

### General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to 15V<sub>p-p</sub> can be achieved by digital signal amplitudes of 3–15V. For example, if  $V_{DD} = 5V$ ,  $V_{SS} = 0V$  and  $V_{EE} = -5V$ , analog signals from  $-5V$  to  $+5V$  can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full  $V_{DD} - V_{SS}$  and  $V_{DD} - V_{EE}$  supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and

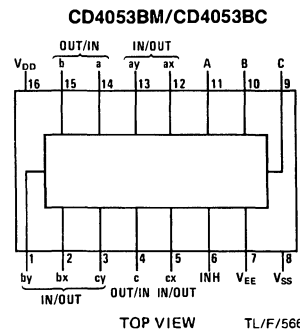
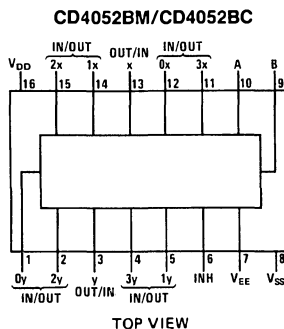
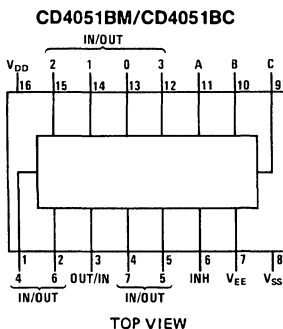
an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

### Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to 15V<sub>p-p</sub>
- Low "ON" resistance: 80Ω (typ.) over entire 15V<sub>p-p</sub> signal-input range for  $V_{DD} - V_{EE} = 15V$
- High "OFF" resistance: channel leakage of  $\pm 10$  pA (typ.) at  $V_{DD} - V_{EE} = 10V$
- Logic level conversion for digital addressing signals of 3–15V ( $V_{DD} - V_{SS} = 3-15V$ ) to switch analog signals to 15 V<sub>p-p</sub> ( $V_{DD} - V_{EE} = 15V$ )
- Matched switch characteristics:  $\Delta R_{ON} = 5\Omega$  (typ.) for  $V_{DD} - V_{EE} = 15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1  $\mu W$  (typ.) at  $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10V$
- Binary address decoding on chip

### Connection Diagrams

#### Dual-In-Line Packages



Order Number CD4051B\*, CD4052B\*, or CD4053B\*

\*Please look into Section 8, Appendix D for availability of various package types.

See the CMOS Logic Databook for Complete Specifications

CD4051BM/CD4051BC/CD4052BM/CD4052BC/CD4053BM/CD4053BC