

CD4031BM/CD4031BC 64-Stage Static Shift Register

General Description

The CD4031BM/CD4031BC is an integrated, complementary MOS (CMOS), 64-stage, fully static shift register. Two data inputs, DATA IN and RECIRCULATE IN, and a MODE CONTROL input are provided. Data at the DATA input (when MODE CONTROL is low) or data at the RECIRCULATE input (when MODE CONTROL is high), which meets the setup and hold time requirements, is entered into the first stage of the register and is shifted one stage at each positive transition of the CLOCK.

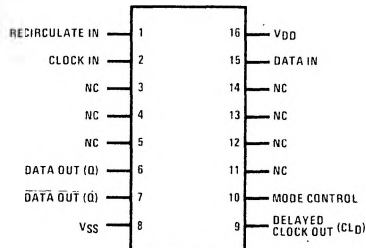
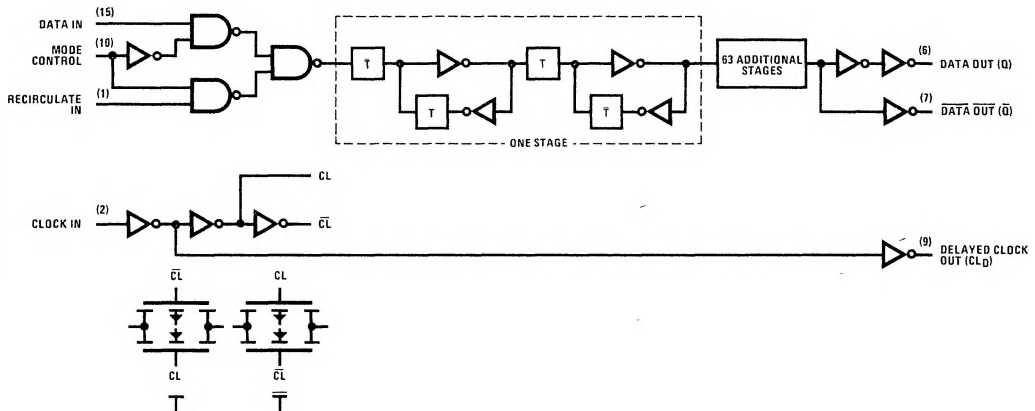
Data output is available in both true and complement forms from the 64th stage. Both the DATA OUT (Q) and DATA OUT (Q̄) outputs are fully buffered.

The CLOCK input of the CD4031BM/CD4031BC is fully buffered, and present only a standard input load capacitance. However, a DELAYED CLOCK OUTPUT (CL_D) has been provided to allow reduced clock drive fan-out and transition time requirements when cascading packages.

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Fully static operation DC to 8 MHz
V_{DD} = 10 V (typ.)
- Fully buffered clock input 5 pF (typ.)
input capacitance
- Single phase clocking requirements
- Delayed clock output for reduced clock drive requirements
- Fully buffered outputs
- High current sinking capability 1.6 mA
Q output @ V_{DD} = 5 V and 25°C

Logic and Connection Diagrams



Absolute Maximum Ratings

(Notes 1 and 2)

V _{DD} Supply Voltage	-0.5 V to +18 V
V _{IN} Input Voltage	-0.5 V to V _{DD} + 0.5 V
T _S Storage Temperature Range	-65°C to +150°C
P _D Package Dissipation	500 mW
T _L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V _{DD} Supply Voltage	+3 V to +15 V
V _{IN} Input Voltage	0 V to V _{DD}
T _A Operating Temperature Range	-55°C to +125°C
	CD4031BM
	CD4031BC
	-40°C to +85°C

DC Electrical Characteristics (Note 2) CD4031BM




PARAMETER	CONDITIONS	-55°C		+25°C			+125°C		UNITS	
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
I _{DD} Quiescent Device Current	V _{DD} = 5 V		5		0.01	5		150	μA	
	V _{DD} = 10 V		10		0.01	10		300	μA	
	V _{DD} = 15 V		20		0.02	20		600	μA	
V _{OL} Low Level Output Voltage	V _{DD} = 5 V } V _{IH} = V _{DD} , V _{IL} = 0 V, I _{OL} < 1 μA		0.05		0	0.05		0.05	V	
			0.05		0	0.05		0.05	V	
			0.05		0	0.05		0.05	V	
V _{OH} High Level Output Voltage	V _{DD} = 5 V } V _{IH} = V _{DD} , V _{IL} = 0 V, I _{OL} < 1 μA		4.95		4.95	5		4.95	V	
			9.95		9.95	10		9.95	V	
			14.95		14.95	15		14.95	V	
V _{IL} Low Level Input Voltage	V _{DD} = 5 V, V _O = 0.5 V or 4.5 V } I _{OL} < 1 μA		1.5		2.25	1.5		1.5	V	
			3.0		4.5	3.0		3.0	V	
			4.0		6.75	4.0		4.0	V	
V _{IH} High Level Input Voltage	V _{DD} = 5 V, V _O = 0.5 V or 4.5 V } I _{OL} < 1 μA		3.5		3.5	2.75		3.5	V	
			7.0		7.0	5.5		7.0	V	
			11.0		11.0	8.25		11.0	V	
I _{OL} Low Level Output Current, Q Output	V _{DD} = 5 V, V _O = 0.4 V } V _{IH} = V _{DD}		2.3		1.9	3.8		1.3	mA	
		V _{DD} = 10 V, V _O = 0.5 V } V _{IL} = 0 V		5.1		4.2	8.4		2.8	mA
			V _{DD} = 15 V, V _O = 1.5 V		10.5		8.8	17		6.1
I _{OL} Low Level Output Current, Q and CL _D Outputs	V _{DD} = 5 V, V _O = 0.4 V } V _{IH} = V _{DD}		0.64		0.51	0.88		0.36	mA	
		V _{DD} = 10 V, V _O = 0.5 V } V _{IL} = 0 V		1.6		1.3	2.25		0.9	mA
			V _{DD} = 15 V, V _O = 1.5 V		4.2		3.4	8.8		2.4
I _{OH} High Level Output Current, All Outputs	V _{DD} = 5 V, V _O = 4.6 V } V _{IH} = V _{DD}		-0.64		-0.51	-0.88		-0.36	mA	
		V _{DD} = 10 V, V _O = 9.5 V } V _{IL} = 0 V		-1.6		-1.3	-2.25		-0.9	mA
			V _{DD} = 15 V, V _O = 13.5 V		-4.2		-3.4	-8.8		-2.4
I _{IN} Input Current	V _{DD} = 15 V, V _{IN} = 0 V		-0.1		-10 ⁻⁵	-0.1		-1.0	μA	
		V _{DD} = 15 V, V _{IN} = 15 V		0.1		10 ⁻⁵	0.1		1.0	μA



Truth Tables

MODE CONTROL (data selection)

MODE CONTROL	DATA IN	RECIRCULATE IN	DATA INTO FIRST STAGE
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

EACH STAGE

D _n	CL	Q _n
0		0
1		1
X		NC

X = irrelevant
 NC = no change
 = Low to High level transition
 = High to Low level transition

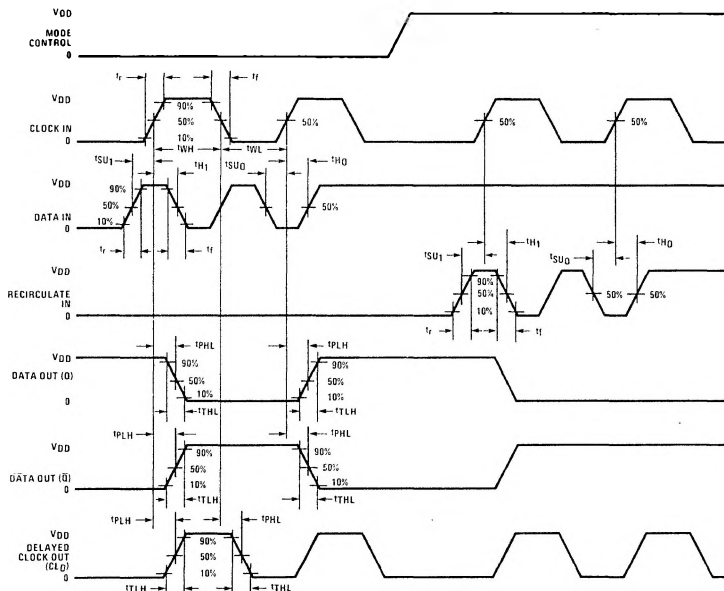
DC Electrical Characteristics (Note 2) CD4031BC

PARAMETER	CONDITIONS	-40°C		+25°C			+85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		20		0.01	20		150	μA
	$V_{DD} = 10V$		40		0.01	40		300	μA
	$V_{DD} = 15V$		80		0.02	80		600	μA
V_{OL} Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
	$V_{DD} = 10V$	$V_{IH} = V_{DD}, V_{IL} = 0V, I_{OL} < 1\mu A$	0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD} = 5V$		4.95		4.95	5		4.95	V
	$V_{DD} = 10V$	9.95		9.95	10		9.95	V	
	$V_{DD} = 15V$	14.95		14.95	15		14.95	V	
V_{IL} Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	$ I_{OL} < 1\mu A$	3.0		4.5	3.0		3.0	V
	$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		3.5		3.5	2.75		3.5	V
	$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0	5.5		7.0	V	
	$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0	V	
I_{OL} Low Level Output Current, Q Output	$V_{DD} = 5V, V_O = 0.4V$		1.8		1.6	3.8		1.3	mA
	$V_{DD} = 10V, V_O = 0.5V$	$V_{IH} = V_{DD}$ $V_{IL} = 0V$	4.0		3.5	8.4		2.8	mA
	$V_{DD} = 15V, V_O = 1.5V$		8.7		7.5	17		6.1	mA
I_{OL} Low Level Output Current, Q and CL_D Outputs	$V_{DD} = 5V, V_O = 0.4V$		0.52		0.44	0.88		0.36	mA
	$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9	mA	
	$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4	mA	
I_{OH} High Level Output Current, All Outputs	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.44	-0.88		-0.36	mA	
	$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9	mA	
	$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	-8.8		-2.4	mA	
I_{IN} Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		-10^{-5}	-0.3		-1.0	μA
	$V_{DD} = 15V, V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Switching Time Waveforms



AC Electrical Characteristics $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}$, Input $t_r = t_f = 20\text{ ns}$, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} , t_{PLH} Propagation Delay Time, Clock to Q and \bar{Q}	$V_{CC} = 5\text{ V}$		300	600	ns
	$V_{CC} = 10\text{ V}$		125	250	ns
	$V_{CC} = 15\text{ V}$		100	200	ns
t_{PHL} , t_{PLH} Propagation Delay Time, Clock to CL_D	$V_{CC} = 5\text{ V}$		125	250	ns
	$V_{CC} = 10\text{ V}$		60	125	ns
	$V_{CC} = 15\text{ V}$		50	100	ns
t_{THL} , t_{TLH} Output Transition Time, All Outputs	$V_{CC} = 5\text{ V}$		100	200	ns
	$V_{CC} = 10\text{ V}$		50	100	ns
	$V_{CC} = 15\text{ V}$		40	80	ns
t_{SU0} Minimum Data Setup Time, DATA IN or RECIRCULATE IN to Clock t_{SU1}	$V_{CC} = 5\text{ V}$		100	200	ns
	$V_{CC} = 10\text{ V}$		50	100	ns
	$V_{CC} = 15\text{ V}$		40	80	ns
t_{H0} Minimum Data Hold Time, Clock to DATA IN or RECIRCULATE IN t_{H1}	$V_{CC} = 5\text{ V}$		100	200	ns
	$V_{CC} = 10\text{ V}$		50	100	ns
	$V_{CC} = 15\text{ V}$		40	80	ns
t_{WL} , t_{WH} Minimum Clock Pulse Width	$V_{CC} = 5\text{ V}$		150	300	ns
	$V_{CC} = 10\text{ V}$		60	125	ns
	$V_{CC} = 15\text{ V}$		50	100	ns
f_{CL} Maximum Clock Frequency	$V_{CC} = 5\text{ V}$	1.6	3.2		MHz
	$V_{CC} = 10\text{ V}$	4.0	8.0		MHz
	$V_{CC} = 15\text{ V}$	5.0	10		MHz
t_{RCL} , t_{FCL} Maximum Clock Input Rise and Fall Times (Note 3)	$V_{CC} = 5\text{ V}$	15			μs
	$V_{CC} = 10\text{ V}$	10			μs
	$V_{CC} = 15\text{ V}$	5			μs
C_{IN} Input Capacitance	Any Input		5	7.5	pF

Note 3: When clocking cascaded packages in parallel, one should insure that: $t_r CL \leq 2(t_{PD} - t_H)$ where: t_{PD} = the propagation delay of the driving stage and t_H = the hold time of the driven stage.

Block Diagram

cascading packages using DELAYED CLOCK (CL_D) output

