

November 1994

Features

- High-Voltage Type (20V Rating)
- Retriggerable/Resettable Capability
- Trigger and Reset Propagation Delays Independent of R_X , C_X
- Triggering From Leading or Trailing Edge
- Q and \bar{Q} Buffered Outputs Available
- Separate Resets
- Wide Range of Output-Pulse Widths
- Schmitt-Trigger Input Allows Unlimited Rise and Fall Times On +TR and -TR Inputs
- 100% Tested For Maximum Quiescent Current at 20V
- Maximum Input Current of $1\mu\text{A}$ at 18V Over Full Package-Temperature Range:
 - 100nA at 18V and +25°C
- Noise Margin (Full Package-Temperature Range):
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's

Applications

- Pulse Delay and Timing
- Pulse Shaping

Description

CD14538BMS dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and \bar{Q} terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X . Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to VSS. An unused -TR input should be tied to VDD. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to VDD. However, if an entire section of the CD14538BMS is not used, its inputs must be tied to either VDD or VSS. See Table 1.

In normal operation the circuit retriggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, \bar{Q} is connected to -TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (-TR) is used. The time period (T) for this multivibrator can be calculated by: $T = R_X C_X$.

The minimum value of external resistance, R_X is $4K\Omega$. The minimum and maximum values of external capacitance, C_X , are 0pF and $100\mu\text{F}$, respectively.

The CD14538BMS is interchangeable with type MC14538 and is similar to and pin-compatible with the CD4098B* and CD4538B**.

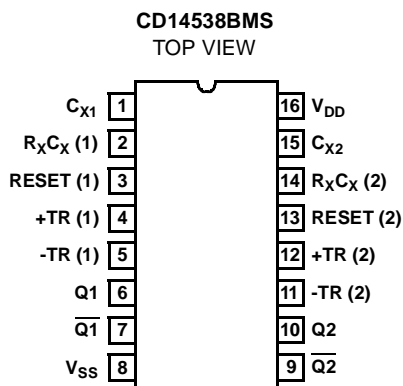
* $T = 0.5 R_X C_X$ for $C_X \geq 1000\text{pF}$.

* $T = R_X C_X$; $C_X \text{ min} = 5000\text{pF}$.

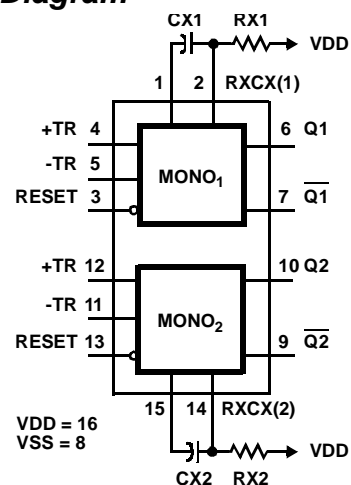
The CD14538BMS is supplied in these 16-lead outline packages:

- Braze Seal DIP H4X
- Frit Seal DIP H1L
- Ceramic Flatpack H6W

Pinout



Functional Diagram



Specifications CD14538BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) (Voltage Referenced to VSS Terminals)	-0.5V to +20V
Input Voltage Range, All Inputs	-0.5V to VDD +0.5V
DC Input Current, Any One Input	±10mA
Operating Temperature Range	-55°C to +125°C
Package Types D, F, K, H	
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (During Soldering)	+265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum	

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W
Maximum Package Power Dissipation (PD) at +125°C		
For TA = -55°C to +100°C (Package Type D, F, K)	500mW	
For TA = +100°C to +125°C (Package Type D, F, K)	Derate	
	Linearity at 12mW/°C to 200mW	
Device Dissipation per Output Transistor	100mW	
For TA = Full Package Temperature Range (All Package Types)		
Junction Temperature	+175°C	

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	μA
				2	+125°C	-	1000	μA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	μA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 2. Go/No Go test with limits applied to inputs 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (Note 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay +TR or -TR to Q or \bar{Q}	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay Reset to Q or \bar{Q}	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	μA
				+125°C	-	150	μA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	300	μA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	μA
				+125°C	-	600	μA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL1	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V

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TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay +TR OR -TR to Q or \bar{Q}	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	220	ns
Propagation Delay Reset to Q or \bar{Q}	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	250	ns
		VDD = 15V	1, 2, 3	+25°C	-	190	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Output Pulse Width Q or \bar{Q} $C_X = .002\mu\text{F}$, $R_X = 100\text{K}$	TW	VDD = 5V	1, 2, 3	+25°C	-	230	μs
		VDD = 10V	1, 2, 3	+25°C	-	232	μs
		VDD = 15V	1, 2, 3	+25°C	-	234	μs
Output Pulse Width $C_X = 0.1\mu\text{F}$ $R_X = 100\text{K}$	TW	VDD = 5V	1, 2, 3	+25°C	-	10.5	ms
		VDD = 10V	1, 2, 3	+25°C	-	10.6	ms
		VDD = 15V	1, 2, 3	+25°C	-	10.6	ms
Output Pulse Width $C_X = 10\mu\text{F}$ $R_X = 100\text{K}$	TW	VDD = 5V	1, 2, 3	+25°C	-	1.06	s
		VDD = 10V	1, 2, 3	+25°C	-	1.06	s
		VDD = 15V	1, 2, 3	+25°C	-	1.07	s
Minimum Retrigger Time	TRR	VDD = 5V	1, 2, 3	+25°C	0	-	ns
		VDD = 10V	1, 2, 3	+25°C	0	-	ns
		VDD = 15V	1, 2, 3	+25°C	0	-	ns
Minimum Input Pulse Width +TR, -TR, or Reset	TW	VDD = 5V	1, 2, 3	+25°C	-	140	ns
		VDD = 10V	1, 2, 3	+25°C	-	80	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

- All voltages referenced to device GND.
- The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
- CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10 μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10 μA	1, 4	+25°C	-	± 1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10 μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10 μA	1, 4	+25°C	-	± 1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

- NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25°C limit. 4. Read and Record

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TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A, RONDEL10
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	
Group A	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas
	Subgroup B-6	Sample 5005	1, 7, 9
Group D	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	6, 7, 9, 10	1, 3 - 5, 8, 11 - 13, 15	2, 14, 16			
Static Burn-In 2 (Note 1)	6, 7, 9, 10	1, 8, 15	2 - 5, 11 - 13, 14, 16			
Dynamic Burn-In (Note 1)	-	1, 4, 8, 12, 15	2, 14, 16	6, 7, 9, 10	5, 11	3, 13
Irradiation (Note 2)	2, 6, 7, 9, 10, 14	1, 8, 15	3 - 5, 11 - 13, 16			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

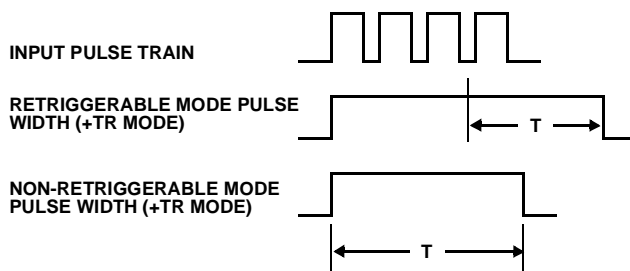
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TABLE 9. FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	VDD TO TERM #		VSS TO TERM #		INPUT PULSE TO TERM #		OTHER CONNECTIONS	
	MONO1	MONO2	MONO1	MONO2	MONO1	MONO2	MONO1	MONO2
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-Retriggerable	3	13			4	12	5 - 7	11 - 9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-Retriggerable	3	13			5	11	4 - 6	12 - 10

NOTE:

1. A triggerable one-shot multivibrator has an output pulse width which is extended one full time period (T) after application of the last trigger pulse.
2. A non-triggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.



Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit or with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when C_X is ≥ 0.5 microfarad, a protection diode with a 1-ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Figure 1.

An alternate protection method is shown in Figure 2, where a 51-ohm current-limiting resistor is inserted in series with C_X . Note that a small pulse width decrease will occur however, and R_X must be appropriately increased to obtain the originally desired pulse width.

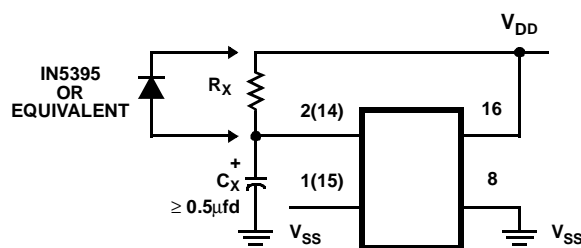


FIGURE 1. RAPID POWER-DOWN PROTECTION CIRCUIT

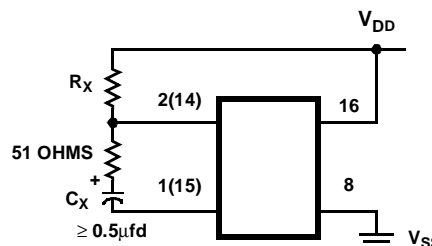


FIGURE 2. ALTERNATE RAPID POWER-DOWN PROTECTION CIRCUIT

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Logic Diagram

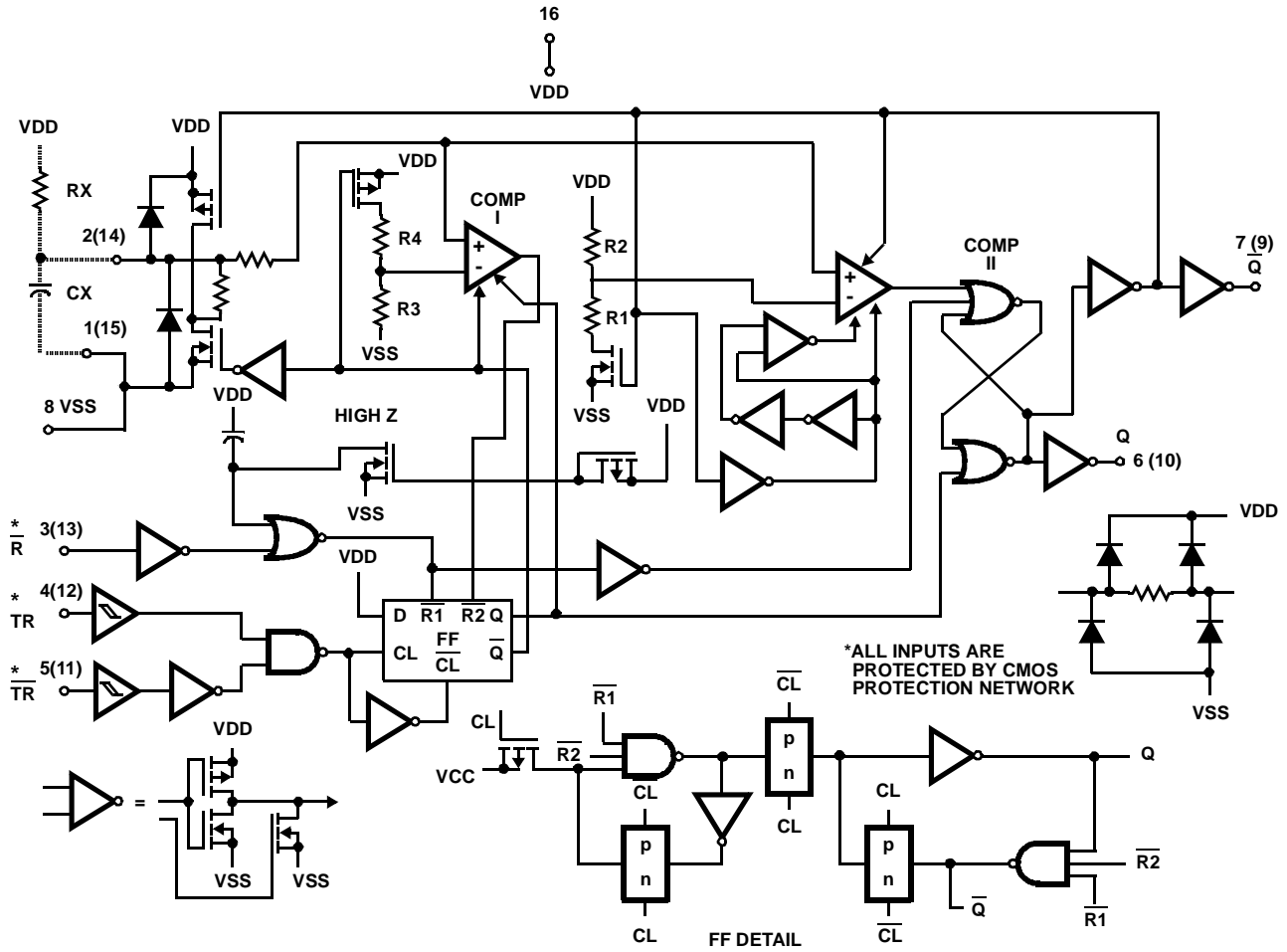


FIGURE 3. 1/2 OF DEVICE SHOWN

Typical Performance Characteristics

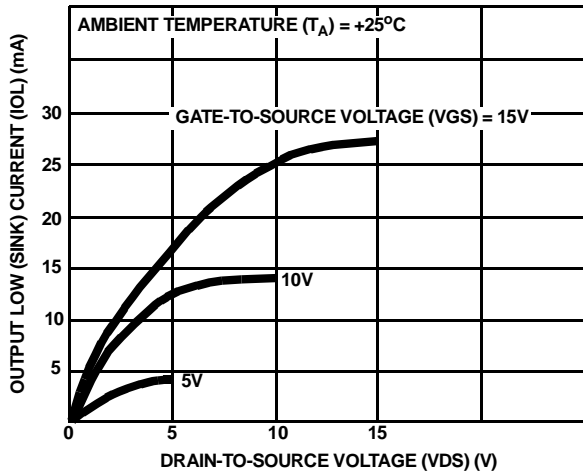


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

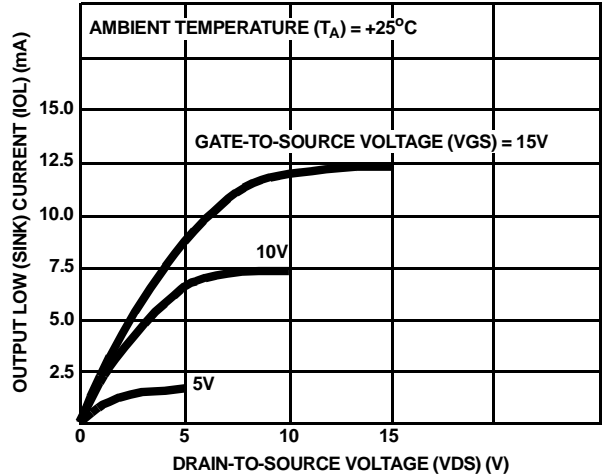


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

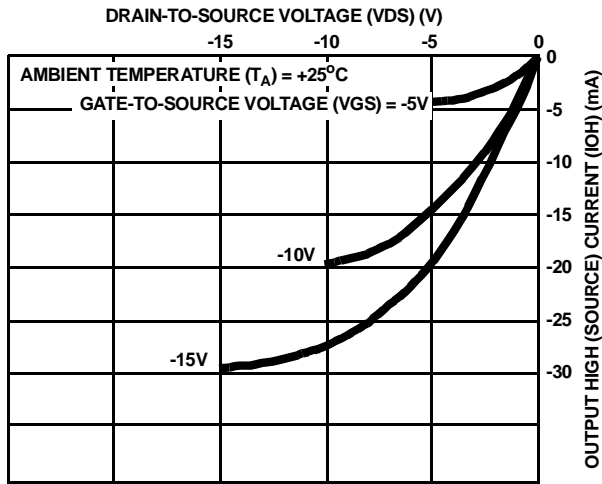


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

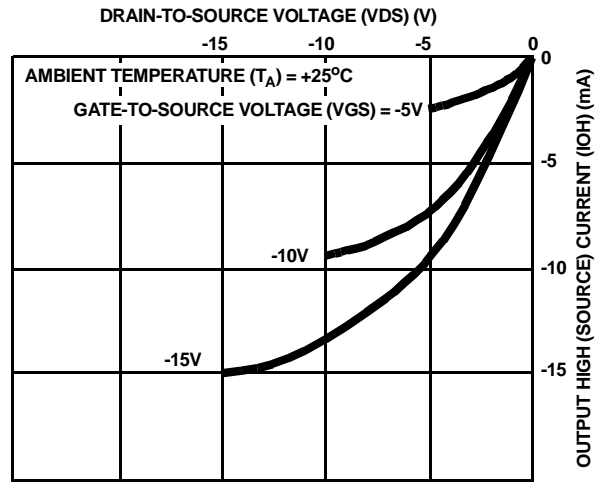


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

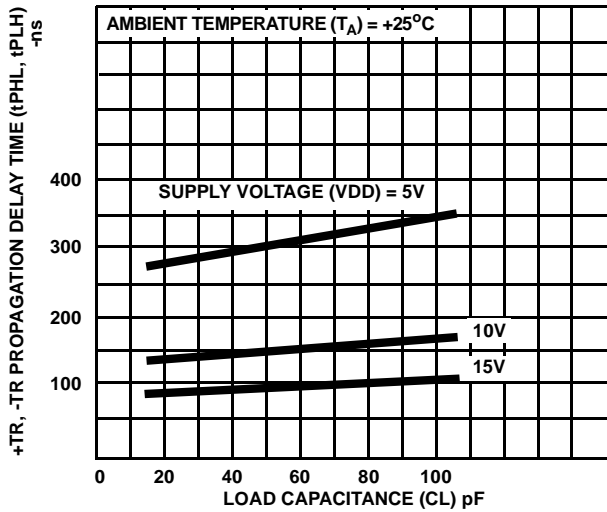


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (+TR OR -TR TO Q OR Q̄)

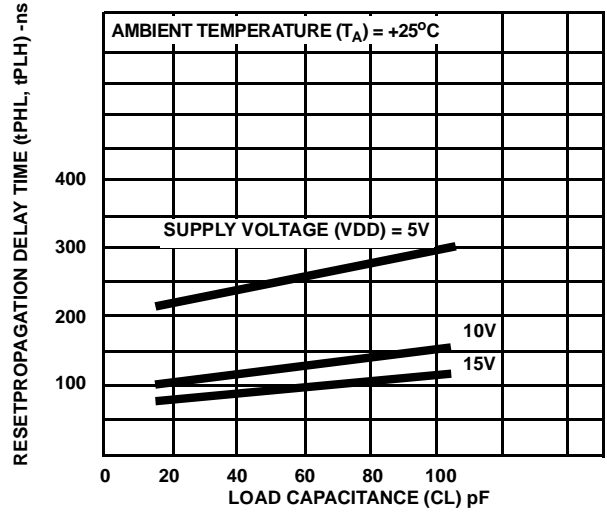


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (RESET TO Q OR Q̄)

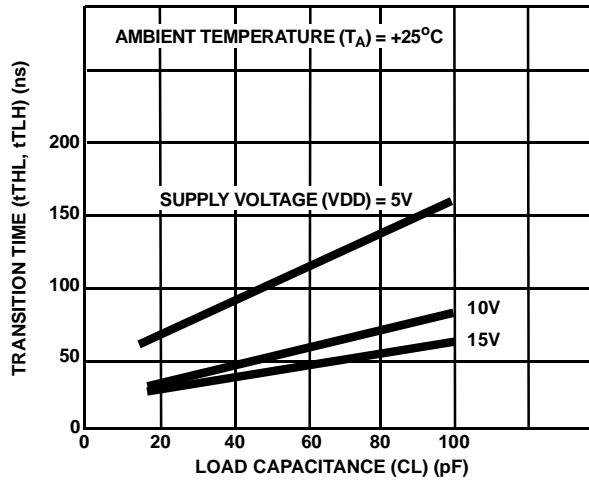


FIGURE 10. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

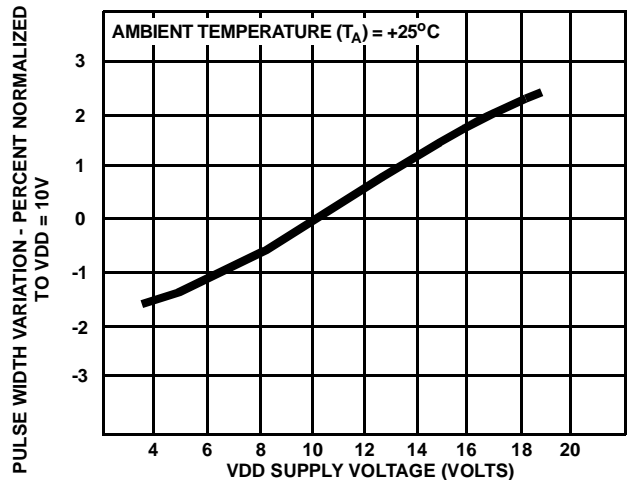


FIGURE 11. TYPICAL PULSE-WIDTH VARIATION AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Characteristics (Continued)

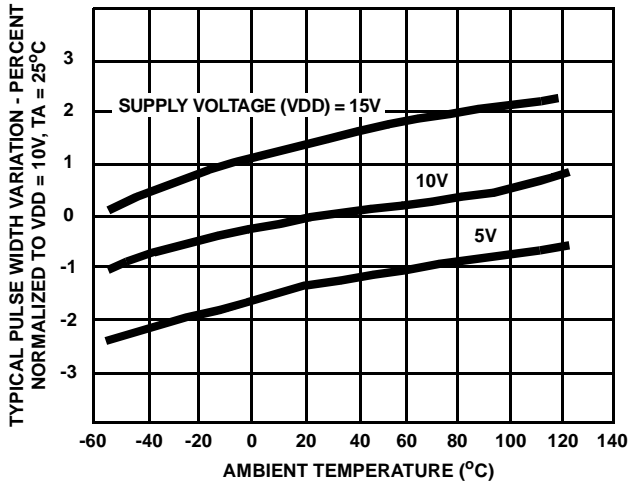


FIGURE 12. TYPICAL PULSE-WIDTH VARIATION AS A FUNCTION OF TEMPERATURE (RX = 100 KΩ, CX = 0.1μF)

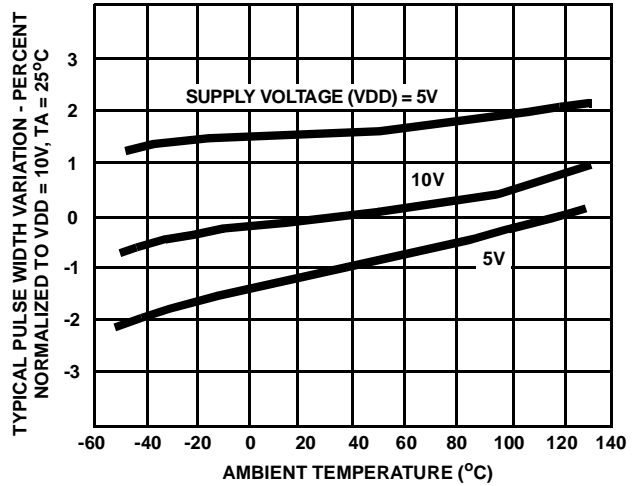


FIGURE 13. TYPICAL PULSE-WIDTH VARIATION AS A FUNCTION OF TEMPERATURE (RX = 100 KΩ, CX = 2000pF)

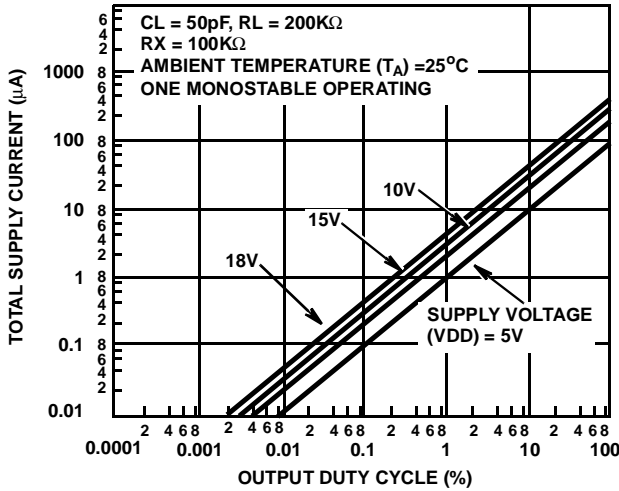


FIGURE 14. TYPICAL TOTAL SUPPLY CURRENT AS A FUNCTION OF OUTPUT DUTY CYCLE

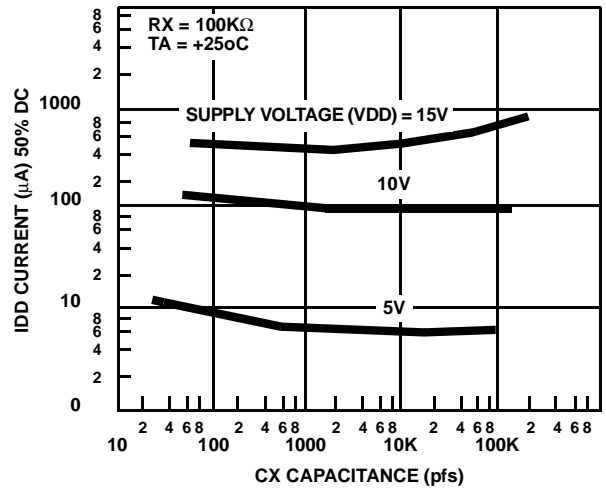
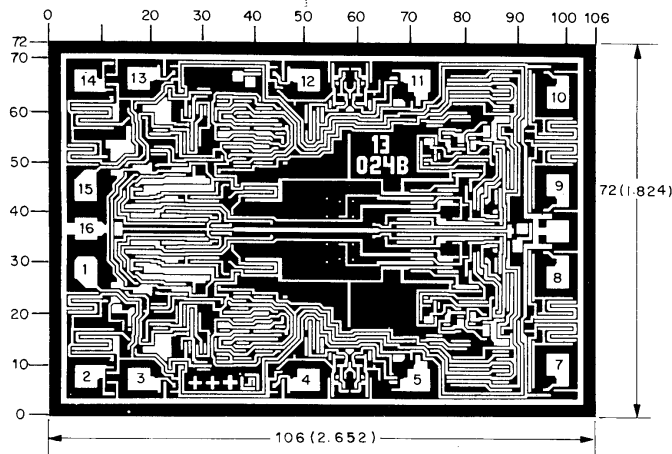


FIGURE 15. TYPICAL TOTAL SUPPLY CURRENT AS A FUNCTION OF LOAD CAPACITANCE

Chip Dimension and Pad Layout



METALLIZATION: Thickness: 11kÅ - 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)