Design Manual

NEC

CB-9 Family
VX/VM Type

0.35 μm CMOS Cell-Based IC

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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MAJOR REVISIONS IN THIS EDITION

Page	Description
Throughout	• Change of family name from "CB-C9 Family VX/VM Type" to "CB-9 Family VX/VM Type". • Modification of glossary entry (change from "mega-function" to "core")
pp. 50, 51	**Table 3-6. DC Characteristics (V_{DD} = 3.3 ± 0.3 V, T_A = –40 to +85°C)** • Addition of TTL 5 V tolerant buffer (18 mA type, 24 mA type) specification values to Low-level output current and High-level output current.
p. 65	**Table 4-1. Power Consumption by Each Input Buffer** • Addition of block type
p. 66	**Table 4-2. Power Consumption by Output Buffers** • Addition of PCI interface block specification values
pp. 69 to 71	**4.3.4 Detailed estimation of internal circuit power consumption** • Modification of **Power consumption in internal cells**
p. 113	**Table 4-14. SSO Pin Conversion Coefficients** • Addition of 3.0 mA type specification values to TTL 5 V tolerant buffer (low noise). • Addition of 3.0 mA type and 6.0 mA type specification values to 5 V buffer (low noise).
p. 126, 127	**5.1.2 Core control pins** • Deletion of description about functional cells that cause no problems even during Hi-Z input from **(2) Use of control pins (b) Countermeasures against high-impedance output**. • Modification of **Figure 5-4. Example of Countermeasure against High-Impedance Output**
p. 153 in the previous edition	Deletion of **6.3.3 "Use prohibited" status of flip-flops**
pp. 167, 168	**6.6.2 Prevention of High impedance** • Modification of description about cautions on bus line configuration. • Modification of **Figure 6-22. Configuration Examples of Circuits for Preventing High Impedance of Internal Bus**
p. 168	Addition of **6.6.4 Cautions regarding occurrence of overcurrent at power application**
pp. 195 to 218 in the previous edition	Deletion of **CHAPTER 8 TEST PATTERN DESIGN**
p. 212	**9.5.1 Signal standard for PCI local bus** • Addition of description about placement of additional power supply.
pp. 241 to 244 in the previous edition	Deletion of **CHAPTER 11 CREATION OF DEBUGGER**

The mark ★ shows major revised points.

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PREFACE

This manual describes various restrictions and cautions concerning LSI design using NEC's CB-9 Family (VX/VM Type) of high-speed, highly integrated CMOS cell-based ICs.

LSI designers should read this manual carefully to help ensure smooth progress in LSI design.

Be sure to remain within the specifications described in this manual (including general items, cautions, and restrictions). Failure to do so may result in poor quality, poor performance, or operation faults in LSI products.

Related documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- **CB-9 Family VX/VM Type**
  - CB-9 Family VX/VM Type Design Manual (This manual)
  - CB-9 Family VX/VM Type Block Library (CMOS 3.3 V) (A12793E)
  - CB-9 Family VX Type Block Library (CMOS 2.0 V) (A12794E)
  - CB-9 Family VX/VM Type (TTL 3.3 V) Block Library (A14710E)
  - CB-9 Family VX/VM Type Memory Macro (Compiled Type) Design Manual (A12982E)
  - CB-9 Family VX/VM Type Memory Macro (Fixed Type) Design Manual (A13899E)
  - CB-9 Family VX/VM Type Analog Macro (High-Speed D/A Converter) Design Manual (A13820E)
  - CB-9 Family VX/VM Type Analog Macro (PLL) Design Manual (A13947E)
  - CB-9 Family VX/VM Type Analog Macro (General-Purpose A/D, D/A Converter) Design Manual (A14021E)
  - CB-9 Family VX/VM Type CPU, Peripheral Design Manual (A14304E)
  - CB-9 Family VX/VM Type NX16550L Core User's Manual (A13258E)
  - CB-9 Family VX/VM Type Core Library CPU Core, Memory Controller Design Manual (A13195E)

- **OPENCAD™**
  - Design For Test User's Manual (A14357E)

To obtain the latest documents when designing, contact an NEC sales office or a distributor.

CONTENTS

CHAPTER 1 GENERAL **19**
- **1.1 Features** **19**
  - 1.1.1 Features of VX/VM types 20
- **1.2 Internal Configuration of Cell-Based ICs** **23**
  - 1.2.1 Chip configuration 23
  - 1.2.2 Chip layout 24
- **1.3 On-chip Transistor Configuration** **25**
- **1.4 Connection between 3.3-V Line and 5-V Line** **26**
- **1.5 QFP Package** **27**
- **1.6 Development Flow** **28**
  - 1.6.1 Development flow (for chips with user logic + ROM/RAM) 28
  - 1.6.2 Development flow (for chips with CPU and CPU peripherals) 29
  - 1.6.3 Description of development flow 30

CHAPTER 2 INTRODUCTION TO CELL-BASED ICs **31**
- **2.1 Estimation of Circuit Size** **32**
  - 2.1.1 Determination of step size 32
  - 2.1.2 Cautions concerning estimation of number of grid utilized 35
  - 2.1.3 Cautions concerning implementation of cores (memory and other large macros) 35
- **2.2 Package Selection** **35**
- **2.3 Power Consumption Check** **39**
- **2.4 Pin Layout** **40**
- **2.5 I/O Interface** **42**
  - 2.5.1 Input block types 42
  - 2.5.2 Output block types 43

CHAPTER 3 PRODUCT SPECIFICATIONS **45**
- **3.1 Terminology** **45**
- **3.2 Absolute Maximum Ratings** **47**
- **3.3 Recommended Operating Conditions** **48**
- **3.4 DC Characteristics** **49**
- **3.5 Pull-up/Pull-down Resistance Values** **52**
- **3.6 AC Characteristics** **53**
- **3.7 Pin Capacitance** **54**

CHAPTER 4 ESTIMATION METHODS FOR CHARACTERISTIC VALUES **57**
- **4.1 Estimation of Static Current Consumption** **57**
  - 4.1.1 Estimation of static current consumption 57
  - 4.1.2 Output leakage current (I_R) 58
- **4.2 Input Through Current** **61**
- **4.3 Power Consumption** **62**
  - 4.3.1 Cause of power consumption 62
  - 4.3.2 Estimation of entire chip's power consumption 63
  - 4.3.3 Estimation of the power consumption of functional cells and interface blocks 64
  - 4.3.4 Detailed estimation of internal circuit power consumption 69

4.3.5 Compensation method for changes in power supply and ambient temperature specifications......72
4.3.6 Determination of power consumption 73
4.4 Propagation Delay Times.... 82
4.4.1 Precision in delay times....82
4.4.2 Calculation of delay times....83
4.4.3 Variation in delay times 85
4.5 Output Buffer Characteristics 88
4.5.1 Output buffer rise and fall times....88
4.5.2 Recommended load capacitance range for output buffers 93
4.5.3 Maximum operating frequency of output buffers....94
4.5.4 Output buffer output currents (I_{OL}, I_{OH})....101
4.6 Simultaneous Switching Limits of Output Buffers 109
4.6.1 Misoperation caused by simultaneous switching....109
4.6.2 SSO factors 111
4.6.3 Determining number of SSO....111
4.6.4 Method for Judging SSO limits 112
4.6.5 Cautions on pin layout 114
4.6.6 Handling when SSO limit is exceeded....114

CHAPTER 5 SYSTEM DESIGN 115
5.1 Circuit Design for Testing.... 115
5.1.1 Circuit for core separate tests....115
5.1.2 Core control pins 125
5.1.3 User logic circuit design for testing....127
5.2 Circuit Design for Debugger.... 127
5.3 Circuit Design for Total Chip Simulation 127
5.4 Design of Clock Lines 128
5.4.1 Asynchronous circuits and synchronous circuits 128
5.4.2 Clock skew 134
5.4.3 Enable control....136
5.4.4 Clock tree synthesis 137
5.4.5 Setting and resetting latches and flip-flops 145
5.5 User Logic Circuit Design for Layout.... 146
5.6 Modular Design.... 147

CHAPTER 6 USER LOGIC DESIGN 149
6.1 Basic Circuit Configuration 149
6.1.1 Use of input and output buffers....149
6.1.2 Handling of unused pins 149
6.1.3 Restriction on fan-out capacity 150
6.1.4 Prohibition of wired logic....150
6.2 Prohibition of Differential Circuits.... 151
6.3 RS Latches and Loop Circuits 151
6.3.1 RS latches 151
6.3.2 Loop circuits 152
6.4 Cautions Concerning High-Speed Circuit Configurations.... 153
6.5 Delay Time Margin.... 154
6.5.1 Timing definitions....155

6.5.2 Delay time margin calculation method (asynchronous circuits) 156
6.5.3 Delay time margin calculation method (high-speed circuits) 157
6.5.4 Minimum pulse width 159
6.5.5 Metastable 160
6.5.6 Critical path 164
6.5.7 Conditions for securing operating margin 166

6.6 Configuration of Internal Buses 167

6.6.1 Internal bus configuration method 167
6.6.2 Prevention of high impedance 167
6.6.3 Restrictions when using bus holder (F098) with internal bus 168
★ 6.6.4 Cautions regarding occurrence of overcurrent at power application 168

6.7 Testability Considerations 169

6.7.1 Initialization of flip-flops 169
6.7.2 Division of counter 169
6.7.3 Addition of test pins and division of circuits 170

6.8 Racing and Spike Noise 170

6.8.1 Racing (conflict) 170
6.8.2 Spike noise 172

CHAPTER 7 TOTAL CHIP SIMULATION FOR CHIP WITH CPU CORE 175

7.1 General 175

7.2 Total Chip Simulation Flow 176

7.3 Creation of Circuit Diagram for Total Chip Simulation 178

7.4 Creation of Program and Test Pattern for Total Chip Simulation 179

7.4.1 Program and test pattern for total chip simulation 179
7.4.2 Cautions concerning creation of programs and test patterns for total chip simulation 179
7.4.3 Test program and test pattern examples 180

7.5 Execution of Simulation Using Circuit Diagram for Total Chip Simulation 191

7.6 Extract Test Pattern for Discrete Cell-Based IC 191

7.7 Verify and Modify Input of “Hi-Z” or “X” Values to Bidirectional Pin’s Input Mode 191

7.8 Check for Test Pattern Conflict and Add Skew 191

7.9 Total Chip Simulation Using Discrete Cell-Based IC 191

CHAPTER 8 SIGN-OFF CONDITIONS AND DATA TO BE PASSED 193

8.1 Basic Conditions for Sign-offs 193

8.2 Data Required for Interface 194

CHAPTER 9 MULTI-FUNCTION BLOCKS 197

9.1 3.3-V, 5-V Interface Blocks 197

9.1.1 Input buffers 197
9.1.2 Output buffers 199

9.2 Input/Output/Bidirectional Buffers with On-Chip Pull-up/Pull-down Resistors 201

9.3 Oscillator Block 202

9.3.1 Overview of oscillator block 202
9.3.2 Cautions on use of oscillator blocks 203
9.3.3 Cautions on oscillator configuration 204
9.3.4 Oscillator block configuration examples 205
9.3.5 Resonator and circuit configuration 206

9.4 GTL (Under Development) **208**
9.4.1 Electrical characteristics 208
9.4.2 Pin layout 209
9.4.3 Connection rules 210
9.4.4 Creation of test patterns 210
9.5 PCI Local Bus Buffer **211**
9.5.1 Signal standard for PCI local bus 211
9.5.2 PCI buffer's output current (I_{OL}, I_{OH}) 213
9.5.3 Electrical characteristics 214
9.6 Scan Path Test Block **214**

APPENDIX A LISTS OF INPUT/OUTPUT PINS AND POWER SUPPLY PINS IN PACKAGES **215**
A.1 VX Type **215**
A.1.1 When using 3.3-V single power supply pins 215
A.1.2 When using internal 2.0-V type power supply pins 221
A.2 VM Type **226**

LIST OF FIGURES (1/3)

Figure No.	Title	Page

1-1 Interface and Supply Voltages 20
1-2 Buffer Layout Example 22
1-3 Equivalent Circuits 26
1-4 Section View of QFP Package 27
1-5 Section View of QFP with Heat Spreader 27
1-6 Section View of TAB in QFP 27

2-1 Relationship between Allowable Power Consumption and Various QFPs 39
2-2 Buffers with Bus Holders 44

4-1 Flow Route of Output Leakage Current (I_R) 58
4-2 Measurement Circuit 58
4-3 Output Leakage Current 59
4-4 5-V Output Buffer Output Waveform 60
4-5 LVTTL Input Through Current (3.3-V Input) 61
4-6 LVTTL Input Through Current (3.3-V Schmitt Input) 61
4-7 TTL 5-V Tolerant Input Through Current (5-V Input) 61
4-8 TTL 5-V Tolerant Input Through Current (5-V Schmitt Input) 61
4-9 5-V Input Through Current 61
4-10 5-V Input Through Current (Schmitt Input) 61
4-11 t_{PD} Variations 87
4-12 $f_{MAX.}$ vs. C_L Restriction (LVTTL Interface, Normal Type) 95
4-13 $f_{MAX.}$ vs. C_L Restriction (LVTTL Interface, Low Noise) 96
4-14 $f_{MAX.}$ vs. C_L Restriction (TTL 5-V Tolerant Interface, Normal Type) 97
4-15 $f_{MAX.}$ vs. C_L Restriction (TTL 5-V Tolerant Interface, Low Noise) 98
4-16 $f_{MAX.}$ vs. C_L Restriction (5-V Interface, Normal Type) 99
4-17 $f_{MAX.}$ vs. C_L Restriction (5-V Interface, Low Noise) 100
4-18 I_O vs. V_O 102
4-19 Misoperation Due to Simultaneous Switching 110

5-1 Test Bus Connection Example 121
5-2 Test Bus Control Circuit Connection Example 123
5-3 Control of Bidirectional Buffer or Three-state Buffer 126
5-4 Example of Countermeasure against High-Impedance Output 127
5-5 Clock Skew 129
5-6 Clock Layout 130
5-7 Example of Multi-phase Clock 131
5-8 Setup/Hold Times for Latches 131
5-9 Division of Combination Circuit 132
5-10 Addition Circuit (Using Three-Phase Clock) 132
5-11 Addition Circuit (Using Single-Phase Clock) 133
5-12 Common Circuit in 74LS Circuit Diagram 133

LIST OF FIGURES (2/3)

Figure No.	Title	Page
5-13	Circuit Using Two-phase Clock	134
5-14	Countermeasures for Clock Lines between Macros	135
5-15	Data Enable Flip-flop	136
5-16	Configuration Example Using Clock Enable	137
5-17	Layout Image for Clock Tree Synthesis	138
5-18	Clock Tree Synthesis	139
5-19	FCTS Layout Restriction	140
5-20	FCTS Layout Diagram	141
5-21	Divide by 5 Counter (Example of Correct Configuration)	145
5-22	Divide by 5 Counter (Example of Incorrect Configuration)	146
5-23	Standardization of Interface between Macros	147
5-24	Modular Design	148
6-1	Basic Circuit Configuration	149
6-2	Prohibition of Wired Logic	150
6-3	Prohibition of Differential Circuits	151
6-4	Asynchronous RS Latch	151
6-5	Loop Circuit	152
6-6	Setup Time	155
6-7	Hold Time	155
6-8	Release Time	155
6-9	Removal Time	155
6-10	Minimum Pulse Width	155
6-11	Circuit Example for Delay Time Margin Calculation	156
6-12	Estimated Timing	156
6-13	In-Phase Clock Circuit Example	157
6-14	Timing for In-Phase Clock	157
6-15	Reverse-Phase Clock Circuit Example	158
6-16	Timing for Reverse-Phase Clock	158
6-17	Estimation of Minimum Pulse Width	159
6-18	Reduction of Pulse Width	159
6-19	System that Includes Critical Paths	164
6-20	Example of Critical Path between Input and Input	165
6-21	Verification of Setup Time	165
6-22	Configuration Examples of Circuits for Preventing High Impedance of Internal Bus	167
6-23	Initialization of Flip-Flop	169
6-24	Division of Counter	169
6-25	Racing	171
6-26	Data Selector Circuit Example	172
6-27	Test Pattern Example (Before Modification)	173
6-28	Test Pattern Example (After Modification)	174

LIST OF FIGURES (3/3)

Figure No.	Title	Page
7-1	Flow of Total Chip Simulation Pattern Generation	176
7-2	Creation of Circuit Diagram for Total Chip Simulation	178
7-3	Block Diagram of Circuit Used for Total Chip Simulation	180
7-4	Block Diagram of System Circuit	181
7-5	Example of Test Pattern for Total Chip Simulation (with External ROM)	182
7-6	Circuit for Total Chip Simulation (with Added ROM and RAM for Simulation)	183
7-7	Program Flow for Total Chip Simulation	184
7-8	Example of Execution Steps When Using OPENCAD (Using V.sim™)	192
9-1	Equivalent Circuit Diagrams of 3.3-V and 5-V Input Buffers	198
9-2	Equivalent Circuit Diagrams and Connection Example of 3.3-V Input Buffer with Fail-safe Function	198
9-3	Equivalent Circuit Diagrams of Output Buffers	200
9-4	Connection Examples of TTL 5-V Tolerant Output Buffer and 5-V Output Buffer	200
9-5	Oscillator Block Configuration Examples	205
9-6	Oscillator Configuration Diagrams	207
9-7	GTL Pin Layout Example	209
9-8	GTL Use Example	210
9-9	PCI Pin List	211
9-10	V_O vs. I_O	213
9-11	Principles of Scan Path Test Method	214

LIST OF TABLES (1/2)

Table No.	Title	Page
1-1	Abbreviated List of Specifications: CB-9 Family's VX/VM Types	19
2-1	Total Grid Counts and Grid Utilization Rates for Each Step Size	34
2-2	Package List	36
3-1	Terms Used in Absolute Maximum Ratings	45
3-2	Terms Used in Recommended Operating Range	46
3-3	Terms Used in DC Characteristics	46
3-4	Absolute Maximum Ratings	47
3-5	Recommended Operating Conditions	48
3-6	DC Characteristics (V_{DD} = 3.3±0.3 V, T_A = –40 to +85°C)	49
3-7	Pull-up/Pull-down Resistance Values (V_{DD} = 3.3±0.3 V, T_A = –40 to +85°C)	52
3-8	Pull-up/Pull-down Resistance Values (V_{DD} = 5.0±0.5 V, T_A = –40 to +85°C)	52
3-9	AC Characteristics (T_A = –40 to +85°C)	53
3-10	Package Capacitance (C_P) (V_{DD} = 0 V, T_A = 25°C)	54
3-11	Interface Block Capacitance (C_B)	56
4-1	Power Consumption by Each Input Buffer	65
4-2	Power Consumption by Output Buffers	66
4-3	Power Consumption by GTL Input Section	67
4-4	Maximum Allowable Power Consumption	74
4-5	List of Thermal Resistance Values	77
4-6	Propagation Delay Time Characteristics	85
4-7	List of Coefficients for LVTTL Output Buffer t_r and t_f Calculations	89
4-8	List of Coefficients for TTL 5-V Tolerant Output Buffer t_r and t_f Calculations	90
4-9	List of Coefficients for 5-V Output Buffer t_r and t_f Calculations	91
4-10	List of Coefficients for 3.3 V-to-2.0 V Output Buffer t_r and t_f Calculations	92
4-11	Recommended Load Capacitance Ranges (pF) for Output Buffers	93
4-12	SSO Limitation Time Range (TYP.)	112
4-13	Limited Number of SSO Pins between 3 GND Pins (3.3-V Output Buffer, I_{OL} = 12 mA)	112
4-14	SSO Pin Conversion Coefficients	113
5-1	Circuit Design Characteristics	128
5-2	FCTS Clock Skew (V_{DD} = 3.3 V, T_A = –40 to +85°C)	142
5-3	FCTS Clock Skew (V_{DD} = 2.0 V, T_A = –40 to +85°C)	142
5-4	FCTS Clock Tree Block Predicted Delay Time Reference Values (V_{DD} = 3.3 V: TYP.)	143
5-5	FCTS Clock Tree Block Predicted Delay Time Reference Values (V_{DD} = 2.0 V: TYP.)	143
5-6	FCTS Specifications (V_{DD} = 3.3 V)	143
5-7	FCTS Specifications (V_{DD} = 2.0 V)	143
5-8	Example of Standard Bus Interfaces for Single-Chip Design	148

LIST OF TABLES (2/2)

Table No.	Title	Page
9-1	Recommended Oscillation Frequency Ranges for Oscillator Blocks	202
9-2	Ceramic Resonator Evaluation List	206
9-3	Crystal Resonator Evaluation List	207
9-4	Electrical Characteristics of GTL	208
A-1	List of Power Supply Pins in Packages (VX Type, 3.3-V Single Power Supply)	215
A-2	List of Power Supply Pins in Packages (VX Type, When Using Internal 2.0-V Power Supply Pin)	221
A-3	List of Power Supply Pins in Packages (VM Type)	226

[MEMO]

CHAPTER 1 GENERAL

1.1 Features

The CB-9 Family's VX/VM Types (μPD82×××) use a 0.35-μm process for high-precision fabrication of cell-based ICs that include a two-layer or three-layer wiring layout for low power consumption, high speed, and high integration.

Users may choose between two types based on power supply voltage: the VX Type (2.0-V or 3.3-V internal power supply, 3.3-V I/O power supply), which is the low-power version, or the VM Type (3.3-V internal power supply, 5-V or 3.3-V I/O power supply), which is the ordinary version.

Table 1-1. Abbreviated List of Specifications: CB-9 Family's VX/VM Types

Type		VX Type	VM Type
Power supply voltage Note	Internal	2.0 V, 3.3 V	3.3 V
	I/O	3.3 V	3.3 V, 5.0 V
I/O interface		LVTTL, TTL 5-V tolerant maximum voltage	LVTTL, TTL, CMOS 5 V
Operating temperature Note		–40 to +85°C	
Delay time	Internal gate	114 ps (V_{DD} = 3.3 V, fan-outs = 2, ℓ = standard wiring length, power gate) 207 ps (V_{DD} = 2.0 V, fan-outs = 2, ℓ = standard wiring length, power gate)	
	Input buffer	169 ps (V_{DD} = 3.3 V, fan-outs = 2, ℓ = standard wiring length) 690 ps (V_{DD} = 5.0 V, fan-outs = 2, ℓ = standard wiring length)	
	Output buffer	864 ps (V_{DD} = 3.3 V, load = 15 pF, I_{OL} = 18 mA) 2045 ps (V_{DD} = 5.0 V, load = 15 pF, I_{OL} = 18 mA)	
Power consumption		0.3 μW/MHz/gate (V_{DD} = 3.3 V) 0.12 μW/MHz/gate (V_{DD} = 2.0 V)	
Technology (design rule)		0.35-μm silicon gate CMOS	
Packages	QFP (fine pitch)	100, 120, 144, 160, 176, 208, 240, 304	
	QFP (with heat spreader)	160, 176, 208, 240, 304	
	TQFP	100, 120	
	LQFP	144, 160, 176, 208	
	PGA	364, 528	
	BGA	256, 352, 420, 500, 576, 696	

Note If the device includes cores, the guaranteed ranges may differ according to the cores that are included.

Remark Before starting design work, contact NEC for the latest information on available packages, which are continually being updated.

1.1.1 Features of VX/VM types

Unlike previous products, the CB-9 Family's VX/VM types enable the voltage of the I/O power supply and internal power supply to be set separately. The VX type can be operated using 2.0-V power internally while also using a 3.3-V I/O power supply, and the VM type can be operated using 3.3-V power internally while also using a 5-V I/O power supply. Both are suited for systems featuring low power consumption.

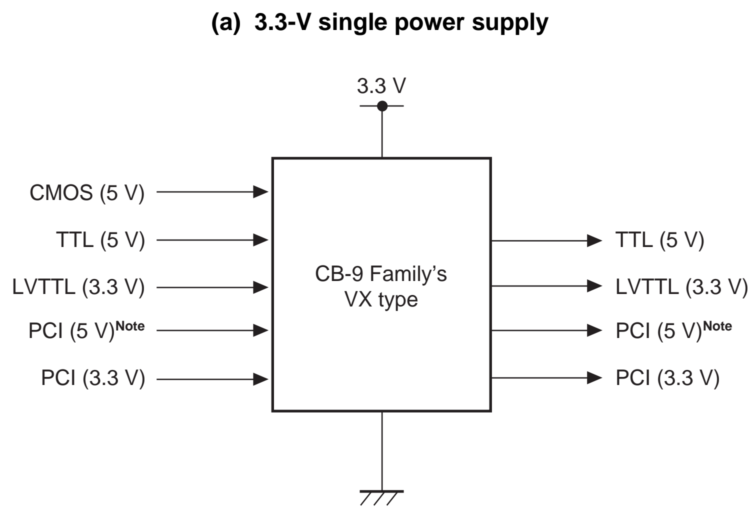
(1) Interface levels and power supply voltages

The CB-9 Family's VX/VM types are available with a 3.3-V or 5-V I/O power supply. Select the type best suited to the target system. CMOS 5-V, TTL, PCI (5 V) can be used when using the 5-V power supply type, and TTL, LVTTL, PCI (3 V) can be used when using the 3.3-V power supply type.

Use a TTL 5-V tolerant buffer when using a TTL interface with the 3.3-V power supply type.

Figure 1-1. Interface and Supply Voltages (1/2)

(a) 3.3-V single power supply

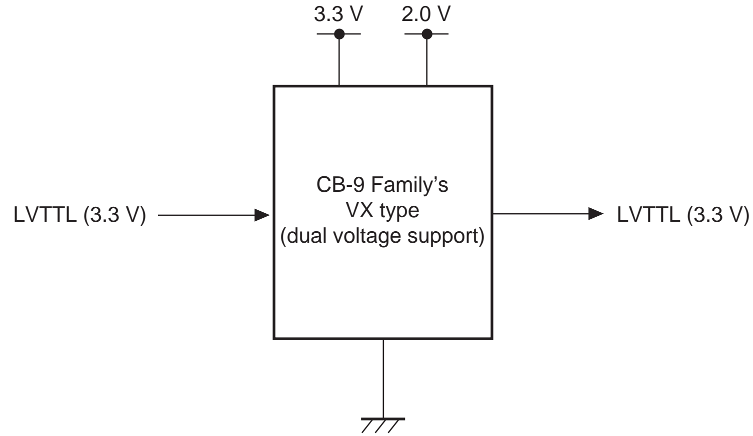


Remark Voltage values in parentheses indicate the interface standard.

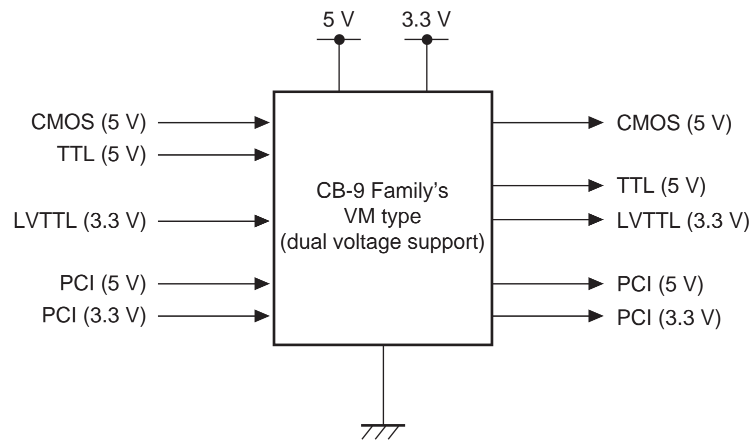
Note When using a VX-type 5-V PCI, a separate 5-V power supply is required (see **9.5.1 Signal standard for PCI local bus**).

Figure 1-1. Interface and Supply Voltages (2/2)

(b) I/O: 3.3 V, internal: 2.0 V



(c) I/O: 3.3 V or 5 V, internal: 3.3 V

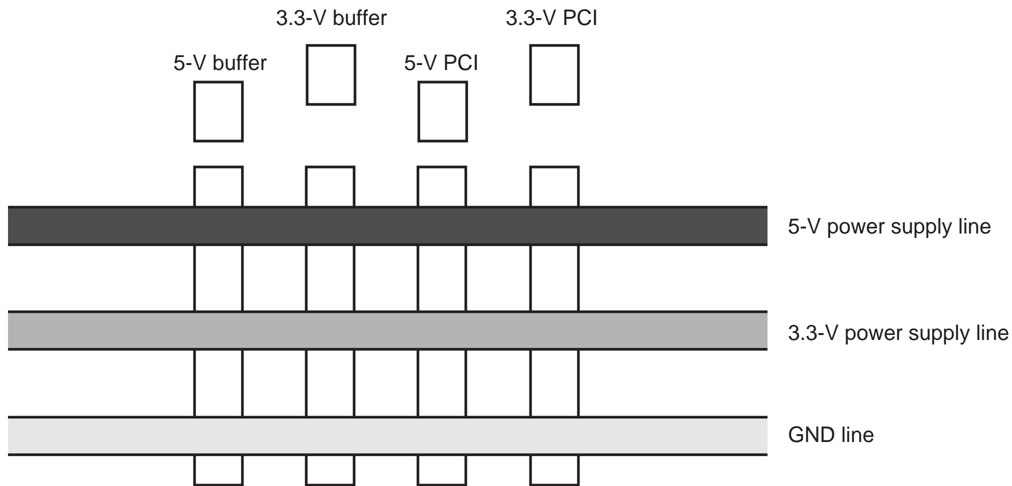


Remark Voltage values in parentheses indicate the interface standard.

(2) I/O buffer layout

The VM type uses the power supply lines shown in Figure 1-2, which means that the 5-V buffer and 3.3-V buffer can be laid out independently. However, latch-up may occur when 5-V buffer is placed next to TTL 5-V-tolerant buffer (refer to **2.4 (5) 5-V buffer**).

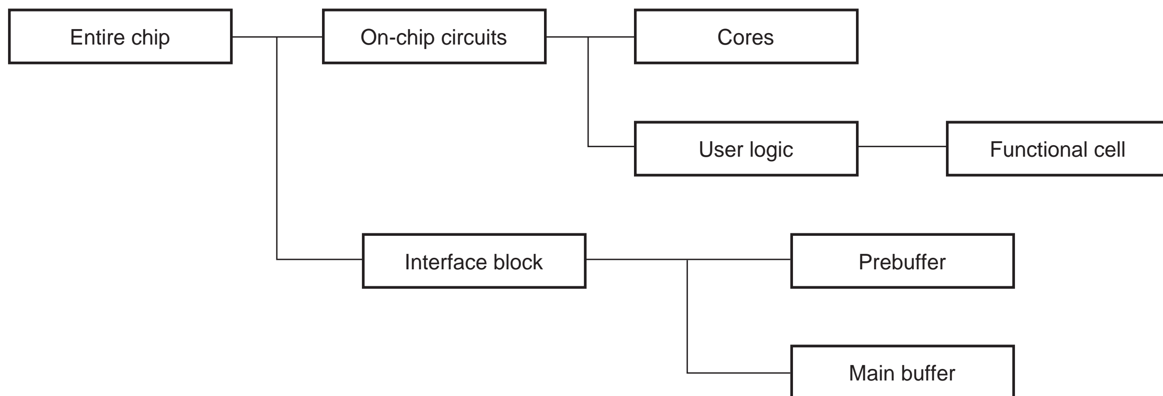
Figure 1-2. Buffer Layout Example



1.2 Internal Configuration of Cell-Based ICs

1.2.1 Chip configuration

Cell-based ICs generally include the following elements.



The meanings of these elements are described below.

Elements	Description
Core	A function block and memory macro that includes a large number of gates, such as a CPU core or peripheral macro
User logic	Circuits created by the user using functional cells
Functional cell	A cell that contains basic functions such as OR, AND, and flip-flop
Interface block	A block used as an interface for external pins
Prebuffer	A buffer that is used to control the main buffer and that includes an interface block
Main buffer	A buffer that is used as an interface for external devices and that includes an interface block
On-chip circuits	All circuits other than the interface block

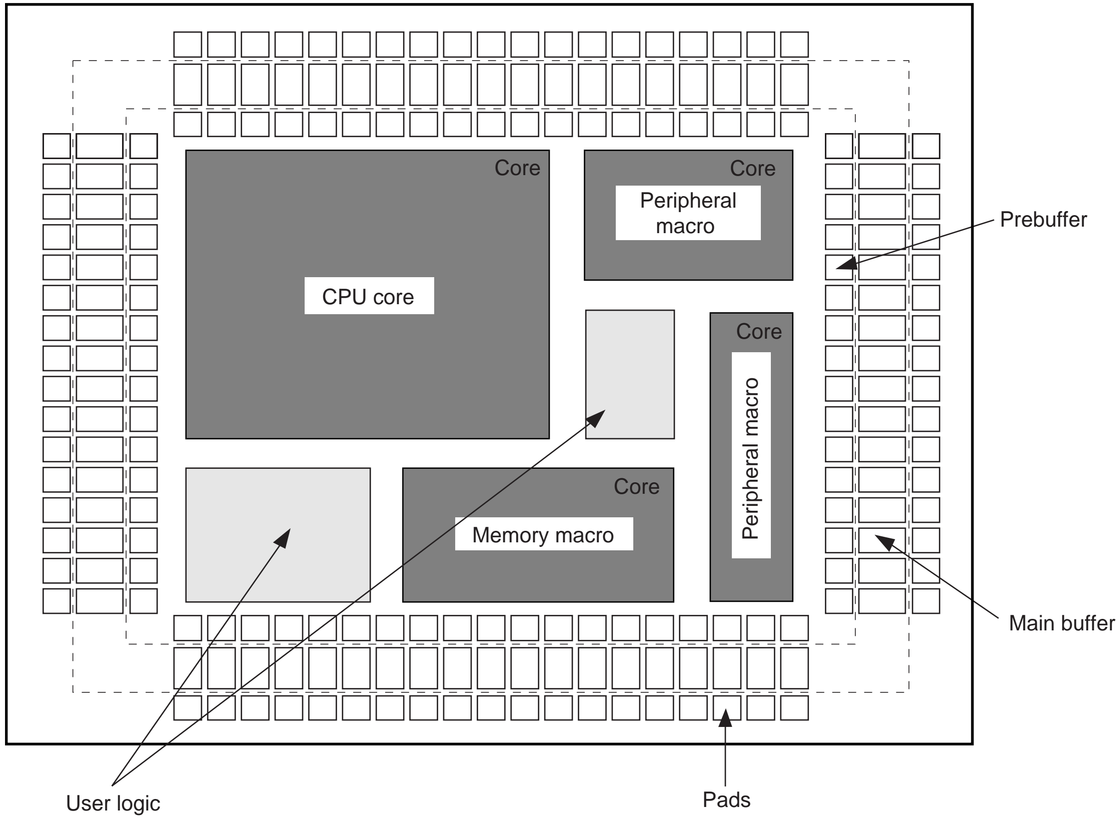
Remark The interface block is a general term that refers to the input buffer, output buffer, and bidirectional buffer.

1.2.2 Chip layout

NEC's cell-based ICs use the building block method.

In the NA7105x and other products, the cores found in NEC's standard ICs can be combined with user logic on the same chip.

A chip layout example is shown below.



1.3 On-chip Transistor Configuration

CMOS circuits include a P-channel MOS transistor (P-ch.Tr) and an N-channel MOS transistor (N-ch.Tr). Ordinarily, either the P-ch.Tr or the N-ch.Tr remains off.

Consequently, almost no power supply current flows through the circuits when the device is in a steady (stationary) state, which keeps power consumption extremely low.

Almost all of the current consumption in CMOS devices occurs when switching circuits. Because an excessively large current flows during these switching operations, a high-speed high-capacity capacitor must be inserted between the power supply and the ground (GND) to sufficiently reduce the power supply's impedance.

When a large waveform is inserted to the CMOS circuits during the rising edge or falling edge period, a through current is fed between the P-ch.Tr and N-ch.Tr to enable both the P-ch.Tr and N-ch.Tr to remain on for a long period. Not only does this increase the current consumption, it can also cause operation faults.

A dual-input NOR gate equivalent circuit diagram and a dual-input NAND gate equivalent circuit diagram are shown respectively in parts (a) and (b) of Figure 1-3. The N-ch.Tr has a generally lower ON-state resistance (about half that of P-ch.Tr), which means that a larger current can be conducted through N-ch.Tr.

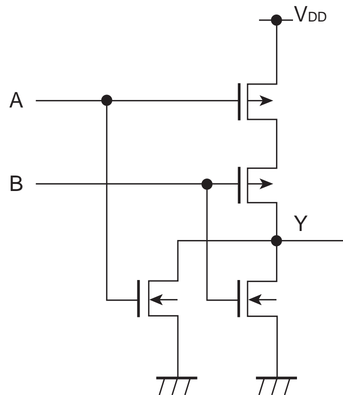
Therefore, as shown in part (a) of Figure 1-3, the ON-state resistance is very large on the output's rising edge in NOR gates connected in series to P-ch.Tr, which reduces the load drive capacity.

In CMOS cell-based ICs, the NOR blocks are slower than NAND blocks and have poor fan-out characteristics. Consequently, NAND blocks should be used whenever possible to increase circuit speed and provide greater circuit stability.

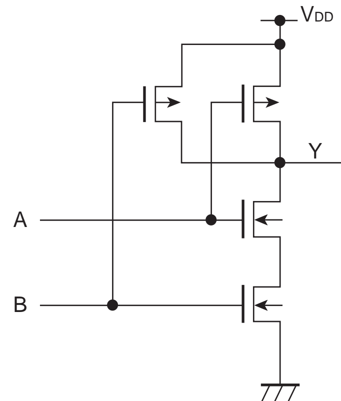
For much the same reasons, a complex gate that includes many transistors connected in series tends to be slow and are thus ill-suited for high-speed circuits, but when used in parts of the chip where high speed is not required, they provide a good method for improving circuit stability and making effective use of cells.

Figure 1-3. Equivalent Circuits

(a) Dual-input NOR equivalent circuit



(b) Dual-input NAND equivalent circuit



1.4 Connection between 3.3-V Line and 5-V Line

Ultra-precise processing of transistors and reduction of power supply voltage are both essential factors in developing faster LSIs that consume less power. This is why lower power consumption has been sought in recent years in microcontrollers, memory devices, etc. Even among cell-based ICs, in the CB-9 Family, which are fabricated using cutting-edge transistor processing technologies, 3.3 V is the standard power supply voltage. However, 3.3 V is not yet the standard in all LSIs. Therefore, CB-9 Family products include an interface block to support connection of conventional LSIs with 5-V power supply voltage.

3.3-V input blocks are used to receive 3.3-V signals and therefore cannot be used to receive 5-V signals, which must be received by 5-V input blocks. The 5-V input blocks are designed to support the trend toward 3.3-V power supply voltage in peripheral circuits of conventional cell-based ICs by being able to receive 3.3-V signals. They also include 3.3-V input blocks with fail-safe functions that can be used for hot-line work.

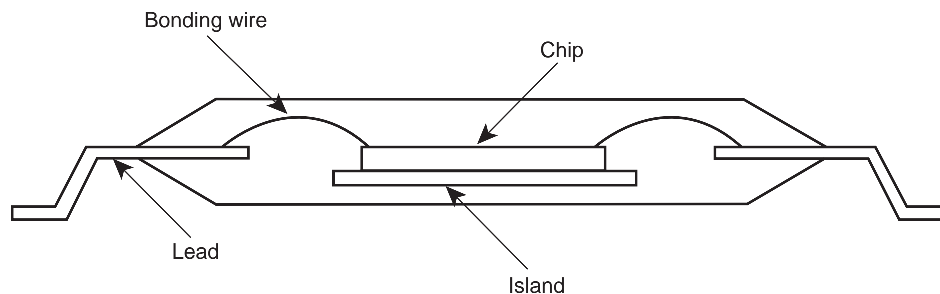
In the output buffer, the output high level continues to be the same level as the V_{DD} level in cell-based ICs, and both an LVTTL output buffer and a 5-V output buffer are provided. Unlike in previous products, the 5-V output buffer can pull up pins using 5-V voltage which is greater than the LSI's power supply voltage. This means that it can be connected to a 5-V bus line. For details of these blocks, see **9.1 3.3-V, 5-V Interface Blocks**.

1.5 QFP Package

Figure 1-4 shows a section view of an ordinary QFP package. In such QFP packages, the chip is inserted on a metal plate called an “island”. This structure includes very thin bonding wires (a few dozen μm thick) that connect the component leads to the chip.

QFP packages that have low thermal resistance use heat-discharging materials in their component leads and islands, however, their structure is same as ordinary QFP packages.

Figure 1-4. Section View of QFP Package



QFPs that include a heat spreader are made of the same materials as low thermal resistance type QFPs. The heat spreader-equipped QFP is characterized by its large island (the heat spreader) that provides greater heat dissipation (see Figure 1-5).

The “TAB in QFP” is a new type of QFP that has been introduced via the CB-9 Family. To enable many pins to be attached to a small chip, the gaps between the bonding pads on the chip had to be narrowed. However, narrowing these gaps makes it very difficult to connect bonding wire between the component leads and the pads. Therefore, TAB (Tape Automated Bonding) tape is used instead of bonding wire to connect the leads and pads, and hence the name “TAB in QFP” (see Figure 1-6). This type of package also features a large island that has heat dissipation effects similar to those of heat spreader packages.

Figure 1-5. Section View of QFP with Heat Spreader

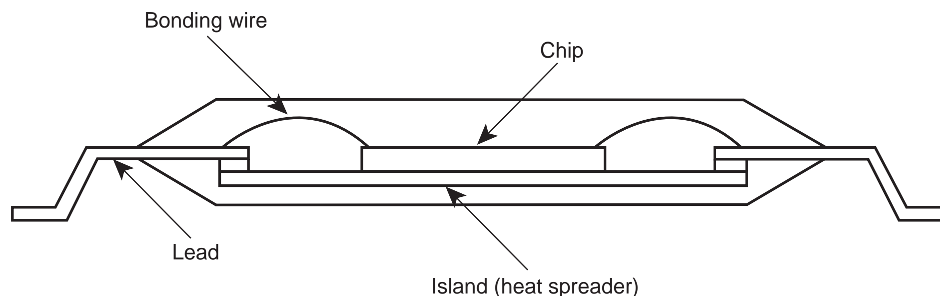
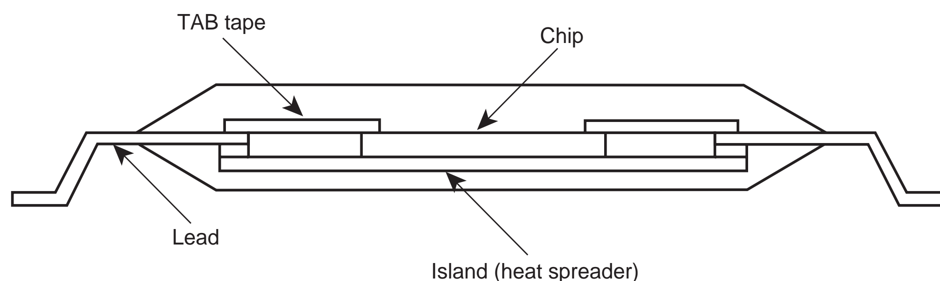
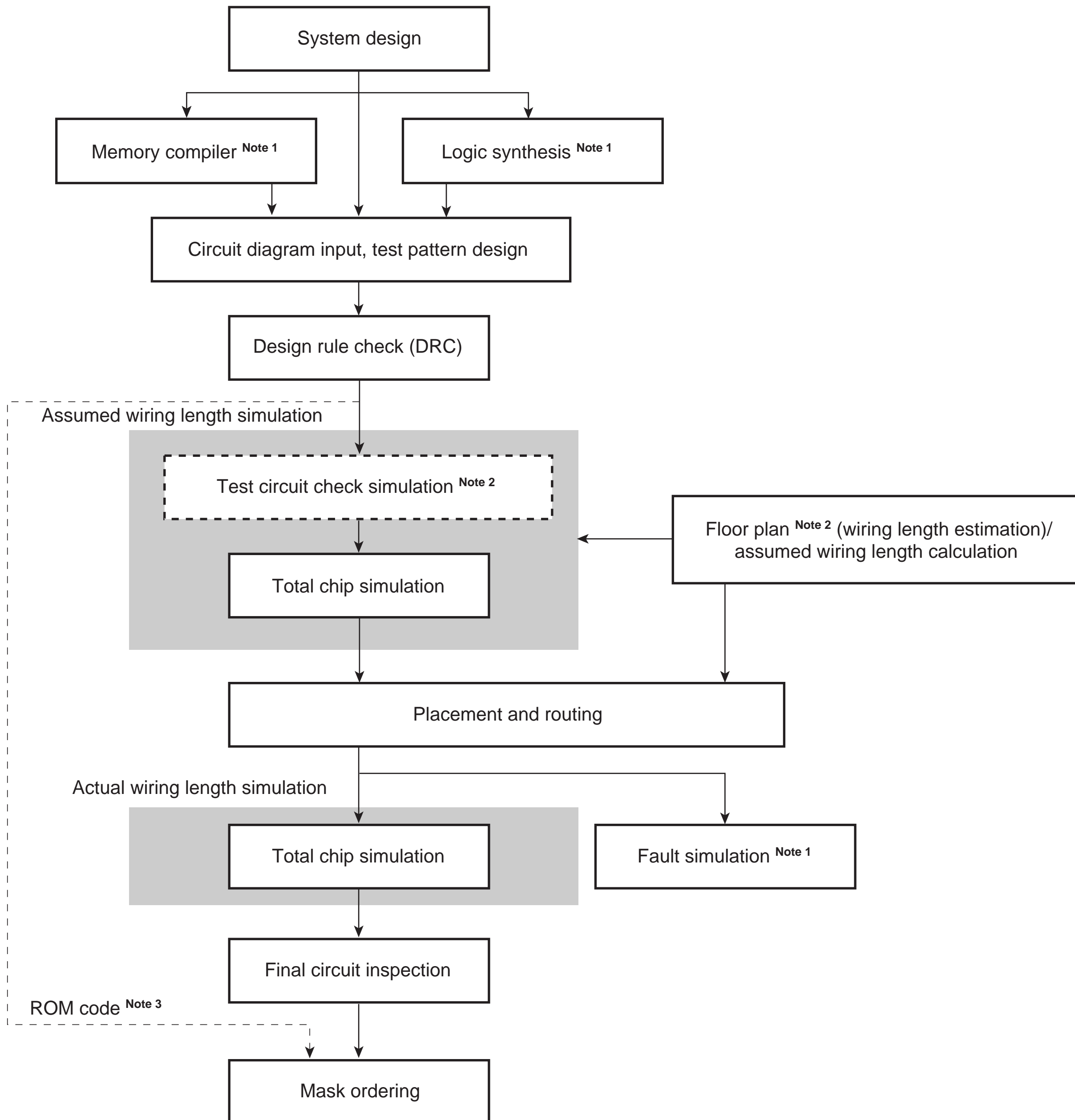


Figure 1-6. Section View of TAB in QFP



1.6 Development Flow

1.6.1 Development flow (for chips with user logic + ROM/RAM)

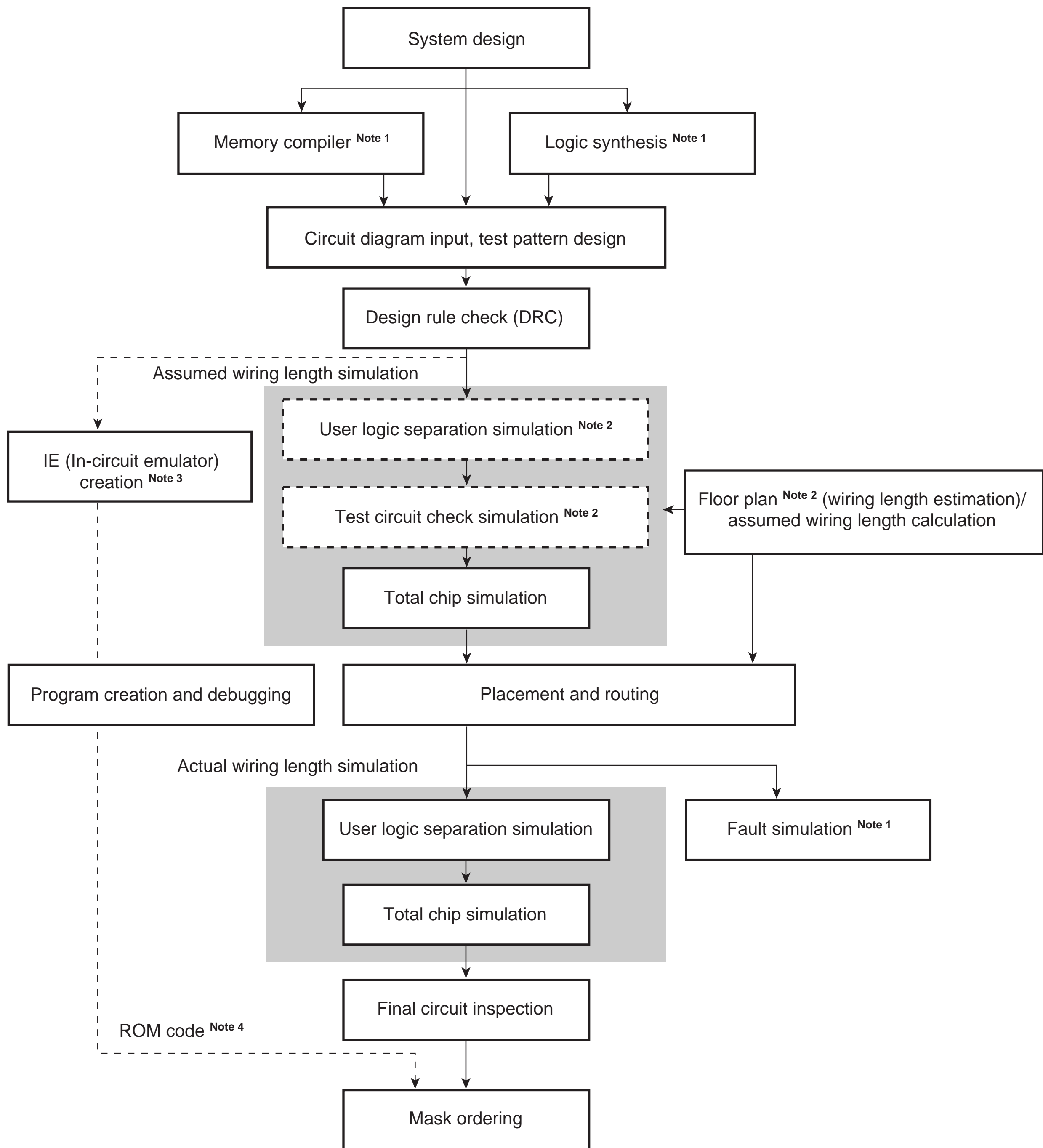


Notes 1. This is an optional function that may not be usable depending on the tool used.

2. Necessary only when memory macros are mounted.

3. Necessary only when ROM macros are mounted.

1.6.2 Development flow (for chips with CPU and CPU peripherals)



Notes 1. This is an optional function that may not be usable depending on the tool used.

2. Necessary only when cores are mounted.

3. Necessary only when CPU cores are mounted.

4. Necessary only when ROM macros are mounted.

1.6.3 Description of development flow

Item	Description
System design	This includes the setting of system specifications before starting the detailed design in order to implement required functions more economically and efficiently.
Memory compiler	This step is required only when the chip contains RAM or ROM. Specifying the bit width and the number of words enables the required RAM and/or ROM to be implemented more easily.
Logic synthesis	Verilog HDL (Hardware Description Language) can be used to automatically generate gate-level circuits. Also, a netlist can be used to optimize logic circuit areas and delay times.
DRC (Design Rule Check)	A check is performed to ensure compliance with all design rules.
Assumed wiring length simulation	
User logic separation simulation [Note 1]	If cores such as a CPU core or CPU peripheral macro are on chip, the gate conversion of the CPU core alone may result in a circuit having tens of thousands of gates. Accordingly, as a way of making the development process more effective, we recommend that the user logic block be implemented separately on a test circuit, which enables a separate simulation to be executed so as to identify and eliminate circuit errors before proceeding to the total chip simulation.
Test circuit check [Note 2]	This check is performed to verify that the core's separate test circuits are correctly connected. We recommend checking to confirm the core block's test can be used as a test circuit for a standard test pattern in the process of shipment inspection.
Floor planning	Floor planning determines how core and user logic blocks will be laid out on the chip. The optimum layout is one that minimizes the total wiring length while also minimizing dead space on the chip.
Assumed wiring length calculation	This calculates an estimated wiring length which is needed to perform simulations before deciding the final layout. The division of the circuit's second layer into blocks is taken into account while estimating the wiring length between blocks based on each block is assumed wiring length and the step size being used. If the user is performing the floor planning, the wire length can be calculated with the floor plan taken into account.
Total chip simulation	This simulates the actual operation mode of the entire chip. Consists mainly in checking the wire connections between macros.
Fault simulation	This simulation determines how many faults can be detected (i.e., the fault coverage) in all circuits using the user-generated test pattern and which part of the faults can not be detected.
Actual wiring length simulation	Using the wiring length of an actual layout (i.e., the actual wiring length), a separate simulation is performed on user logic and a total chip simulation is also performed. The simulation conditions are intended to reflect the actual operating conditions and the tester conditions.
IE setup	If the chip contains a CPU core, an in-circuit emulator is set up to aid the development of application software.

Notes 1. This is not required for a user logic + RAM/ROM chip.

2. If the chip includes a RAM macro, be sure to access RAM during test mode to check the test circuit. If the chip includes a ROM macro, be sure to set up a test pattern that will output all of the bits in the ROM code during test mode.

CHAPTER 2 INTRODUCTION TO CELL-BASED ICs

When designing LSIs using cell-based ICs for all or part of a user-designed system, determine the specifications as follows to ensure appropriate cell-based IC circuit size and an optimum number of I/O pins.

Although larger circuit sizes make circuit design more difficult and raise the LSI's unit cost, the LSI's PC board mount area can be reduced to minimize the number of required I/O pins. In addition, propagation delay times can be reduced by minimizing the number of required LSIs.

On the other hand, while reducing the circuit size facilitates design, a greater number of cell-based ICs are needed to configure the system, which can be inconvenient for PC board mounting. Also, the fact that signals must be propagated between many LSIs makes it difficult to minimize propagation delay times.

Accordingly, when designing cell-based ICs, the whole range of issues from propagation delay time and circuit size to implementation areas must be taken into consideration.

Use the following initial steps when designing these circuits.

Initial steps in circuit design

(1) Estimate circuit size and step size

↓

(2) Select package

↓

(3) Check power consumption

↓

(4) Pin layout

↓

(5) Check I/O interface level

2.1 Estimation of Circuit Size

2.1.1 Determination of step size

There are 25 step sizes available in the CB-9 Family's VX/VM type cell-based ICs. The step size depends on the number of gates used. Consider the following items when determining the step size for user circuits.

(1) Wiring layout method (two layer/three layer)
(2) Type and quantity of on-chip cores
(3) Scope of user logic
(4) Number of pin pairs
(5) Floor plan (core layout method)
(6) Package selection
(7) Number of required signals

When there are a large number of cores or when the user logic block is small, there may be cases where the number of steps that must be selected according to floor planning restrictions and is greater than the number of steps selected based on simple grid conversion.

A general method for investigating supported step sizes is described below. This method provides only a general criterion and it should not be used for investigating unit costs, etc. No matter what the number of steps is, the TAT and unit costs still differ depending on whether the IC uses two-layer or three-layer design.

[Criterion for when Σ (core grid count) ≤ (user logic grid count)]

$$M + \frac{U + B}{\gamma} \leq L$$

M: Σ (including the various core grids and wiring area)
U: Σ (user logic grid count)
B: Σ (Interface block grid count)
L: Total grid count for expected steps
γ: Grid utilization rate (percentage of usable grids among all mounted grids in user logic block)

Table 2-1 lists the total grid counts and the grid utilization rates for each step size.

- **Criterion for correspondence of gate count to grid count in user logic block.**

When investigating size issues, setting the correspondence of gate count (in which each dual-input NAND gate is converted to one gate) to grid count in user logic blocks depends greatly on the type of functional block being used. The following formula is based on averages.

1 gate ≒ 3.0 grids

For a formal investigation, use the grid count information in the list output from the design rule check program or use values converted from the grid count indicated in the block library.

[Σ (core grid count) > Σ (criterion for user logic grid count)]

This requires a detailed investigation that takes floor planning into account. For details of floor planning, contact NEC.

Table 2-1. Total Grid Counts and Grid Utilization Rates for Each Step Size

Step Size	Grid Utilization Rate[Note 1]		No. of Grids Utilized	
	Two Layer	Three Layer	VX Type (LVTTL Buffer Only)	VX Type[Note 2], VM Type
B60*	51%	75%	527500	397700
C02*	50%	74%	706500	555800
C40*	49%	73%	869500	721000
C78*	48%	72%	1101200	915400
D01*	48%	72%	1223500	1037300
D26*	47%	71%	1378400	1177000
D52*	47%	71%	1546300	1339300
D90*	46%	70%	1812800	1579500
E16*	46%	70%	2011000	1746900
E54*	45%	70%	2294700	2027500
E80*	45%	69%	2488900	2235800
F18*	44%	69%	2814700	2531800
F44*	44%	69%	3056800	2732300
F70*	44%	68%	3271700	2971300
G08*	43%	68%	3639300	3320000
G34*	43%	68%	3867700	3545900
G72*	43%	67%	4274000	3920200
H10*	42%	67%	4683400	4315600
H49*	42%	67%	5105600	4741200
H87*	42%	66%	5539200	5166000
J26*	41%	66%	5951500	5608200
J51*	41%	66%	6263000	5873000
K15*	41%	65%	7089400	6679800
K92*	40%	65%	8037500	7607500

Notes 1. The grid utilization rate changes depending on the number of pin pairs. The values indicated in this table are representative values and cannot be used to estimate steps.

2. When using TTL 5-V tolerant buffer and buffer with fail-safe or 2.0-V internal power supply type.

Remark The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C
See also **2.2 Package Selection**.

2.1.2 Cautions concerning estimation of number of grid utilized

(1) Input/Output/Bidirectional buffer block

When configuring various external interface blocks (input/output/bidirectional), both I/O areas and internal areas are used. Therefore, to calculate the total grid utilization, add the number of internal input/output/bidirectional glids to be used, as described in Block Library.

(2) Critical paths

If there is a path for which speed is an important consideration, there are methods for shortening the propagation path for each block along the path. However, using these methods may drastically reduce wire design flexibility. In such cases, the design rule should be to remain within 80% or 90% of the limit values for the grid utilization rate.

2.1.3 Cautions concerning implementation of cores (memory and other large macros)

The following points should be noted when implementing cores.

- External pin layout
- Block types used for circuits other than in macro section

(1) External pin layout

When several cores have been implemented, lay out related external pins as close to the implemented macros as possible. If the macro layout has been done without considering the external pins, the wire length to external pins will be longer, which will reduce the grid utilization rate. As a result, the wiring may not be complete in some cases. Be sure to contact NEC concerning the macro layout method if you plan to use several cores.

(2) Block types used for circuits other than in macro section

If the number of available grids is extremely small in the gate section due to the implementation of a core, there may be cases in which medium-size macros such as an 8-bit latch cannot be physically implemented.

2.2 Package Selection

The CB-9 Family’s VX/VM type includes a package for each step size. Select the package that best suits the number of I/O pins cited in the circuit specifications.

CB-9 Family VX/VM type devices do not have input-only pins or output-only pins. The number of I/O pins and power supply pins varies according to the step size being used.

The position of the power supply pins and the number of signal pins differ according to the package. See **APPENDIX A LISTS OF INPUT/OUTPUT PINS AND POWER SUPPLY PINS IN PACKAGES**.

Contact NEC for the latest release information on packages.

Table 2-2. Package List (1/3)

Package						B60*	C02*	C40*	C78*	D01*	D26*	D52*	D90*
Type	No. of Pins	External Dimensions (mm)	Lead Pitch (mm)	Resin Thickness (mm)	CODE								
QFP	44	10 × 10	0.80	2.70	44GB-3B4	C	–	–	–	–	–	–	–
	52	14 × 14	1.00	2.70	52GC-3B6	C	–	–	–	–	–	–	–
	64	14 × 20	1.00	2.70	64GF-3BE	C	–	–	–	–	–	–	–
	100	14 × 20	0.65	2.70	A0GF-3BA	–	–	–	C	C	C	C	–
	120	28 × 28	0.80	3.70	C0GD-5BB	–	–	C	C	C	C	C	C
	160	28 × 28	0.65	3.70	G0GD-5BD	–	–	–	–	–	C	C	C
	160[Note 1]	28 × 28	0.65	3.20	XFGD-LBD	–	–	–	–	–	–	C	C
QFP (fine pitch)	100	14 × 14	0.50	1.45	A0GC-7EA	C	C	C	C	C	C	C	C
	120	20 × 20	0.50	2.70	C0GJ-3EB	–	C	C	C	C	C	C	C
	144	20 × 20	0.50	2.70	E4GJ-3EN	–	–	C	C	C	C	C	C
	160	24 × 24	0.50	2.70	G0GM-3ED	–	–	–	–	–	C	C	C
	176	24 × 24	0.50	2.70	H6GM-3EU	–	–	–	–	–	–	–	C
	144[Note 1]	20 × 20	0.50	2.70	XRGJ-JEU	C	T	T	C	C	C	C	C
	160[Note 1]	24 × 24	0.50	2.70	XFGM-JED	C	T	T	T	T	C	T	C
	176[Note 1]	24 × 24	0.50	2.70	XEGM-JEU	C	C	T	T	T	T	T	C
	208[Note 1]	28 × 28	0.50	3.20	XAGD-LML	–	C	C	T	T	T	T	T
	240[Note 1]	32 × 32	0.50	3.20	Q0GN-LMU	–	–	C	C	T	T	T	T
	256[Note 1]	28 × 28	0.40	3.20	R6GD-LMV	–	–	–	–	–	–	–	–
	304[Note 1]	40 × 40	0.50	3.70	W4GL-NMU	–	–	–	–	–	–	–	–
QFP (fine pitch) with HSP	160[Note 1]	24 × 24	0.50	2.70	XCGM-KED	–	–	–	–	–	–	–	C
	176[Note 1]	24 × 24	0.50	2.70	XHGM-KEU	–	–	–	–	–	–	–	–
	208[Note 1]	28 × 28	0.50	3.20	XBGD-MML	–	–	–	–	–	–	–	–
	240[Note 1]	32 × 32	0.50	3.20	XNGN-MMU	–	–	–	–	–	–	–	–
	304[Note 1]	40 × 40	0.50	3.70	XJGL-PMU	–	–	–	–	–	–	–	–
TQFP	64[Note 1]	10 × 10	0.50	1.00	64GB-9EU	C	C	–	–	–	–	–	–
	80	12 × 12	0.50	1.05	80GK-BE9	C	C	C	C	C	C	C	–
	100[Note 1]	14 × 14	0.50	1.00	XDGC-9EU	C	C	C	C	C	C	C	C
	120[Note 1]	14 × 14	0.40	1.00	XMGC-9EV	–	C	C	C	C	C	C	C
LQFP	144[Note 1]	20 × 20	0.50	1.40	XGGJ-8EU	–	–	C	C	C	C	C	C
	160[Note 1]	24 × 24	0.50	1.40	XLGM-8ED	–	–	–	–	–	–	–	–
	176[Note 1]	24 × 24	0.50	1.40	XSGM-8EU	–	–	–	–	–	–	C	C
	208[Note 1]	28 × 28	0.50	1.40	XKGD-8EU	–	–	–	–	–	–	–	–
Plastic BGA	225	27 × 27	1.50	1.53	N5S1-B1	–	–	–	–	–	–	T	T
	256	27 × 27	1.27	1.53	WNS1-B6	–	–	–	C	C	C	T	T
	313	35 × 35	2.54[Note 2]	1.73	X3S1-F5	–	–	–	–	–	–	–	C
	352	35 × 35	1.27	1.73	AGS1-F6	–	–	–	–	–	–	–	–
Tape BGA	256	27 × 27	1.27	0.80	R6N7-B6	–	–	–	C	C	C	T	T
	352	35 × 35	1.27	0.80	AGN7-F6	–	–	–	C	C	C	C	C
	420	35 × 35	1.27	0.80	BFN7-F6	–	–	–	–	–	–	–	–
	500	40 × 40	1.27	0.80	CGN7-H6	–	–	–	–	–	–	–	–
	576	40 × 40	1.27	0.80	CCN7-H6	–	–	–	–	–	–	–	–
	696	40 × 40	1.00	0.90	DBN7-H9	–	–	–	–	–	–	–	–

Notes 1. Low thermal resistance type (using copper material)

2. A staggered arrangement

Remarks 1. – : Not available

2. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: D90* = D90T and D90C

3. HSP: Heat spreader

Table 2-2. Package List (2/3)

Package					E16*	E54*	E80*	F18*	F44*	F70*	G08*	G34*
Type	No. of Pins	External Dimensions (mm)	Lead Pitch (mm)	Resin Thickness (mm)								
QFP	44	10 × 10	0.80	2.70	–	–	–	–	–	–	–	–
	52	14 × 14	1.00	2.70	–	–	–	–	–	–	–	–
	64	14 × 20	1.00	2.70	–	–	–	–	–	–	–	–
	100	14 × 20	0.65	2.70	–	–	–	–	–	–	–	–
	120	28 × 28	0.80	3.70	–	–	–	–	–	–	–	–
	160	28 × 28	0.65	3.70	–	–	–	–	–	–	–	–
QFP (fine pitch)	100	14 × 14	0.50	1.45	C	C	C	C	C	C	–	–
	120	20 × 20	0.50	2.70	C	C	C	C	C	C	C	C
	144	20 × 20	0.50	2.70	C	C	C	C	C	C	C	C
	160	24 × 24	0.50	2.70	C	C	C	C	C	C	C	–
	176	24 × 24	0.50	2.70	C	C	C	–	–	–	–	–
	144 Note 1	20 × 20	0.50	2.70	C	C	C	C	C	–	–	–
	160 Note 1	24 × 24	0.50	2.70	C	C	C	C	C	C	C	C
	176 Note 1	24 × 24	0.50	2.70	C	C	C	C	C	C	C	C
	208 Note 1	28 × 28	0.50	3.20	T	T	T	C	C	C	C	C
	240 Note 1	32 × 32	0.50	3.20	T	T	T	T	C	T	T	T
	256 Note 1	28 × 28	0.40	3.20	–	T	T	T	T	T	–	–
	304 Note 1	40 × 40	0.50	3.70	–	–	–	T	T	T	T	T
QFP (fine pitch) with HSP	160 Note 1	24 × 24	0.50	2.70	C	C	C	C	C	C	–	–
	176 Note 1	24 × 24	0.50	2.70	–	C	C	C	C	C	C	C
	208 Note 1	28 × 28	0.50	3.20	–	–	–	C	C	C	C	C
	240 Note 1	32 × 32	0.50	3.20	–	–	–	–	–	–	–	–
	304 Note 1	40 × 40	0.50	3.70	–	–	–	–	–	–	–	–
TQFP	64 Note 1	10 × 10	0.50	1.00	–	–	–	–	–	–	–	–
	80	12 × 12	0.50	1.05	–	–	–	–	–	–	–	–
	100 Note 1	14 × 14	0.50	1.00	C	–	–	–	–	–	–	–
	120 Note 1	14 × 14	0.40	1.00	C	C	C	–	–	–	–	–
LQFP	144 Note 1	20 × 20	0.50	1.40	C	C	C	C	C	C	C	C
	160 Note 1	24 × 24	0.50	1.40	C	C	C	C	C	–	–	–
	176 Note 1	24 × 24	0.50	1.40	C	C	C	–	–	–	–	–
	208 Note 1	28 × 28	0.50	1.40	–	C	C	C	C	–	–	–
Plastic BGA	225	27 × 27	1.50	1.53	T	T	T	T	T	T	T	T
	256	27 × 27	1.27	1.53	T	T	T	T	T	T	T	T
	313	35 × 35	2.54 Note 2	1.73	C	C	T	T	T	T	T	T
	352	35 × 35	1.27	1.73	–	–	–	–	C	T	T	T
Tape BGA	256	27 × 27	1.27	0.80	T	T	T	T	T	T	T	–
	352	35 × 35	1.27	0.80	C	C	C	T	T	T	T	T
	420	35 × 35	1.27	0.80	C	C	C	C	C	C	C	T
	500	40 × 40	1.27	0.80	–	–	–	C	C	C	C	C
	576	40 × 40	1.27	0.80	–	–	–	–	–	–	–	C
	696	40 × 40	1.00	0.90	–	–	–	–	–	–	–	–

Notes 1. Low thermal resistance type (using copper material)

2. A staggered arrangement

Remarks 1. – : Not available

2. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: D90* = D90T and D90C

3. HSP: Heat spreader

Table 2-2. Package List (3/3)

Package					G72*	H10*	H49*	H87*	J26*	J51*	K15*	K92*
Type	No. of Pins	External Dimensions (mm)	Lead Pitch (mm)	Resin Thickness (mm)								
QFP	44	10 × 10	0.80	2.70	–	–	–	–	–	–	–	–
	52	14 × 14	1.00	2.70	–	–	–	–	–	–	–	–
	64	14 × 20	1.00	2.70	–	–	–	–	–	–	–	–
	100	14 × 20	0.65	2.70	–	–	–	–	–	–	–	–
	120	28 × 28	0.80	3.70	–	–	–	–	–	–	–	–
	160	28 × 28	0.65	3.70	–	–	–	–	–	–	–	–
QFP (fine pitch)	100	14 × 14	0.50	1.45	–	–	–	–	–	–	–	–
	120	20 × 20	0.50	2.70	C	C	C	C	–	–	–	–
	144	20 × 20	0.50	2.70	C	C	C	C	–	–	–	–
	160	24 × 24	0.50	2.70	–	–	–	–	–	–	–	–
	176	24 × 24	0.50	2.70	–	–	–	–	–	–	–	–
	144[Note 1]	20 × 20	0.50	2.70	–	–	–	–	–	–	–	–
	160[Note 1]	24 × 24	0.50	2.70	C	C	C	C	C	C	C	C
	176[Note 1]	24 × 24	0.50	2.70	C	C	C	C	C	C	C	C
	208[Note 1]	28 × 28	0.50	3.20	C	C	C	C	C	C	C	C
	240[Note 1]	32 × 32	0.50	3.20	C	C	C	C	C	C	C	C
	256[Note 1]	28 × 28	0.40	3.20	–	–	–	–	–	–	–	–
	304[Note 1]	40 × 40	0.50	3.70	T	T	T	C	C	T	C	C
QFP (fine pitch) with HSP	160[Note 1]	24 × 24	0.50	2.70	–	–	–	–	–	–	–	–
	176[Note 1]	24 × 24	0.50	2.70	C	C	C	C	C	–	–	–
	208[Note 1]	28 × 28	0.50	3.20	C	C	C	C	C	C	C	C
	240[Note 1]	32 × 32	0.50	3.20	–	–	C	C	C	C	C	C
	304[Note 1]	40 × 40	0.50	3.70	–	–	–	–	–	T	C	C
TQFP	64[Note 1]	10 × 10	0.50	1.00	–	–	–	–	–	–	–	–
	80	12 × 12	0.50	1.05	–	–	–	–	–	–	–	–
	100[Note 1]	14 × 14	0.50	1.00	–	–	–	–	–	–	–	–
	120[Note 1]	14 × 14	0.40	1.00	–	–	–	–	–	–	–	–
LQFP	144[Note 1]	20 × 20	0.50	1.40	C	C	C	–	–	–	–	–
	160[Note 1]	24 × 24	0.50	1.40	–	–	–	–	–	–	–	–
	176[Note 1]	24 × 24	0.50	1.40	–	–	–	–	–	–	–	–
	208[Note 1]	28 × 28	0.50	1.40	–	–	–	–	–	–	–	–
Plastic BGA	225	27 × 27	1.50	1.53	–	–	–	–	–	–	–	–
	256	27 × 27	1.27	1.53	–	–	–	–	–	–	–	–
	313	35 × 35	2.54[Note 2]	1.73	T	T	T	T	T	T	T	T
	352	35 × 35	1.27	1.73	T	T	T	T	T	T	T	T
Tape BGA	256	27 × 27	1.27	0.80	–	–	–	–	–	–	–	–
	352	35 × 35	1.27	0.80	T	T	T	T	T	T	T	T
	420	35 × 35	1.27	0.80	T	T	T	T	T	T	T	T
	500	40 × 40	1.27	0.80	C	C	T	T	T	T	T	T
	576	40 × 40	1.27	0.80	C	C	C	C	C	C	T	T
	696	40 × 40	1.00	0.90	–	–	–	C	C	C	C	C

Notes 1. Low thermal resistance type (using copper material)

2. A staggered arrangement

Remarks 1. – : Not available

2. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: D90* = D90T and D90C

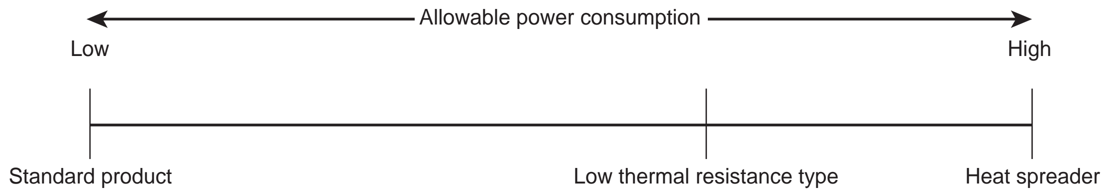
3. HSP: Heat spreader

2.3 Power Consumption Check

Even though CMOS cell-based ICs are known for their low power consumption, they actually consume a considerable amount of power when operated at a high speed (such as 30 MHz or higher). The temperature of the LSI (chip) rises in proportion to the amount of power consumed. If the chip temperature rises too much, the product's reliability may decline, so be sure to keep the LSI's power consumption at or below the rated limit value.

Restrictions on power consumption vary according to the package. To improve the allowable power consumption ratings, the following type of QFP package is available in addition to the normal one: low thermal resistance type or with heat spreader. Figure 2-1 shows the relationship between allowable power consumption and various types of QFPs. For details, see **4.3 Power Consumption**.

Figure 2-1. Relationship between Allowable Power Consumption and Various QFPs



2.4 Pin Layout

The positions of each package's power supply pins and NC pins are determined in advance. Note the following cautions when determining the pin layout.

It may be necessary to expand (add) power supply pins depending on considerations such as the number of simultaneous output operation pins. For details, see **4.6 Simultaneous Switching Limits of Output Buffers**.

Analog-only power supply pins are required when implementing analog macros (which are still under development), so be sure to contact NEC in this case.

Cautions regarding pin layout

(1) Clock pins, control pins (set, reset), etc.

Position these pins near the ground (GND) pin since they are easily affected by noise.

(2) Output pins

Separate the output pins as far as possible from the clock pins and other pins that are easily affected by noise. Groups of output pins that contain several simultaneous operation pins should be positioned between V_{DD} and GND pins.

(3) NC (No Connection) pins

When mounting a cell-based IC on a PC board, do not use any NC pins as a signal relay pin.

Even a pin that is not used may actually be connected to a pad on the chip. When mounting a cell-based IC on a PC board, connect these pins to a ground (GND) or V_{DD} pin.

(4) I/O pins for scan path

If the scan path test method will be used, be sure to specify I/O pins for the scan path using the pin numbers specified as the correct layout for the particular package, since the test pin layout for each package size has already been determined. (For details, see the **Design For Test User's Manual (A14375E)**.)

(5) 5-V buffer

The CB-9 Family's VX/VM type includes a 5-V buffer. Note that a latch-up may occur if this 5-V buffer is adjacent to the TTL 5-V tolerant buffer.

Therefore, when these two buffers are adjacent, insert a 3.3-V power supply pin, a GND pin, an LVTTL buffer, or an NC pin.

(6) Layout of I/O buffers using two I/O areas (pads)

In the CB-9 Family's VX/VM type, two I/O areas (pads) are used for various types of interface blocks. The pin layout for these buffers is determined according to the step size and package. When using either of the following buffers, be sure to contact NEC to confirm the pin numbers that can be used for the layout.

(a) 5V interface 18 mA/24 mA output buffers (under development)

If the 5V interface 18 mA/24 mA output/bidirectional buffers are laid out at pins that do not enable both the CMOS type and TTL type, the pins immediately to the right of the allocated pin must be physical NC pins. Accordingly, this layout does not work if the pin to the right is either a V_{DD} or GND pin. Note that this also reduces the number of available signal pins.

(b) GTL interface output/bidirectional buffers (under development)

These output/bidirectional buffers are used to implement high-speed signal transmission using low-amplitude signals, and therefore extra care must be taken regarding any noise that is generated on the GND line. When a GTL buffer is implemented on a cell-based IC, one GND pin must be laid out adjacent to each pair of GTL pins. Therefore, one side of the two I/O cells used for these blocks should be connectable to a GND pin. However, this severely restricts layout flexibility. In addition, the set of GTL pins should be laid out with three GND pins on each side, or a similar measure should be taken to provide adequate separation from normal output buffer noise.

Since a reference voltage is required for the GTL interface, there must be a reference voltage pin. In addition, an input enable pin is required to avoid static current consumption in the input section.

List of relevant blocks

BG0W, EGTL

(7) Layout of oscillator block pins (under development)

For a description of the possible layout positions for the oscillator block, see **APPENDIX A LISTS OF INPUT/ OUTPUT PINS AND POWER SUPPLY PINS IN PACKAGES**.

Do not layout pins (such as reset pins) next to the oscillator pins if they are susceptible to operation errors caused by ambient noise.

(8) Layout of analog macro

When implementing an analog macro, NC pins may be used depending on the macro's type. Contact NEC before determining the layout of any analog macros.

(9) Addition of mode setting pin

The three modes shown in the table below can be controlled by using the FM11 and FM12 mode setting interface blocks. For mode setting, add two dedicated pins.

FM11	FM21	Mode	Target Simulation
0	0	Normal mode (actual operation mode)	For user use
0	1	LFT (I_{OL}, I_{OH} MIN.) test mode[Note 1]	For NEC use (User use prohibited)
1	0	I_{DD} test mode[Note 2]	For NEC use (User use prohibited)
1	1	Setting prohibited	Setting prohibited

Notes 1. LFT test mode: This mode is used to minimize the output current for target devices that are simultaneously ON during product shipment testing.

2. I_{DD} test mode: Test mode in which pull-up/pull-down resistors are disconnected to permit accurate measurement of the static current consumption during product shipment testing.

2.5 I/O Interface

2.5.1 Input block types

Signal level
3.3 V
5.0 V

Function
Buffer
Fail safe

Input format
Normal
Schmitt trigger

Pull-up/pull-down resistor
No resistor
With 50-kΩ pull-up resistor
With 5-kΩ pull-up resistor
With 50-kΩ pull-down resistor

Signal level
GTL Note

Function
Buffer

Input format
Normal

Note Under development

Three types of input interface level blocks are described below.

<1> 3.3-V interface level blocks
These blocks are used to connect to LSIs having a 3.3-V power voltage level. Some of these blocks include a fail-safe function. The fail-safe blocks also include an overvoltage protection function so that when the cell-based IC's power voltage is off, power will not be supplied to the cell-based IC even if there is signal input.

<2> 5-V interface level blocks
These blocks are used to connect to LSIs having a 5-V power voltage level.

<3> GTL (under development)
GTL (Gunning Transceiver Logic; low-amplitude interface) is a differential circuit similar to an ECL (Emitter-Coupled Logic) circuit, and therefore it is able to capture ultra high-speed signals.

2.5.2 Output block types

Signal level	Function	Output format	Pull-up/pull-down resistor	Load drive capacity I_{OL}	
3.3 V	Buffer	LVTTL	No resistor	$I_{OL} = I_{OH}$	1.0 mA
5.0 V	3-State	Low noise	With 50-kΩ pull-up resistor		2.0 mA
	Open drain	TTL	With 5-kΩ pull-up resistor		3.0 mA
		CMOS	With 50-kΩ pull-down resistor		6.0 mA
			With bus holder		9.0 mA
					12.0 mA
					18.0 mA
					24.0 mA

Signal level	Function	Output format	Pull-up/pull-down resistor	Load drive capacity I_{OL}	
GTL Note	Open drain	Normal	No resistor		40.0 mA Note

Note Under development

Three types of output interface level blocks are described below.

<1> 3.3-V interface level blocks

These blocks are used to connect to LSIs having a 3-V LVTTL interface.

<2> 5-V interface level blocks

These blocks are used to connect to LSIs having a 5-V power voltage level. There are two types: CMOS level and TTL level. The 5-V interface supports this block in VM Type devices. However, if using a TTL-level interface, it is possible to use not only the VM type's TTL-level interface buffer but also the VX type's TTL 5-V tolerant interface buffer.

<3> GTL (under development)

The GTL's output section is an enabled open drain buffer.

In addition, a low noise buffer for noise suppression and a high-speed buffer are also included. The output drive capacity is the same as for I_{OL} and I_{OH} for the following types.

- LVTTL interface buffer (6 types)
- TTL 5-V tolerant interface buffer (6 types)
- 5-V CMOS-level interface (VM type only)
- TTL interface (VM type only)
- Low-noise buffer

In CMOS circuits, when the input potential is not fixed (i.e., is "floating"), an excessive through current can enter, allowing noise signals into the circuit, which can cause operation faults. Enable buffers having pull-up or pull-down resistor or buffers with bus holders to be used for open pins on the PC board.

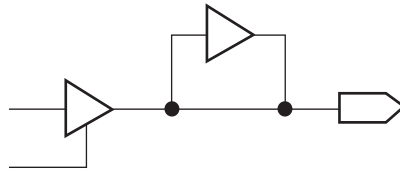
<4> Buffer with bus holder

The CB-9 Family's VX/VM types include buffers with bus holders as means of dealing with high-impedance output. These buffers with bus holders include a hold circuit (bus holder) that retains the value prior to high impedance, even when the high impedance is from a three-state output buffer or bidirectional buffer.

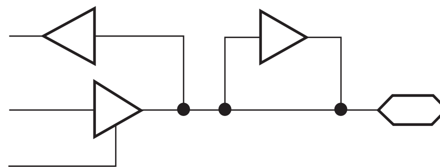
Buffers in bus holders have little drive power that it cannot be used to drive the bus. Consequently, do not pull-up or pull-down a bus that uses buffers with bus holders. In addition, signals may invert by the influence of noise.

Figure 2-2. Buffers with Bus Holders

(a) Three-state buffer with bus holder



(b) Bidirectional buffer with bus holder



CHAPTER 3 PRODUCT SPECIFICATIONS

The CB-9 Family's VX/VM type devices include an I/O interface block that enables them to be connected not only to LSIs that have 3.3-V power sources but also to LSIs that have 5-V power sources.

The product ratings of CB-9 Family VX/VM type devices are described below.

3.1 Terminology

Table 3-1. Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Input current	I_I	Indicates absolute tolerance values to prevent latchups when a current is applied to an input pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is applied to the device.

Table 3-2. Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations to occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	This voltage, which is applied to the input pins of the cell-based IC, indicates the high level state voltage for normal operation of the input buffer. • If a voltage that is equal to or greater than the MIN. value is applied, the input voltage is guaranteed as a high level voltage.
Low-level input voltage	V_{IL}	This voltage, which is applied to the input pins of the cell-based IC, indicates the low level state voltage for normal operation of the input buffer. • If a voltage that is equal to or less than the MAX. value is applied, the input voltage is guaranteed as a low level voltage.
Positive trigger voltage	V_P	This is the input level at which the output level is inverted when the input to a cell-based IC is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	This is the input level at which the output level is inverted when the input to a cell-based IC is changed from the high-level side to the low-level side.
Hysteresis voltage	V_H	This is the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{ri}	This is the limit value for the time period when an input voltage applied to a cell-based IC rises from 10% to 90%.
Input fall time	t_{fi}	This is the limit value for the time period when an input voltage applied to a cell-based IC falls from 90% to 10%.

Table 3-3. Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Static current consumption	I_{DDS}	This is the current that flows from the power supply pins when the rated power supply voltage is being applied without any changes in the input voltage or the output pin voltage.
Off-state output leakage current	I_{OZ}	When a 3-state output has high impedance, this is the current that flows from the power supply pins when the rated power supply voltage is applied.
Output short circuit current	I_{OS}	When output is at high level, this is the current that flows when the output pins are shorted (to GND pins).
Input leak current	I_I	This is the current that flows via the input pin when a voltage is applied to that pin.
Low-level output current	I_{OL}	This is the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	This is the current that flows from the output pins when the rated high-level output voltage is being applied.
Low-level output voltage	V_{OL}	This is the output voltage when at low level and when the output pin is open.
High-level output voltage	V_{OH}	This is the output voltage when at high level and when the output pin is open.

3.2 Absolute Maximum Ratings

Table 3-4. Absolute Maximum Ratings

Parameter		Symbol	Conditions	Ratings	Unit
Power supply voltage		V_{DD}			
	2.0 V type Note 1			–0.5 to +4.6	V
	3.3 V type			–0.5 to +4.6	V
	5.0 V type Note 2			–0.5 to +6.0	V
I/O voltage		V_I/V_O			
	LVTTL buffer		$V_I/V_O < V_{DD} + 0.5$ V	–0.5 to +4.6	V
	TTL 5-V tolerant buffer		$V_I/V_O < V_{DD} + 3.0$ V	–0.5 to +6.6	V
	5-V buffer Note 2		$V_I/V_O < V_{DD} + 0.5$ V	–0.5 to +6.0	V
Output current		I_O	I_{OL} = 1 mA	3	mA
			I_{OL} = 2 mA	7	mA
			I_{OL} = 3 mA	10	mA
			I_{OL} = 6 mA	20	mA
			I_{OL} = 9 mA	30	mA
			I_{OL} = 12 mA	40	mA
			I_{OL} = 18 mA	60	mA
			I_{OL} = 24 mA	75	mA
Operating temperature		T_A		–40 to +85	°C
Storage temperature		T_{stg}		–65 to +150	°C

Notes 1. This can only be used in the VX type; it cannot be used in the VM type.

2. This can only be used in the VM type; it cannot be used in the VX type.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

3.3 Recommended Operating Conditions

Table 3-5. Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	2.0-V power supply Note 1	1.8	2.0	2.2	V
		3.3-V power supply	3.0	3.3	3.6	V
		5.0-V power supply, CMOS level	4.5	5.0	5.5	V
		5.0-V power supply, TTL level	4.75	5.00	5.25	V
Negative trigger voltage	V_N	LVTTL buffer	0.6		1.8	V
		TTL 5-V tolerant buffer	0.6		1.8	V
		CMOS 5-V buffer Notes 2, 3	0.6		3.1	V
		TTL buffer Notes 2, 4	0.6		1.8	V
Positive trigger voltage	V_P	LVTTL buffer	1.2		2.4	V
		TTL 5-V tolerant buffer	1.2		2.4	V
		CMOS 5-V buffer Notes 2, 3	1.8		4.0	V
		TTL buffer Notes 2, 4	1.2		2.4	V
Hysteresis voltage	V_H	LVTTL buffer	0.3		1.5	V
		TTL 5-V tolerant buffer	0.3		1.5	V
		CMOS 5-V buffer Notes 2, 3	0.3		1.5	V
		TTL buffer Notes 2, 4	0.3		1.5	V
Low-level input voltage	V_{IL}	LVTTL buffer	0		0.8	V
		TTL 5-V tolerant buffer	0		0.8	V
		CMOS 5-V buffer Note 2	0		0.3 V_{DD}	V
		TTL buffer Note 2	0		0.8	V
		3.3-V PCI buffer	0		0.3 V_{DD}	V
		5-V PCI buffer Note 5	0		0.8	V
High-level input voltage	V_{IH}	LVTTL buffer	2.0		V_{DD}	V
		TTL 5-V tolerant buffer	2.0		5.5	V
		CMOS 5-V buffer Note 2	0.7 V_{DD}		V_{DD}	V
		TTL buffer Note 2	2.2		V_{DD}	V
		3.3-V PCI buffer	0.5 V_{DD}		V_{DD}	V
		5-V PCI buffer Note 5	2.0		V_{DD}	V
Input rise/fall times (Normal input)	t_r		0		200	ns
	t_f		0		200	ns
Input rise/fall times (Schmitt input)	t_r		0		10	ms
	t_f		0		10	ms

Notes 1. VX type only

2. VM type only

3. CMOS-Schmitt

4. TTL-Schmitt

5. 5-V PCI interface buffer (V_{DD} = 5 V ±5%)

Remark Use a Schmitt trigger input buffer in cases where input of a dull signal with slow rise/fall time causes operation faults due to noise in the signal line. When determining the pin layout, note that fluctuation in the power supply line, such as caused by simultaneous operation of output buffers, may reduce the performance of Schmitt trigger input buffers.

3.4 DC Characteristics

Table 3-6. DC Characteristics (V_{DD} = 3.3±0.3 V, T_A = –40 to +85°C) (1/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Static current consumption Note 1	I_{DDS}	$V_I = V_{DD}$ or GND	B60 to E54 Note 2			200	μA
			E80 to H10 Note 2			400	μA
			H49 to K92 Note 2			800	μA
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or GND				±10	μA
Output short circuit current Note 3	I_{OS}					–250	μA
Input leakage current (3.3 V)	I_I						
Normal input		$V_I = V_{DD}$ or GND			$\pm10^{-5}$	±10	μA
3.3-V PCI input		$V_I = V_{DD}$ or GND				±10	μA
With pull-up resistor (50 kΩ)		V_I = GND		–28	–83	–191	μA
With pull-up resistor (5 kΩ)		V_I = GND		–281	–703	–1895	μA
With pull-down resistor (50 kΩ)		$V_I = V_{DD}$		28	83	191	μA
Input leakage current (5 V) Note 4	I_I						
Normal input		$V_I = V_{DD}$ or GND			$\pm10^{-4}$	±10	μA
5-V PCI input Note 5		V_I = 2.7 V or 0.5 V				±70.0	μA
With pull-up resistor (50 kΩ)		V_I = GND		–36	–145	–308	μA
With pull-up resistor (5 kΩ)		V_I = GND		–300	–1163	–2750	μA
With pull-down resistor (50 kΩ)		$V_I = V_{DD}$		45	116	367	μA

Notes 1. The static current consumption increases when an interface block or oscillator with an on-chip pull-up/pull-down resistor is used.

2. Step size

3. The output short current time is one second or less and is only for one pin on the LSI.

4. VM type only (V_{DD} = 5 V ± 10%)

5. 5-V PCI input (V_{DD} = 5 V ±5%)

Remark The "+" and "–" symbols in the above table indicate the direction of current flow. "+" indicates a current flowing into the device and "–" indicates a current flowing from the device.

Table 3-6. DC Characteristics (V_{DD} = 3.3±0.3 V, T_A = –40 to +85°C) (2/4)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-level output current			I_{OL}					
	LVTTL buffer							
		3 mA type		V_{OL} = 0.4 V	3			mA
		6 mA type			6			mA
		9 mA type			9			mA
		12 mA type			12			mA
		18 mA type			18			mA
		24 mA type			24			mA
	TTL 5-V tolerant buffer							
		1 mA type			1			mA
		2 mA type			2			mA
		3 mA type			3			mA
		6 mA type			6			mA
		9 mA type			9			mA
		12 mA type			12			mA
★		18 mA type			18			mA
★		24 mA type			24			mA
	5-V buffer Note							
		1 mA type			1			mA
		2 mA type			2			mA
		3 mA type			3			mA
		6 mA type			6			mA
		9 mA type			9			mA
		12 mA type			12			mA
		18 mA type			18			mA

Note VM type only (V_{DD} = 5 V ± 10%)

Table 3-6. DC Characteristics (V_{DD} = 3.3±0.3 V, T_A = –40 to +85°C) (3/4)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output current			I_{OH}					
	LVTTL buffer							
		3 mA type		V_{OH} = 2.4 V	–3			mA
		6 mA type			–6			mA
		9 mA type			–9			mA
		12 mA type			–12			mA
		18 mA type			–18			mA
		24 mA type			–24			mA
	TTL 5-V tolerant buffer							
		1 mA type			–1			mA
		2 mA type			–1			mA
		3 mA type			–2			mA
		6 mA type			–2			mA
		9 mA type			–2			mA
		12 mA type			–2			mA
★		18 mA type			–2			mA
★		24 mA type			–2			mA
	5-V buffer Note			V_{OH} = V_{DD} – 0.4 V				
		1 mA type			–1			mA
		2 mA type			–2			mA
		3 mA type			–3			mA
		6 mA type			–6			mA
		9 mA type			–9			mA
		12 mA type			–12			mA
		18 mA type			–18			mA

Note VM type only (V_{DD} = 5 V ± 10%)

Remark The "+" and "–" symbols in the above table indicate the direction of current flow. "+" indicates a current flowing into the device and "–" indicates a current flowing from the device.

Table 3-6. DC Characteristics (V_{DD} = 3.3±0.3 V, T_A = –40 to +85°C) (4/4)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-level output voltage		V_{OL}					
	LVTTL buffer		I_{OL} = 0 mA			0.1	V
	TTL 5-V tolerant buffer					0.1	V
	5-V buffer Note 1					0.1	V
	3.3-V PCI buffer		I_{OL} = 1500 mA			0.1 V_{DD}	V
	5-V PCI buffer Note 2		I_{OL} = 3 mA, 6 mA			0.55	V
High-level output voltage		V_{OH}					
	LVTTL buffer		I_{OH} = 0 mA	V_{DD}–0.1			V
	TTL 5-V tolerant buffer			V_{DD}–0.2			V
	5-V buffer Note 1			V_{DD}–0.1			V
	3.3-V PCI buffer		I_{OH} = –500 mA	0.9 V_{DD}			V
	5-V PCI buffer Note 2		I_{OH} = –2 mA	2.4			V

Notes 1. VM type only (V_{DD} = 5 V ±10%)

2. VM type only (V_{DD} = 5 V ±5%)

3.5 Pull-up/Pull-down Resistance Values

Table 3-7. Pull-up/Pull-down Resistance Values (V_{DD} = 3.3±0.3 V, T_A = –40 to +85°C)

Parameter	Library Expression	MIN.	TYP.	MAX.	Unit
Pull-up resistor	5 kΩ	1.9	4.7	10.7	kΩ
	50 kΩ	18.9	39.8	107.1	kΩ
Pull-down resistor	50 kΩ	18.9	39.8	107.1	kΩ

Table 3-8. Pull-up/Pull-down Resistance Values (V_{DD} = 5.0±0.5 V, T_A = –40 to +85°C)

Parameter	Library Expression	MIN.	TYP.	MAX.	Unit
Pull-up resistor	5 kΩ	2.0	4.3	15.0	kΩ
	50 kΩ	17.9	34.6	125.0	kΩ
Pull-down resistor	50 kΩ	15.0	43.4	100.0	kΩ

3.6 AC Characteristics

Table 3-9 lists AC characteristics.

In the table, the toggle frequency (f_{tog}) is the value at the maximum operating clock frequency ($f_{MAX.}$) of the toggle flip-flop for internal cells. In actual circuits, note that the maximum operating clock frequency ($f_{MAX.}$) varies according to the circuit configuration.

Table 3-9. AC Characteristics (T_A = –40 to +85°C) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Toggle frequency	f_{tog}	Internal toggle flip-flop (fan-out 2, 3.3 V)	850			MHz
		Internal toggle flip-flop (fan-out 2, 2.0 V)	380			MHz
Propagation delay time	t_{PD}	Internal gate (fan-out 2, standard wiring length, 2.0 V)		296		ps
		Internal gate (power gate, fan-out 2, standard wiring length, 2.0 V)		207		ps
		Internal gate (fan-out 2, standard wiring length, 3.3 V)		155		ps
		Internal gate (power gate, fan-out 2, standard wiring length, 3.3 V)		114		ps
		LVTTL input buffer (fan-out 2, standard wiring length)		169		ps
		LVTTL output buffer (C_L = 15 pF, I_{OL} = 18 mA)		864		ps
		TTL 5-V tolerant input buffer (fan-out 2, standard wiring length)		253		ps
		TTL 5-V tolerant output buffer (C_L = 15 pF, I_{OL} = 18 mA)		952		ps
		LVTTL input buffer (V_{DD} = 2.0 V, fan-out 2, standard wiring length)		211		ps
		LVTTL output buffer (V_{DD} = 2.0 V, C_L = 15 pF, I_{OL} = 18 mA)		1231		ps
		5-V input buffer (fan-out 2, standard wiring length)		690		ps
		5-V output buffer (C_L = 15 pF, I_{OL} = 18 mA)		2045		ps
Output rise time	t_r	LVTTL buffer (C_L = 15 pF, I_{OL} = 9 mA)		1915		ps
		TTL 5-V tolerant buffer (C_L = 15 pF, I_{OL} = 9 mA)		2777		ps
		LVTTL buffer (V_{DD} = 2.0 V, C_L = 15 pF, I_{OL} = 9 mA)		1815		ps
		5-V buffer (C_L = 15 pF, I_{OL} = 9 mA)		1601		ps

Table 3-9. AC Characteristics (T_A = –40 to +85°C) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output fall time	t_f	LVTTL buffer (C_L = 15 pF, I_{OL} = 9 mA)		1337		ps
		TTL 5-V tolerant buffer (C_L = 15 pF, I_{OL} = 9 mA)		1675		ps
		LVTTL buffer (V_{DD} = 2.0 V, C_L = 15 pF, I_{OL} = 9 mA)		1205		ps
		5-V buffer (C_L = 15 pF, I_{OL} = 9 mA)		1583		ps

3.7 Pin Capacitance

The pin capacitance values include the interface block capacitance and the package's own capacitance. Table 3-10 lists the capacitance values (C_P) of each package, and Table 3-11 lists the interface block capacitance values (C_B).

Pin capacitance C_T = Interface block capacitance C_B + Package capacitance C_P

Table 3-10. Package Capacitance (C_P) (V_{DD} = 0 V, T_A = 25°C) (1/2)

Package		Lead Pitch (mm)	Nominal Size (mm)	C_P (pF)
QFP	44 pin	0.80	10 × 10	
	52 pin	1.00	14 × 14	
	64 pin	1.00	14 × 20	
	100 pin	0.65	14 × 20	
	120 pin	0.80	28 × 28	
	160 pin	0.65	28 × 28	
	160 pin Note 1	0.65	28 × 28	
QFP (fine pitch)	100 pin	0.50	14 × 14	1.0
	120 pin	0.50	20 × 20	1.4
	144 pin	0.50	20 × 20	1.3
	160 pin	0.50	24 × 24	
	176 pin	0.50	24 × 24	
	144 pin Note 1	0.50	20 × 20	
	160 pin Note 1	0.50	24 × 24	
	176 pin Note 1	0.50	24 × 24	
	208 pin Note 1	0.50	28 × 28	1.9
	240 pin Note 1	0.50	32 × 32	2.5
	256 pin Note 1	0.40	28 × 28	
	304 pin Note 1	0.50	40 × 40	2.8
QFP (fine pitch) with HSP	160 pin Note 1	0.50	24 × 24	1.9
	176 pin Note 1	0.50	24 × 24	
	208 pin Note 1	0.50	28 × 28	2.3
	240 pin Note 1	0.50	32 × 32	
	304 pin Note 1	0.50	40 × 40	
TQFP	64 pin Note 1	0.50	10 × 10	
	80 pin	0.50	12 × 12	
	100 pin Note 1	0.50	14 × 14	0.9
	120 pin Note 1	0.40	14 × 14	

Table 3-10. Package Capacitance (C_P) (V_{DD} = 0 V, T_A = 25°C) (2/2)

Package		Lead Pitch (mm)	Nominal Size (mm)	C_P (pF)
LQFP	144 pin[Note 1]	0.50	20 × 20	
	160 pin[Note 1]	0.50	24 × 24	
	176 pin[Note 1]	0.50	24 × 24	
	208 pin[Note 1]	0.50	28 × 28	
Plastic BGA	225 pin	1.50	27 × 27	
	256 pin	1.27	27 × 27	
	313 pin	2.54[Note 2]	35 × 35	
	352 pin	1.27	35 × 35	
Tape BGA	256 pin	1.27	27 × 27	1.0
	352 pin	1.27	35 × 35	1.2
	420 pin	1.27	35 × 35	1.1
	500 pin	1.27	40 × 40	1.3
	576 pin	1.27	40 × 40	1.0
	696 pin	1.00	40 × 40	1.2

Notes 1. Low thermal resistance type.

2. A staggered arrangement

Remarks 1. Condition f = 1 MHz, 0V except pins to be measured.

2. Blanks are undefined.

Table 3-11. Interface Block Capacitance (C_B)

(a) Input buffer

Interface Level	$C_{B (MIN.)}$ (pF)		$C_{B (MAX.)}$ (pF)	
	Normal	With Failsafe	Normal	With Failsafe
LVTTL	4.0	2.0	6.0	4.0
5 V (VM type only)	8.0	–	10.0	–

Remark V_{DD} = 0 V, T_J = 25°C, f = 1 MHz

(b) Output buffer/bidirectional buffer

Interface Level		C_B (pF)							
		1 mA	2 mA	3 mA	6 mA	9 mA	12 mA	18 mA	24 mA
LVTTL	MIN.	–	–	4.0	4.0	4.0	4.0	4.0	4.0
	MAX.	–	–	6.0	6.0	6.0	6.0	6.0	6.0
TTL 5-V tolerant	MIN.	8.0	8.0	8.0	8.0	8.0	8.0	8.0	8.0
	MAX.	10.0	10.0	10.0	10.0	10.0	10.0	10.0	10.0
5 V (VM type only)	MIN.	–	–	8.0	8.0	8.0	8.0	8.0	8.0
	MAX.	–	–	10.0	10.0	10.0	10.0	10.0	10.0

Remark V_{DD} = 0 V, T_J = 25°C, f = 1 MHz

This chapter describes methods for estimating (calculating) power consumption, delay times, etc.

4.1 Estimation of Static Current Consumption

4.1.1 Estimation of static current consumption

A very slight amount of leakage current flows from the power supply to the GND in normal standby mode. If neither an input/output buffer with on-chip pull-up/pull-down resistor nor a 5-V output block are used, the static current consumption is equivalent to this leakage current. On the other hand, if an input/output buffer with on-chip pull-up/pull-down resistor is used, a resistance occurs according to the signal level, causing a DC current to flow, which increases the static current consumption.

In a TTL-level or CMOS-level 5-V output buffer, if the buffer is pulled up by a 5-V power supply, a current flows from the output pin into the LSI even when the output level is high (the CMOS 5-V output buffer is under development).

Use the following formula to calculate the static current consumption.

$$I_{DDS\,(max)} = I_L + I_{U50} \times \ell + I_{D50} \times m + I_{U5} \times n + I_{RT} \times p \ (\mu A)$$

I_L: Leakage current H49-K92 (800 μA)
E80-H10 (400 μA)
Step size other than above: (200 μA)

I_{U50}: Current consumption with 50-kΩ on-chip pull-up resistor (165 μA)

I_{D50}: Current consumption with 50-kΩ on-chip pull-down resistor (141 μA)

I_{U5}: Current consumption with 5-kΩ on-chip pull-up resistor (1305 μA)

I_{RT}: TTL 5-V tolerant output buffer output current
Output levels
Low level (V_{PU}/R_{PU} A)
High level (See **4.1.2 Output leakage current (I_R)**)
High impedance (14 μA)

ℓ: Number of buffers with low-level signals, among the I/O buffers with 50-kΩ on-chip pull-up resistor

m: Number of buffers with high-level signals, among the I/O buffers with 50-kΩ on-chip pull-down resistor

n: Number of buffers with low-level signals, among the I/O buffers with 5-kΩ on-chip pull-up resistor

p: Number of TTL 5-V tolerant output buffers pulled up by 5-V power supply

V_{PU}: 5-V pull-up voltage

R_{PU}: Pull-up resistor

If the circuit includes a three-state circuit, be sure to check for possible effects of off-state output leakage current.

4.1.2 Output leakage current (I_R)

The TTL 5-V tolerant output buffer is able to function as an interface for a 5-V LSI. In a TTL 5-V tolerant output buffer, if the buffer is pulled up by a 5-V power supply to flow an output DC current, the current flows into the LSI. Normally, use a VM type 5-V output buffer.

Figure 4-1. Flow Route of Output Leakage Current (I_R)

TTL 5-V tolerant output buffer

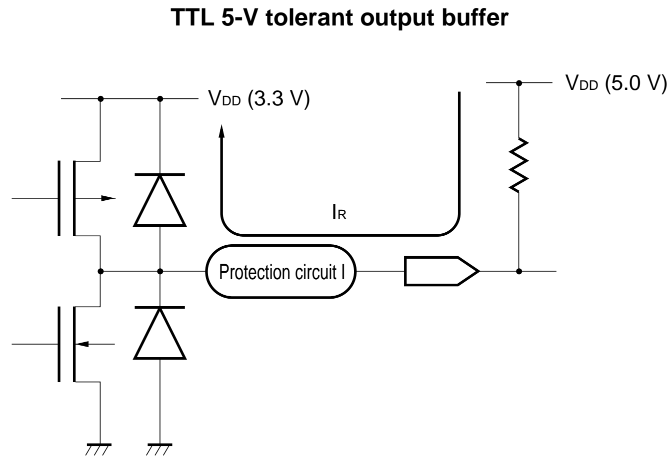
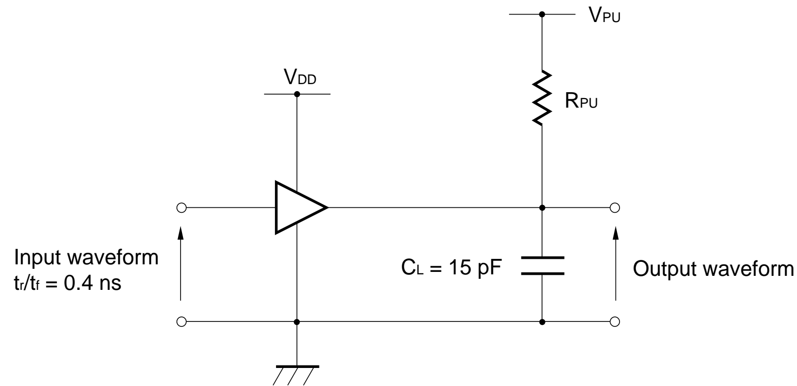


Figure 4-3 shows the output leakage current as determined by pull-up resistors. Figure 4-4 shows output waveforms for typical pull-up resistor values. Figure 4-2 describes the output waveform measurement circuit and various conditions.

Figure 4-2. Measurement Circuit

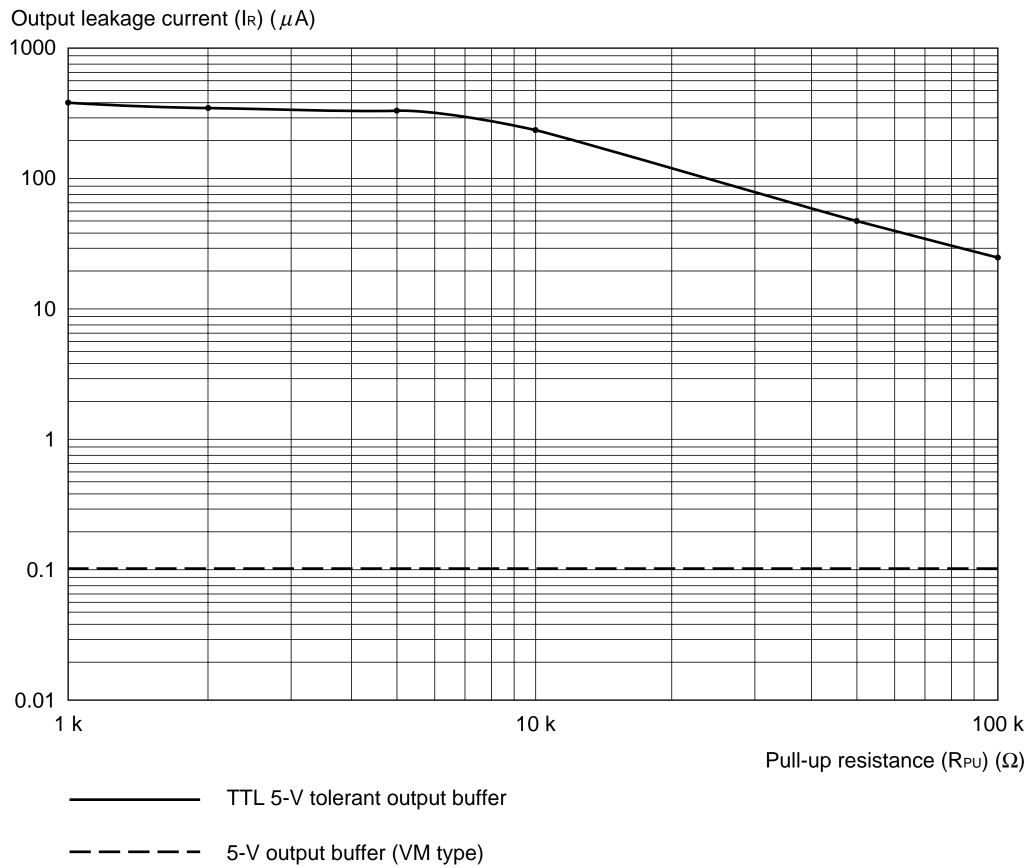


Measurement conditions

V_{DD} = 3.0 V T_J = 125°C

V_{PU} = 5.5 V

Figure 4-3. Output Leakage Current



Conditions

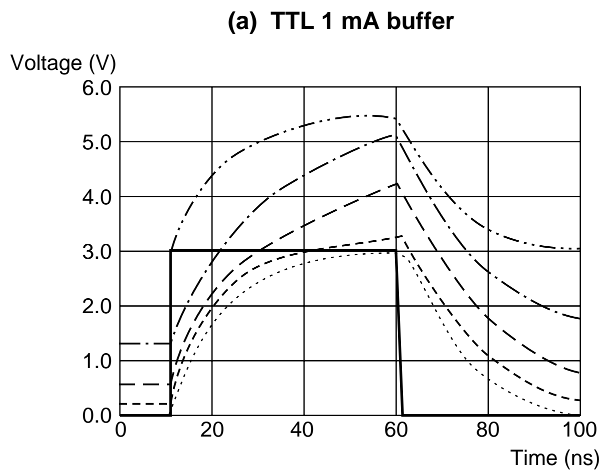
V_{DD} = 3.0 V, V_{PU} = 5.5 V

T_J = 125°C

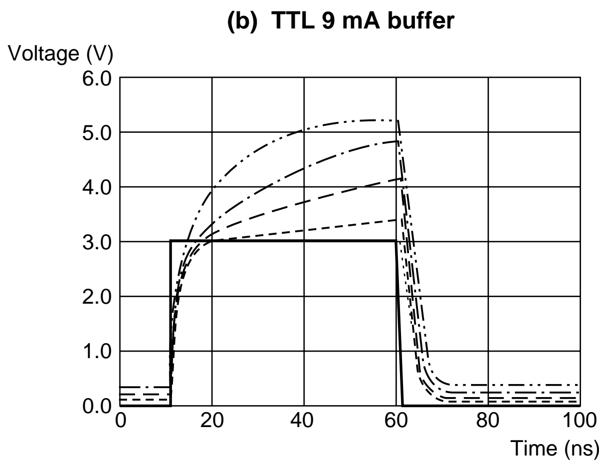
Worst case

Figure 4-4. 5-V Output Buffer Output Waveform

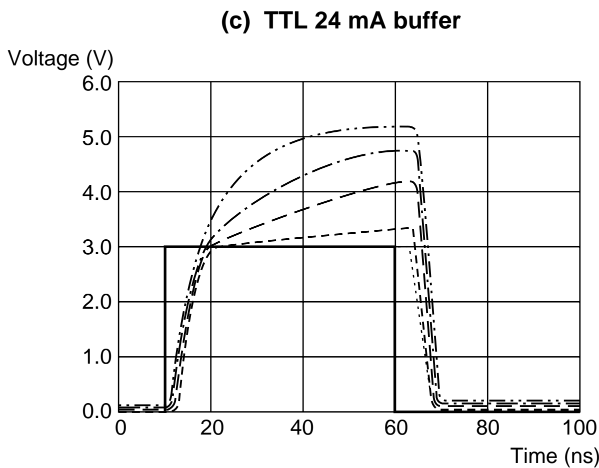
(a) TTL 1 mA buffer



(b) TTL 9 mA buffer



(c) TTL 24 mA buffer



Remarks 1.

- ———— Input waveform
- ············ No pull-up
- —··—··— R_{PU} = 0.5 kΩ
- —·—·— R_{PU} = 1.0 kΩ
- — — — — R_{PU} = 2.0 kΩ
- - - - - - - R_{PU} = 5.0 kΩ

2. Measurement conditions
V_{DD} = 3.0 V, T_J = 125˚C
V_{PU} = 5.5 V

4.2 Input Through Current

When the input voltage V_{IN} is the same as the power supply voltage V_{DD}, the input leakage current has the same value as described in **CHAPTER 3 PRODUCT SPECIFICATIONS**. However, if the input voltage is lower than the power supply voltage or if it is higher than the GND level, a current will pass from the P channel through the N channel. This type of current is called an input through current. Figure 4-5 shows an input through current for a 3.3-V interface in which V_{DD} = 3.6 V, Figure 4-6 shows an input through current for a 3.3-V Schmitt interface in which V_{DD} = 3.6 V, Figure 4-7 shows an input through current for a 5-V interface in which V_{DD} = 6.0 V, and Figure 4-8 shows an input through current (reference value) for a 5-V Schmitt interface in which V_{DD} = 6.0 V.

Figure 4-5. LVTTL Input Through Current (3.3-V Input)

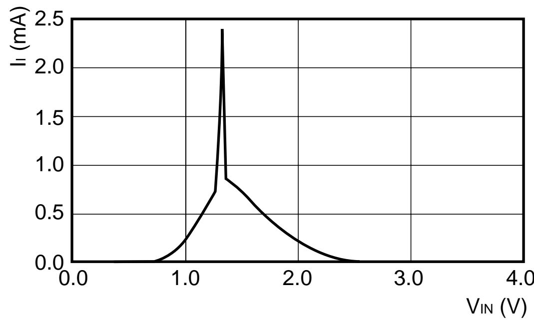


Figure 4-6. LVTTL Input Through Current (3.3-V Schmitt Input)

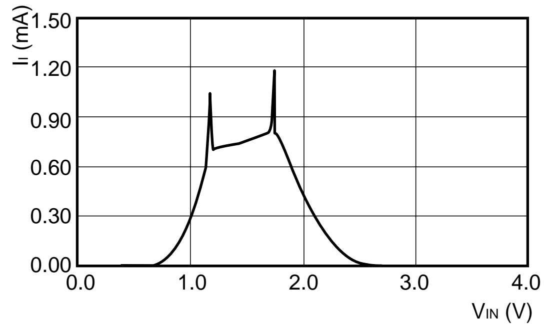


Figure 4-7. TTL 5-V Tolerant Input Through Current (5-V Input)

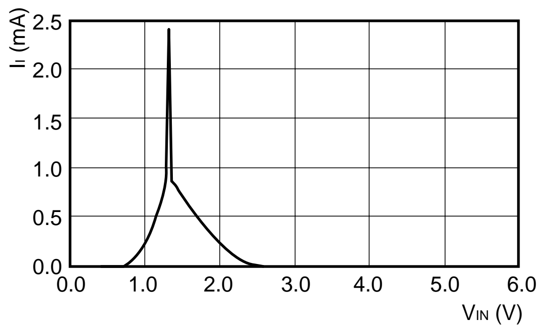


Figure 4-8. TTL 5-V Tolerant Input Through Current (5-V Schmitt Input)

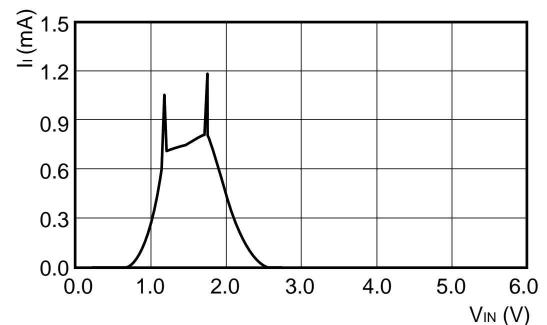


Figure 4-9. 5-V Input Through Current

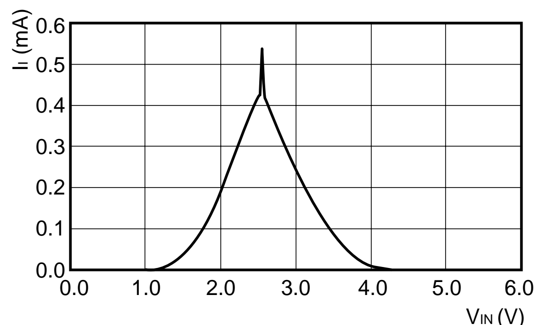
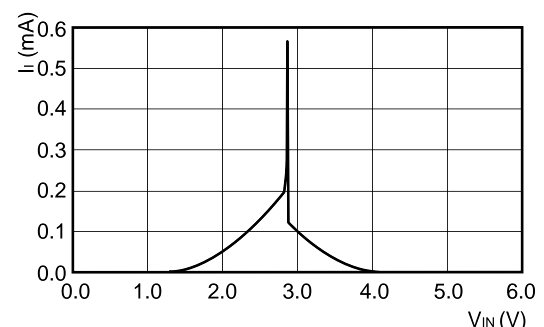


Figure 4-10. 5-V Input Through Current (Schmitt Input)



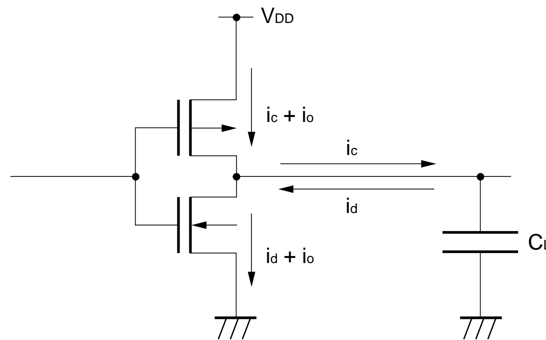
4.3 Power Consumption

Although CMOS transistors have low power consumption compared to bipolar devices, they actually consume a considerable amount of power when their circuits are large and when they are operated at a high frequency. The temperature of the LSI (chip), which is critical to the reliability (service life) of LSI products, may rise in proportion to the amount of power consumed, so be sure to consider each LSI's power consumption needs.

4.3.1 Cause of power consumption

In cell-based ICs, as in standard CMOS devices, the amount of current consumed is the sum of the following values.

Charge current of load capacitance connected to each transistor: i_c
Discharge current of load capacitance connected to each transistor: i_d
Through current when switching each transistor: i_O
Device's leakage current: I_L



If the LSI is not operating at all, it has neither any charge/discharge current nor any through current, so in such cases the chip's power consumption is merely the device's overall leakage current. On the other hand, when the LSI is operating, the charge/discharge current and through current comprise a much greater share of the power consumption value than does the leakage current, such that the leakage current can be safely ignored. Although the through current may increase greatly if the output rise (or fall) time is much shorter than each transistor's input rise (or fall) time, in general it varies in proportion to the charge/discharge current.

4.3.2 Estimation of entire chip's power consumption

If, after completing all of the circuit designs, it becomes apparent that the chip's power consumption exceeds the package's maximum allowable power consumption, the designers must either change to a package that has a lower thermal resistance or modify the circuits to reduce the chip's power consumption. Either method may result in large losses in terms of development TAT and costs.

Use the following method to estimate the chip's power consumption.

(1) First, estimate the power consumption of the various macros (cores, user logic, interface blocks).
For more information about the power consumption of cores, see **CB-9 Family VX/VM Type CPU, Peripheral Design Manual (A14304E)**.
For more information on user logic and interface blocks, see **4.3.3 Estimation of the power consumption of functional cells and interface blocks** below.

(2) Next, estimate the overall power consumption. Since adding all of the macro power consumption results from (1) above often produces a total value that is greater than the package's maximum allowable power consumption, calculate only the power consumption of macros that operate simultaneously and check whether those results are within the package's maximum allowable power consumption.
For details of the maximum allowable power consumption for various packages, see **4.3.6 Determination of power consumption** below.

4.3.3 Estimation of the power consumption of functional cells and interface blocks

Power consumption is determined based on the discharge current and through current of the various transistors. However, since it is difficult to define the status of each transistor, an approximate calculation of power consumption is instead performed based on the various types of blocks.

The results of the following formulas are premised on power supply and ambient temperature values of V_{DD} = 3.3 V and T_A = 25°C or V_{DD} = 2.0 V and T_A = 25°C. Therefore, the formulas must be adjusted when different power supply and ambient temperature values are used (see **4.3.5 Compensation method for change in power supply and ambient temperature specifications** below).

Total power consumption	$P_D = \Sigma P_{DGRID} + \Sigma P_{DI} + \Sigma P_{GTL} + \Sigma P_{DO}$
or	$P_D = \Sigma P_{DGATE} + \Sigma P_{DI} + \Sigma P_{GTL} + \Sigma P_{DO}$

(a) ΣP_{DGRID} … power consumption by functional cells (when V_{DD} = 3.3 V)

$\Sigma P_{DGRID} = \Sigma (0.10$ [Note 1] $\times f_C \times GRID \times A)$ (μW)
or
$\Sigma P_{DGATE} = \Sigma (0.30$ [Note 1] $\times f_C \times GATE \times A)$ (μW)

f_C: Clock operating frequency (MHz)
GRID: Number of grids operated by f_C
GATE: Number of gates operated by f_C
A: Operation rate [Note 2]

Remarks 1. When using clock tree synthesis, be sure to take into consideration the power consumption of buffers that are inserted on the clock line. The inserted buffers should operate at the same frequency as the clock. For details of the number of grids corresponding to inserted buffers, see **5.4.4 Clock tree synthesis** below.

2. For description of a more precise power consumption estimation method, see **4.3.4 Detailed estimation of internal circuit power consumption** below.

(b) ΣP_{DGRID} … power consumption by functional cells (when V_{DD} = 2.0 V)

$\Sigma P_{DGRID} = \Sigma (0.04$ [Note 1] $\times f_C \times GRID \times A)$ (μW)
or
$\Sigma P_{DGATE} = \Sigma (0.12$ [Note 1] $\times f_C \times GATE \times A)$ (μW)

f_C: Clock operating frequency (MHz)
GRID: Number of grids operated by f_C
GATE: Number of gates operated by f_C
A: Operation rate [Note 2]

Remarks 1. When using clock tree synthesis, be sure to take into consideration the power consumption of buffers that are inserted on the clock line. The inserted buffers should operate at the same frequency as the clock. For details of the number of grids corresponding to inserted buffers, see **5.4.4 Clock tree synthesis** below.

2. For description of a more precise power consumption estimation method, see **4.3.4 Detailed estimation of internal circuit power consumption** below.

(c) ΣP_{DI} … power consumption by input buffers and bi-directional buffers input section

$$\Sigma P_{DI} = \Sigma (P_I \times f_D + P_{CONST}) \times \text{Buffer} \quad (\mu W)$$

f_D: Data operating frequency (MHz)

Buffer: Number of input buffers and/or bi-directional buffers operated by f_D

If an input buffer is being operated intermittently, use an average operating frequency (f_A) Note 3

P_I: Power consumption by each input buffer (μW/Buffer/MHz)

P_{CONST}: Constant power consumption Note 4

Remark 1 cycle of a clock is considered to consist of a high and a low level. Thus, when treating a 10-MHz clock as data, calculate it as a 20-MHz clock.

★ **Table 4-1. Power Consumption by Each Input Buffer**

Block Type	P_I
FI01, FIA1, FIV1	3.76
FIS1, FIE1, FIF1	7.68
BC0P	1.5
FPV1,BP1C	10.7
BQ0P	42.5
BDJPAL	3.9
BU0PAL	51.3

(d) ΣP_{DO} … power consumption by output buffers and bi-directional buffers output section

$$\Sigma P_{DO} = \Sigma \{(P_O + P_{CO} \times C_L) \times f_D + P_{CONST}\} \times \text{Buffer} \quad (mW)$$

P_O: Power consumption by each output buffer (no load) (mW/MHz)

P_{CO}: Power consumption by each output buffer (load dependent) (mW/MHz/pF)

C_L: Load capacitance

f_D: Data operating frequency (MHz)

If an output buffer is being operated intermittently, use an average operating frequency (f_A) Note 3.

Buffer: Number of output buffers and/or bi-directional buffers operated by f_D

P_{CONST}: Constant power consumption Note 4

Remark 1 cycle of a clock is considered to consist of a high and a low level. Thus, when treating a 10-MHz clock as data, calculate it as a 20-MHz clock.

Table 4-2. Power Consumption by Output Buffers (1/2)

Internal 3.3 V/External 3.3 V LVTTL			Internal 2.0 V/External 3.0 V 3.0 V Interface			Internal 2.0 V/External 3.3 V LVTTL		
Block (I_{OL})	P_O	P_{CO}	Block (I_{OL})	P_O	P_{CO}	Block (I_{OL})	P_O	P_{CO}
FO09(3mA)	0.0607	0.0131	FO09AS(3mA)	0.0502	0.0089	FO09AS(3mA)	0.0626	0.0109
FO04(6mA)	0.0781	0.0119	FO04AS(6mA)	0.0639	0.0092	FO04AS(6mA)	0.0795	0.0111
FO01(9mA)	0.0810	0.0114	FO01AS(9mA)	0.0658	0.0093	FO01AS(9mA)	0.0816	0.0112
FO02(12mA)	0.0868	0.0109	FO02AS(12mA)	0.0697	0.0092	FO02AS(12mA)	0.0867	0.0111
FO03(18mA)	0.0943	0.0112	FO03AS(18mA)	0.0759	0.0093	FO03AS(18mA)	0.0950	0.0110
FO06(24mA)	0.1071	0.0109	FO06AS(24mA)	0.0852	0.0093	FO06AS(24mA)	0.1077	0.0112

★ **Table 4-2. Power Consumption by Output Buffers (2/2)**

TTL5-V Tolerant Interface			5-V Interface			PCI Interface		
Block (I_{OL})	P_O	P_{CO}	Block (I_{OL})	P_O	P_{CO}	Block	P_O	P_{CO}
FV0A(1mA)	0.2275	0.0113	FV0AAL(1mA)	0.2098	0.0246	B00Y, BC0P	0.0911	0.0111
FV0B(2mA)	0.2267	0.0104	FV0BAL(2mA)	0.2413	0.0259	BP1C	0.3085	0.0127
FV09(3mA)	0.2339	0.0120	FV09AL(3mA)	0.2518	0.0264	BQ0P	0.0835	0.0112
FV04(6mA)	0.2408	0.0120	FV04AL(6mA)	0.2826	0.0272	BV0Y	0.3226	0.0114
FV01(9mA)	0.2461	0.0117	FV01AL(9mA)	0.3147	0.0264	FOIO	0.0902	0.0098
FV02(12mA)	0.2614	0.0116	FV02AL(12mA)	0.3754	0.0257	FP14	0.2644	0.0136
			FV03AL(18mA)	0.5340	0.0252	BDJPAL, BV0YAL	0.4272	0.0259
						BU0PAL	0.3443	0.0262
						FVIOAL	0.4265	0.0256

3.3 V is defined as the output level of the TTL 5-V tolerant output, and 5.0 V is defined as the output level of the 5-V output.

Use the following formula to convert when the TTL 5-V tolerant output has 5-V pull-up.

$$P_{DO\,(5.0\,V)} = 1.65 \times P_{DO} \quad \text{(mW)}$$

(e) ΣP_{GTL} … power consumption by GTL (under development)

$\Sigma P_{GTL} = \Sigma P_{GI} \times \text{Buffer} + \Sigma P_{GO} \times \text{Buffer}$ (mW)

P_{GI}: Power consumption by input section (mW/Buffer)
P_{GO}: Power consumption by output section (mW/Buffer)

Table 4-3. Power Consumption by GTL Input Section

Condition	Current consumption (mA)	P_{GI} (mW/Buffer)
IEN = 1, A = 0		
IEN = 1, A = 1		
IEN = 0		

Remark Values are still under study.

Power consumption by GTL output section

P_{GO} = Under study (mW/Buffer)

Notes 1. The power consumption per grid (mW/cell/MHz) is rated under the following conditions.

<1> The ratio of combination circuits, flip-flops, and latches in the circuits is assumed to be as follows.
Gate: flip-flop: latch = 0.5 : 0.4 : 0.1

<2> The latch timing is assumed to be 40% of the gate’s active period when the data frequency is 1 MHz.

<3> The flip-flop power consumption value assumes a 1-MHz clock frequency and a 0.25-MHz data frequency.

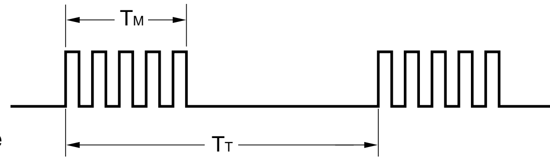
<4> The various output loads assume that $\Sigma F/I = 2$ and $\ell = 0.38$ (F/I conversion)

2. Operation rate
For example, in a buffer circuit, the input frequency and output frequency are the same and all of its transistors are operating, so the power consumption has a gate operation rate of “1”. By contrast, the power consumption of flip-flops and latch circuits is the total sum of the power consumption generated by the clock block. If the clock signal changes but the data does not change, the power consumption is generated only by the clock block and not by the data path block. In such cases, if the gate operation rate is “1”, it still takes into account the power consumption in the data path block. The gate operation rate uses a coefficient in which an “overflow margin” is set for such cases. In ordinary circuits, the operation rate is set at about 0.3. When there is a relatively large number of gates that operate at the clock frequency (such as when using clock tree synthesis), the operation rate tends to be greater than 0.3. The customer must set the operation rate according to the circuit specifications.

Notes 3. Average operation frequency (f_A)

When operation is intermittent, the average operation frequency (f_A) can be considered.

$$f_A = f_M \times T_M \div T_T$$



T_M: Measured operation time

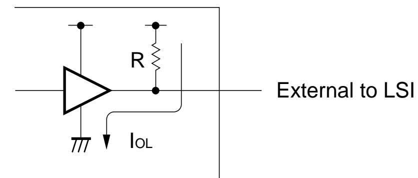
T_T: Intermittent operation cycle

f_M: Frequency during measured operation time

4. Constant power consumption

When a DC current is flowing through an input, output, or bi-directional buffer, a constant power consumption value should be added.

Example 1. DC current from pull-up/pull-down resistor



$$P_{CONST} = (V_{DD}^2/R) \times A$$

V_{DD}: Power supply voltage

R: Pull-up/pull-down resistance value

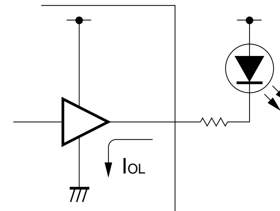
If the resistor is implemented in the LSI, use the TYP. resistance value.

A: Operation rate

This is the share of low-level status when using a pull-up resistor or high-level status when using a pull-down resistor.

The customer must set the operation rate according to the circuit specifications.

Example 2. Driving large-current devices, such as LEDs



$$P_{CONST} = V_O \times I_O \times A$$

A: When LED is ON.

4.3.4 Detailed estimation of internal circuit power consumption

Accurate calculations of the power consumption in internal circuits require many items of information, including information about each block, capacitance, the number of blocks that operate at the same time, and each block's operating frequency. This makes the calculations rather complicated; in many cases too complicated to be useful. NEC has therefore set reference values for power consumption based on hypothetical circuit operations and configurations. Consequently, note that these reference values may be slightly higher or lower than those obtained for the customer's circuits and configurations.

The following calculation method can be used for separate calculations of internal circuit power consumption in combination circuits, latches, flip-flops, etc. This method should be used to revise power consumption values. However, slightly larger values should be considered when using the calculation results to calculate such things as battery life.

In combination circuits, power consumption is generated whenever the gates or clocks change, even if the data does not change. Note with caution that if a clock is supplied to an entire chip using clock tree synthesis, power consumption occurs even when the macro is in standby mode.

★ **Power consumption in internal cells**

$$\Sigma P_{DGRID} = \Sigma P_{DGate} + \Sigma P_{DLatch} + \Sigma P_{DF/F} + \Sigma P_{DT}$$

(1) Combination circuit (when V_{DD} = 3.3 V)

$P_{DGate} = 0.14 \times A \times f \times GRID$ (μW)

A: Data operation rate[Note]

f: System operating frequency (MHz)

GRID: Number of combination circuit grids

(2) Combination circuit (when V_{DD} = 2.0 V)

$P_{DGate} = 0.05 \times A \times f \times GRID$ (μW)

A: Data operation rate[Note]

f: System operating frequency (MHz)

GRID: Number of combination circuit grids

(3) Latch (when V_{DD} = 3.3 V)

$P_{DLatch} = \{0.07 \times N + 0.01 \times (1 - N)\} \times A \times f \times GRID$ (μW)

N: $\dfrac{T_{(Gate = ON)}}{T_{(Gate = ON)} + T_{(Gate = OFF)}}$

A: Data operation rate[Note]

F: System operating frequency (MHz)

GRID Number of latch grids

(4) Latch (when V_{DD} = 2.0 V)

$P_{DLatch} = \{0.03 \times N + 0.005 \times (1 - N)\} \times A \times f \times GRID$ (μW)

N: $\dfrac{T_{(Gate = ON)}}{T_{(Gate = ON)} + T_{(Gate = OFF)}}$

A: Data operation rate[Note]

f: System operating frequency (MHz)

GRID: Number of latch grids

(5) D-F/F, JK-F/F, shift register, and counter (when V_{DD} = 3.3 V)

$P_{DF/F} = (0.10 \times A + 0.02) \times f \times GRID$ (μW)

A: Data operation rate[Note]

f: System operating frequency (MHz)

GRID: Number of D-F/F, JK-F/F, shift register, and counter grids

(6) D-F/F, JK-F/F, shift register, and counter (when V_{DD} = 2.0 V)

$P_{DF/F} = (0.04 \times A + 0.01) \times f \times GRID$ (μW)

A: Data operation rate[Note]

f: System operating frequency (MHz)

GRID: Number of D-F/F, JK-F/F, shift register, and counter grids

(7) T-F/F (V_{DD} = 3.3 V)

$P_{DT} = 0.07 \times f \times GRID$ (μW)

f: System operating frequency (MHz)

GRID: Number of T-F/F grids

(8) T-F/F (V_{DD} = 2.0 V)

$P_{DT} = 0.03 \times f \times GRID$ (μW)

f: System operating frequency (MHz)

GRID: Number of T-F/F grids

(9) Clock line (when V_{DD} = 3.3 V)

It is necessary to estimate the number of F/F, latch, and other blocks connected to the clock line.

$P_{CLK} = 0.873 \times f \times n$ (μW)

f: System operating frequency (MHz)

n: Number of blocks connected to clock line

(10) Clock line (when V_{DD} = 2.0 V)

It is necessary to estimate the number of F/F, latch, and other blocks connected to the clock line.

$P_{CLK} = 0.333 \times f \times n$ (μW)

f: System operating frequency (MHz)

n: Number of blocks connected to clock line

(11) Correction items (when V_{DD} = 3.3 V)

If, according to the user's circuit specifications, the estimated output load is greater than the average output load of each block (0.04 pF), make the following corrections for each block.

$P_{DGRID} = 10.89 \times (C_L - 0.04) \times A \times f \times n$ (μW)

C_L: Output load estimated by user (C_L > 0.04 pF)

A: Data operation are rate[Note]

f: System operating frequency (MHz)

n: Number of blocks connected that have an output load of C_L (take note that this is not the number of grids).

(12) Correction items (when V_{DD} = 2.0 V)

If, according to the user's circuit specifications, the estimated output load is greater than the average output load of each block (0.036 pF), make the following corrections for each block.

$P_{DGRID} = 4.00 \times (C_L - 0.036) \times A \times f \times n$ (μW)

C_L: Output load estimated by user (C_L > 0.036 pF)

A: Data operation rate[Note]

f: System operating frequency (MHz)

n: Number of blocks connected that have an output load of C_L (take note that this is not the number of grids).

Note The data operation rate is the proportion of total blocks operating simultaneously. Therefore, it 30% of the data line is operating simultaneously, the operation rate is 0.3. Note that because the data operation rate differs depending on the circuit specification, this rate must be set by users themselves.

4.3.5 Compensation method for changes in power supply and ambient temperature specifications

Be sure to compensate for power supply and ambient temperature specifications if they differ from the conditions (V_{DD} = 3.3V, T_A = 25°C and V_{DD} = 2.0V, T_A = 25°C) used in the calculation method described in 4.3.3 above.

$$P_W = P_D \times K_1 + \Sigma P_{CONST} \times K_2$$

P_D: Calculation result for total power consumption (including constant power consumption)
ΣP_{CONST}: Total for constant power consumption only
K_1: Compensation coefficient
K_2: Compensation coefficient

Compensation coefficient K_1

Rated power supply/temperature	Compensation coefficient $K_{1\ (TYP.)}$	Compensation coefficient $K_{1\ (MAX.)}$
V_{DD} = 3.3 ± 0.3 V T_A = –40 to +85°C	1.00	1.28
V_{DD} = 2.0 V ± 10% T_A = –40 to +85°C	1.00	1.17

Compensation coefficient K_2

Rated power supply/temperature	Compensation coefficient $K_{2\ (TYP.)}$	Compensation coefficient $K_{2\ (MAX.)}$
V_{DD} = 3.3 ± 0.3 V T_A = –40 to +85°C	0.00	0.15
V_{DD} = 2.0 V ± 10% T_A = –40 to +85°C	0.00	0.09

When determining the power consumption, use the compensation coefficient TYP. value. When high reliability is required, use the compensation coefficient MAX. value. The MAX. value can also be used when calculating maximum values for power consumption in the power supply and the temperature specification range.

4.3.6 Determination of power consumption

To determine power consumption, determine whether or not the calculated power consumption result (P_D) is within the maximum allowable power consumption (P_{WL}) as rated for each package and step size. Values for the maximum allowable power consumption (P_{WL}) as rated for each package or step size are listed in **Table 4-4. Maximum Allowable Power Consumption**.

$$P_D \leq P_{WL}$$

Because the values listed in **Table 4-4. Maximum Allowable Power Consumption** are based on an ambient temperature (T_A) range of -40 to +85°C and natural convection, if a different maximum temperature range is being used or if there is an air flow factor, the maximum allowable power consumption for the environment being used can be calculated based on the maximum ambient temperature ($T_{AMAX.}$) and the rated thermal resistance values (θ_{ja}) for each package and step size. The rated thermal resistance values (θ_{ja}) for each package and step size are listed in **Table 4-5. List of Thermal Resistance Values**. When measuring thermal resistance, mount the sample on a glass epoxy substrate measuring 90 × 90 mm in area and 1.6 mm in thickness.

$$P_{WL} = (125 - T_{AMAX.}) / \theta_{ja} \quad (W)$$

$$\text{Condition } T_{AMAX.} \geq 40°C$$

Table 4-4. Maximum Allowable Power Consumption (1/3)

Unit: W

Package	No. of Pins	Step Size Note 1								
		B60*	C02*	C40*	C78*	D01*	D26*	D52*	D90*	E16*
QFP	44		–	–	–	–	–	–	–	–
	52		–	–	–	–	–	–	–	–
	64		–	–	–	–	–	–	–	–
	100	–	–	–					–	–
	120	–	–							–
	160	–	–	–	–	–				–
	160 Note 2	–	–	–	–	–	–			–
QFP (fine pitch)	100	0.35	0.38	0.41	0.43	0.45	0.47	0.49	0.51	0.53
	120	–	0.45	0.48	0.51	0.52	0.54	0.56	0.58	0.60
	144	–	–		0.51	0.52	0.54	0.56	0.58	0.60
	160	–	–	–	–	–				
	176	–	–	–	–	–	–	–		
	144 Note 2									
	160 Note 2	0.75	0.75	0.75	0.75	0.82	0.82	0.82	0.82	0.83
	176 Note 2					0.82	0.82	0.82	0.82	0.83
	208 Note 2	–		1.05	1.05	1.05	1.05	1.05	1.05	1.05
	240 Note 2	–	–			1.08	1.08	1.08	1.08	1.08
	256 Note 2	–	–	–	–	–	–	–	–	–
	304 Note 2	–	–	–	–	–	–	–	–	–
QFP (fine pitch) with HSP	160 Note 2	–	–	–	–	–	–	–	1.33	1.33
	176 Note 2	–	–	–	–	–	–	–	–	–
	208 Note 2	–	–	–	–	–	–	–	–	–
	240 Note 2	–	–	–	–	–	–	–	–	–
	304 Note 2	–	–	–	–	–	–	–	–	–
TQFP	64 Note 2			–	–	–	–	–	–	–
	80	0.35	0.38	0.40	0.42	0.43	0.45	0.46	–	–
	100 Note 2	0.51	0.53	0.56	0.57	0.59	0.60	0.61	0.63	0.63
	120 Note 2	–	0.51	0.54	0.57	0.58	0.60	0.62	0.63	
LQFP	144 Note 2	–	–		0.68	0.69	0.71	0.73	0.75	0.77
	160 Note 2	–	–	–	–	–	–	–	–	0.77
	176 Note 2	–	–	–	–	–	–		0.75	0.77
	208 Note 2	–	–	–	–	–	–	–	–	–
Plastic BGA	225	–	–	–	–	–	–	1.21	1.21	1.21
	256	–	–	–	1.33	1.33	1.33	1.33	1.33	1.33
	313	–	–	–	–	–	–	–	1.54	1.54
	352	–	–	–	–	–	–	–	–	–
Tape BGA	256	–	–	–	1.90	1.90	1.90	1.90	1.90	1.90
	352	–	–	–					2.50	2.50
	420	–	–	–	–	–	–	–	–	
	500	–	–	–	–	–	–	–	–	–
	576	–	–	–	–	–	–	–	–	–
	696	–	–	–	–	–	–	–	–	–

Notes 1. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C

2. Low thermal resistance type (using copper material)

Remarks 1. –: Not available

2. Note with caution that the listed values include values from packages that are still under development.

3. HSP: Heat spreader

Table 4-4. Maximum Allowable Power Consumption (2/3)

Unit: W

Package	No. of Pins	Step Size Note 1							
		E54*	E80*	F18*	F44*	F70*	G08*	G34*	G72*
QFP	44	–	–	–	–	–	–	–	–
	52	–	–	–	–	–	–	–	–
	64	–	–	–	–	–	–	–	–
	100	–	–	–	–	–	–	–	–
	120	–	–	–	–	–	–	–	–
	160	–	–	–	–	–	–	–	–
	160 Note 2	–	–	–	–	–	–	–	–
QFP (fine pitch)	100	0.56	0.58	0.61	0.62	0.63	–	–	–
	120	0.63	0.63	0.67	0.68	0.69	0.71	0.73	0.75
	144	0.63	0.63	0.67	0.68	0.69	0.71	0.73	0.75
	160							–	–
	176			–	–	–	–	–	–
	144 Note 2					–	–	–	–
	160 Note 2	0.87	0.89	0.91	0.93	0.95	0.98	1.00	1.03
	176 Note 2	0.87	0.89	0.91	0.93	0.95	0.98	1.00	1.03
	208 Note 2	1.05	1.05	1.05	1.05	1.08	1.11	1.11	1.14
	240 Note 2	1.08	1.08	1.25	1.25	1.25	1.25	1.25	1.25
	256 Note 2						–	–	–
	304 Note 2	–	–	1.14	1.14	1.14	1.29	1.29	1.29
QFP (fine pitch) with HSP	160 Note 2	1.33	1.33	1.33	1.33	1.33	–	–	–
	176 Note 2	1.05	1.33	1.33	1.33	1.33	1.33	1.33	1.33
	208 Note 2	–	–	1.54	1.54	1.54	1.54	1.54	1.54
	240 Note 2	–	–	–	–	–	–	–	–
	304 Note 2	–	–	–	–	–	–	–	–
TQFP	64 Note 2	–	–	–	–	–	–	–	–
	80	–	–	–	–	–	–	–	–
	100 Note 2	–	–	–	–	–	–	–	–
	120 Note 2			–	–	–	–	–	–
LQFP	144 Note 2	0.80	0.82	0.83	0.85	0.85	0.89	0.89	0.91
	160 Note 2	0.80	0.82	0.83	0.85	–	–	–	–
	176 Note 2	0.80	0.82	–	–	–	–	–	–
	208 Note 2			0.89	0.91	–	–	–	–
Plastic BGA	225	1.21	1.21	1.21	1.21	1.21	1.21	1.21	–
	256	1.33	1.33	1.33	1.33	1.33	1.33	1.33	–
	313	1.54	1.54	1.54	1.54	1.54	1.54	1.54	1.54
	352	–	–	–	1.82	1.82	1.82	1.82	1.82
Tape BGA	256	1.90	1.90	1.90	1.90	1.90	1.90	–	–
	352	2.50	2.50	2.50	2.50	2.50	2.50	2.50	2.50
	420	2.50	2.50	2.50	2.50	2.50	2.50	2.50	2.50
	500	–	–	2.86	2.86	2.86	2.86	2.86	2.86
	576	–	–	–	–	–	–	2.86	2.86
	696	–	–	–	–	–	–	–	–

Notes 1. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C

2. Low thermal resistance type (using copper material)

Remarks 1. –: Not available

2. Note with caution that the listed values include values from packages that are still under development.

3. HSP: Heat spreader

Table 4-4. Maximum Allowable Power Consumption (3/3)

Unit: W

Package	No. of Pins	Step Size Note 1						
		H10*	H49*	H87*	J26*	J51*	K15*	K92*
QFP	44	–	–	–	–	–	–	–
	52	–	–	–	–	–	–	–
	64	–	–	–	–	–	–	–
	100	–	–	–	–	–	–	–
	120	–	–	–	–	–	–	–
	160	–	–	–	–	–	–	–
	160 Note 2	–	–	–	–	–	–	–
QFP (fine pitch)	100	–	–	–	–	–	–	–
	120	0.77	0.80	0.82	–	–	–	–
	144	0.77	0.80	0.82	–	–	–	–
	160	–	–	–	–	–	–	–
	176	–	–	–	–	–	–	–
	144 Note 2	–	–	–	–	–	–	–
	160 Note 2	1.05	1.08	1.08	1.11	1.14	1.18	1.21
	176 Note 2	1.05	1.08	1.08	1.11	1.14	1.18	1.21
	208 Note 2	1.18	1.21	1.25	1.25	1.29	1.33	1.38
	240 Note 2	1.29	1.33	1.38	1.38	1.43	1.48	1.60
	256 Note 2	–	–	–	–	–	–	–
	304 Note 2	1.29	1.29	1.29	1.29	1.33	1.38	1.43
QFP (fine pitch) with HSP	160 Note 2	–	–	–	–	–	–	–
	176 Note 2	1.33	1.33	1.33	1.33	–	–	–
	208 Note 2	1.54	1.54	1.54	1.54	1.54	1.54	1.54
	240 Note 2	–	1.90	1.90	1.90	1.90	1.90	1.90
	304 Note 2	–	–	–	–	2.22	2.22	2.22
TQFP	64 Note 2	–	–	–	–	–	–	–
	80	–	–	–	–	–	–	–
	100 Note 2	–	–	–	–	–	–	–
	120 Note 2	–	–	–	–	–	–	–
LQFP	144 Note 2	0.93	0.95	–	–	–	–	–
	160 Note 2	–	–	–	–	–	–	–
	176 Note 2	–	–	–	–	–	–	–
	208 Note 2	–	–	–	–	–	–	–
Plastic BGA	225 Note 2	–	–	–	–	–	–	–
	256 Note 2	–	–	–	–	–	–	–
	313 Note 2	1.54	1.54	1.54	1.54	1.54	1.54	1.54
	352 Note 2	1.82	1.82	1.82	1.82	1.82	1.82	1.82
Tape BGA	256	–	–	–	–	–	–	–
	352	2.50	2.50	2.50	2.50	2.50	2.50	2.50
	420	2.50	2.50	2.50	2.50	2.50	2.50	2.50
	500	2.86	2.86	2.86	2.86	2.86	2.86	2.86
	576	2.86	2.86	2.86	2.86	2.86	2.86	2.86
	696	–	–	2.86	2.86	2.86	2.86	2.86

Notes 1. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C

2. Low thermal resistance type (using copper material)

Remarks 1. –: Not available

2. Note with caution that the listed values include values from packages that are still under development.

3. HSP: Heat spreader

Table 4-5. List of Thermal Resistance Values (1/5)

Unit: °C/W

Package	No. of Pins	Step Size [Note 1]														
		B60*			C02*			C40*			C78*			D01*		
		Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
QFP	44				–	–	–	–	–	–	–	–	–	–	–	–
	52				–	–	–	–	–	–	–	–	–	–	–	–
	64				–	–	–	–	–	–	–	–	–	–	–	–
	100	–	–	–	–	–	–	–	–	–						
	120	–	–	–	–	–	–									
	160	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	160[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
QFP (fine pitch)	100	115	106	97	106	96	87	98	88	80	92	82	73	89	79	70
	120	–	–	–	89	81	74	83	76	68	79	71	64	77	69	61
	144	–	–	–	–	–	–				79	71	64	77	69	61
	160	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	176	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	144[Note 2]															
	160[Note 2]	53	43	42	53	43	42	53	43	42	53	43	42	49	40	39
	176[Note 2]													49	40	39
	208[Note 2]	–	–	–				38	31	29	38	31	29	38	31	29
	240[Note 2]	–	–	–	–	–	–							37	32	30
	256[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	304[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
QFP (fine pitch) with HSP	160[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	176[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	208[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	240[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	304[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
TQFP	64[Note 2]							–	–	–	–	–	–	–	–	–
	80	114	95	88	106	87	79	100	80	72	95	75	66	92	72	63
	100[Note 2]	78	70	62	75	66	59	72	63	56	70	61	54	68	60	52
	120[Note 2]	–	–	–	78	69	62	74	65	58	70	62	55	69	60	53
LQFP	144[Note 2]	–	–	–	–	–	–				59	53	47	58	51	46
	160[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	176[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	208[Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Plastic BGA	225	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	256	–	–	–	–	–	–	–	–	–	30	26	24	30	26	24
	313	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	352	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Tape BGA	256	–	–	–	–	–	–	–	–	–	21	15	12	21	15	12
	352	–	–	–	–	–	–	–	–	–						
	420	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	500	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	576	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	696	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Notes 1. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C

2. Low thermal resistance type (using copper material)

Remarks 1. –: Not available

2. Note with caution that the listed values include values from packages that are still under development.

3. HSP: Heat spreader

Table 4-5. List of Thermal Resistance Values (2/5)

Unit: °C/W

Package	No. of Pins	Step Size Note 1														
		D26*			D52*			D90*			E16*			E54*		
		Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
QFP	44	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	52	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	64	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	100							–	–	–	–	–	–	–	–	–
	120										–	–	–	–	–	–
	160										–	–	–	–	–	–
	160 Note 2	–	–	–							–	–	–	–	–	–
QFP (fine pitch)	100	85	75	67	82	72	64	78	68	59	75	65	57	72	62	54
	120	74	66	59	72	64	57	69	61	53	67	59	52	64	56	49
	144	74	66	59	72	64	57	69	61	53	67	59	52	64	56	49
	160															
	176	–	–	–	–	–	–									
	144 Note 2															
	160 Note 2	49	40	39	49	40	39	49	40	39	48	39	38	46	38	37
	176 Note 2	49	40	39	49	40	39	49	40	39	48	39	38	46	38	37
	208 Note 2	38	31	29	38	31	29	38	31	29	38	31	29	38	31	29
	240 Note 2	37	32	30	37	32	30	37	32	30	37	32	30	37	32	30
	256 Note 2	–	–	–	–	–	–	–	–	–	–	–	–			
	304 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
QFP (fine pitch) with HSP	160 Note 2	–	–	–	–	–	–	30	18	15	30	18	15	30	18	15
	176 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	38	18	15
	208 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	240 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	304 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
TQFP	64 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	80	89	69	60	87	66	57	–	–	–	–	–	–	–	–	–
	100 Note 2	67	58	51	66	57	50	64	55	48	63	54	47	–	–	–
	120 Note 2	67	58	51	65	57	49	63	54	47						
LQFP	144 Note 2	56	50	44	55	49	43	53	47	41	52	46	40	50	44	38
	160 Note 2	–	–	–	–	–	–	–	–	–	52	46	40	50	44	38
	176 Note 2	–	–	–				53	47	41	52	46	40	50	44	38
	208 Note 2	–	–	–	–	–	–	–	–	–	–	–	–			
Plastic BGA	225	–	–	–	33	28	26	33	28	26	33	28	26	33	28	26
	256	30	26	24	30	26	24	30	26	24	30	26	24	30	26	24
	313	–	–	–	–	–	–	26	22	21	26	22	21	26	22	21
	352	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Tape BGA	256	21	15	12	21	15	12	21	15	12	21	15	12	21	15	12
	352							16	11	9	16	11	9	16	11	9
	420	–	–	–	–	–	–	–	–	–				16	11	9
	500	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	576	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	696	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Notes 1. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C

2. Low thermal resistance type (using copper material)

Remarks 1. –: Not available

2. Note with caution that the listed values include values from packages that are still under development.

3. HSP: Heat spreader

Table 4-5. List of Thermal Resistance Values (3/5)

Unit: °C/W

Package	No. of Pins	Step Size Note 1														
		E80*			F18*			F44*			F70*			G08*		
		Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
QFP	44	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	52	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	64	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	100	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	120	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	160	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	160 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
QFP (fine pitch)	100	69	60	52	66	57	49	65	55	47	63	53	46	–	–	–
	120	63	54	47	60	52	45	59	51	44	58	50	43	56	48	41
	144	63	54	47	60	52	45	59	51	44	58	50	43	56	48	41
	160															
	176				–	–	–	–	–	–	–	–	–	–	–	–
	144 Note 2										–	–	–	–	–	–
	160 Note 2	45	37	36	44	36	35	43	35	34	42	35	33	41	34	32
	176 Note 2	45	37	36	44	36	35	43	35	34	42	35	33	41	34	32
	208 Note 2	38	31	29	38	31	29	38	31	29	37	31	29	36	30	28
	240 Note 2	37	32	30	32	27	25	32	27	25	32	27	25	32	27	25
	256 Note 2													–	–	–
	304 Note 2	–	–	–	35	30	27	35	30	27	35	30	27	31	26	23
QFP (fine pitch) with HSP	160 Note 2	30	18	15	30	18	15	30	18	15	30	18	15	–	–	–
	176 Note 2	30	18	15	30	18	15	30	18	15	30	18	15	30	18	15
	208 Note 2	–	–	–	26	19	16	26	19	16	26	19	16	26	19	16
	240 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	304 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
TQFP	64 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	80	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	100 Note 2	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	120 Note 2				–	–	–	–	–	–	–	–	–	–	–	–
LQFP	144 Note 2	49	43	38	48	42	36	47	41	35	47	40	35	45	39	34
	160 Note 2	49	43	38	48	42	36	47	41	35	–	–	–	–	–	–
	176 Note 2	49	43	38	–	–	–	–	–	–	–	–	–	–	–	–
	208 Note 2				45	40	36	44	39	35	–	–	–	–	–	–
Plastic BGA	225	33	28	26	33	28	26	33	28	26	33	28	26	33	28	26
	256	30	26	24	30	26	24	30	26	24	30	26	24	30	26	24
	313	26	22	21	26	22	21	26	22	21	26	22	21	26	22	21
	352	–	–	–	–	–	–	22	18	16	22	18	16	22	18	16
Tape BGA	256	21	15	12	21	15	12	21	15	12	21	15	12	21	15	12
	352	16	11	9	16	11	9	16	11	9	16	11	9	16	11	9
	420	16	11	9	16	11	9	16	11	9	16	11	9	16	11	9
	500	–	–	–	14	10	8	14	10	8	14	10	8	14	10	8
	576	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	696	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Notes 1. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C

2. Low thermal resistance type (using copper material)

Remarks 1. –: Not available

2. Note with caution that the listed values include values from packages that are still under development.

3. HSP: Heat spreader

Table 4-5. List of Thermal Resistance Values (4/5)

Unit: °C/W

Package	No. of Pins	Step Size [Note 1]														
		G34*			G72*			H10*			H49*			H87*		
		Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)		
		0	1	2	0	1	2	0	1	2	0	1	2	0	1	2
QFP	44	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	52	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	64	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	100	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	120	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	160	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	160 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
QFP (fine pitch)	100	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	120	55	47	40	53	45	38	52	44	37	50	42	36	49	41	35
	144	55	47	40	53	45	38	52	44	37	50	42	36	49	41	35
	160	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	176	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	144 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	160 [Note 2]	40	33	31	39	32	30	38	32	29	37	31	29	37	30	28
	176 [Note 2]	40	33	31	39	32	30	38	32	29	37	31	29	37	30	28
	208 [Note 2]	36	29	27	35	29	26	34	28	26	33	27	25	32	27	24
	240 [Note 2]	32	27	25	32	27	25	31	26	24	30	25	23	29	25	22
	256 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	304 [Note 2]	31	26	23	31	26	23	31	26	23	31	26	23	31	26	23
QFP (fine pitch) with HSP	160 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	176 [Note 2]	30	18	15	30	18	15	30	18	15	30	18	15	30	18	15
	208 [Note 2]	26	19	16	26	19	16	26	19	16	26	19	16	26	19	16
	240 [Note 2]	–	–	–	–	–	–	–	–	–	21	15	13	21	15	13
	304 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
TQFP	64 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	80	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	100 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	120 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
LQFP	144 [Note 2]	45	38	33	44	37	32	43	36	31	42	36	30	–	–	–
	160 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	176 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	208 [Note 2]	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Plastic BGA	225	33	28	26	–	–	–	–	–	–	–	–	–	–	–	–
	256	30	26	24	–	–	–	–	–	–	–	–	–	–	–	–
	313	26	22	21	26	22	21	26	22	21	26	22	21	26	22	21
	352	22	18	16	22	18	16	22	18	16	22	18	16	22	18	16
Tape BGA	256	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
	352	16	11	9	16	11	9	16	11	9	16	11	9	16	11	9
	420	16	11	9	16	11	9	16	11	9	16	11	9	16	11	9
	500	14	10	8	14	10	8	14	10	8	14	10	8	14	10	8
	576	14	10	8	14	10	8	14	10	8	14	10	8	14	10	8
	696	–	–	–	–	–	–	–	–	–	–	–	–	14	10	8

Notes 1. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C

2. Low thermal resistance type (using copper material)

Remarks 1. –: Not available

2. Note with caution that the listed values include values from packages that are still under development.

3. HSP: Heat spreader

Table 4-5. List of Thermal Resistance Values (5/5)

Unit: °C/W

Package	No. of Pins	Step Size Note 1											
		J26*			J51*			K15*			K92*		
		Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)			Forced-Air Cooling (m/s)		
		0	1	2	0	1	2	0	1	2	0	1	2
QFP	44	–	–	–	–	–	–	–	–	–	–	–	–
	52	–	–	–	–	–	–	–	–	–	–	–	–
	64	–	–	–	–	–	–	–	–	–	–	–	–
	100	–	–	–	–	–	–	–	–	–	–	–	–
	120	–	–	–	–	–	–	–	–	–	–	–	–
	160	–	–	–	–	–	–	–	–	–	–	–	–
	160 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
QFP (fine pitch)	100	–	–	–	–	–	–	–	–	–	–	–	–
	120	–	–	–	–	–	–	–	–	–	–	–	–
	144	–	–	–	–	–	–	–	–	–	–	–	–
	160	–	–	–	–	–	–	–	–	–	–	–	–
	176	–	–	–	–	–	–	–	–	–	–	–	–
	144 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
	160 Note 2	36	30	27	35	29	27	34	28	26	33	27	24
	176 Note 2	36	30	27	35	29	27	34	28	26	33	27	24
	208 Note 2	32	26	24	31	26	23	30	25	22	29	24	21
	240 Note 2	29	24	22	28	23	21	27	22	20	25	21	19
	256 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
	304 Note 2	31	26	23	30	25	22	29	25	21	28	24	20
QFP (fine pitch) with HSP	160 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
	176 Note 2	30	18	15	–	–	–	–	–	–	–	–	–
	208 Note 2	26	19	16	26	19	16	26	19	16	26	19	16
	240 Note 2	21	15	13	21	15	13	21	15	13	21	15	13
	304 Note 2	–	–	–	18	15	12	18	15	12	18	15	12
TQFP	64 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
	80	–	–	–	–	–	–	–	–	–	–	–	–
	100 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
	120 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
LQFP	144 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
	160 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
	176 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
	208 Note 2	–	–	–	–	–	–	–	–	–	–	–	–
Plastic BGA	225	–	–	–	–	–	–	–	–	–	–	–	–
	256	–	–	–	–	–	–	–	–	–	–	–	–
	313	26	22	21	26	22	21	26	22	21	26	22	21
	352	22	18	16	22	18	16	22	18	16	22	18	16
Tape BGA	256	–	–	–	–	–	–	–	–	–	–	–	–
	352	16	11	9	16	11	9	16	11	9	16	11	9
	420	16	11	9	16	11	9	16	11	9	16	11	9
	500	14	10	8	14	10	8	14	10	8	14	10	8
	576	14	10	8	14	10	8	14	10	8	14	10	8
	696	14	10	8	14	10	8	14	10	8	14	10	8

Notes 1. The asterisk that appears next to the listed step sizes indicates T and C types.
Example: B60* = B60T and B60C

2. Low thermal resistance type (using copper material)

Remarks 1. –: Not available

2. Note with caution that the listed values include values from packages that are still under development.

3. HSP: Heat spreader

4.4 Propagation Delay Times

4.4.1 Precision in delay times

The propagation delay time (t_{PD}) may vary for I/O buffers and internal functional cells due to the following causes.
Causes of delay time variation

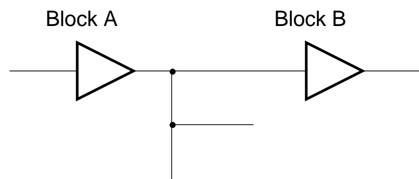
- Load capacitance (number of fan-outs, wire capacitance)
- Power supply voltage
- Ambient temperature
- Variation in manufacturing
- Other circuit-related causes

Circuit-related causes other than variation in power supply voltage, ambient temperature, and load capacitance include variation caused by the waveform of the input signal, variation in the transfer gate's equivalent input capacitance, the Miller effect, and variation in the input threshold voltage. NEC has introduced delay simulators and static delay calculators so as to take these causes into account to the fullest extent possible and thereby ensure maximum precision in delay calculations. Note, therefore, that when using the delay time values listed in Block Library, the listed delay times may not match the delay time values calculated by the customer.

4.4.2 Calculation of delay times

The formula shown below is an abbreviated formula that simplifies this calculation. This formula will yield a relatively accurate result as long as the load in particular meets the following conditions. The margin of error increases with higher load capacitance, and the result may be less than that produced by the simulator. Please be aware that these calculation results cannot be applied for actual design and are to be used only as reference values. Moreover, rounding of the signal input is not taken into consideration in the abbreviated formula. Therefore, these calculation results cannot be used if the total F/I prior to the block for which delay is calculated exceeds 15% of the F/O limit of the previous driver block.

Example



When Block B is the block for which delay time is being calculated, the abbreviated formula will provide a precise result as long as the total number of fan-ins connected to Block A's output is within 15% of Block A's fan-out limit.

(1) Delay times in input buffers and internal function blocks

An approximate calculation of the delay times in internal function blocks can be made based on the load (number of fan-outs) and wire length (wire capacitance) connected to the corresponding output pin.

- Load capacitance: $C_L = \Sigma (C_{IN} + L \times 0.18)$ (pF)
  C_{IN}: Input capacitance (pF) [C_{IN}]
  L: Wire length (mm)

  $t_{PD} = t_{LD0} + C_L \times t_1$ (ns)
  t_{LD0}: Gate delay (ns) [IntrinsicA]
  t_1: Delay coefficient (ns/pF) [ExtrinsicA]

Remark Terms enclosed in square brackets [ ] are expressions used in the block library.

(2) Delay times in output buffers

An approximate calculation of the delay times in an output buffer can be made based on the load capacitance connected to the corresponding output pin.

$t_{PD} = t_{LD0} + C_L \times t_1$ (ns)

t_{LD0}: Gate delay (ns) [IntrinsicA]

C_L: Load capacitance connected to corresponding output pin

t_1: Delay coefficient (ns/pF) [ExtrinsicA]

Remark Terms enclosed in square brackets [ ] are expressions used in the block library.

See Block Library for values corresponding to C_{IN}, t_{LD0}, and t_1.

In the above equations, the minimum and maximum delay time values are obtained using the corresponding maximum or minimum values listed in the block library for t_{LD0} and t_1.

4.4.3 Variation in delay times

As was explained in **4.4.1 Precision in delay times**, there are various causes for variations in propagation delay times (t_{PD}) related to I/O buffers and internal function blocks. The MIN./MAX. values described in the Block Library are the minimum and maximum values under conditions of V_{DD} = 3.3 ± 0.3 V and T_A = –40 to +85°C (T_J = –40 to +125°C). The differential between the TYP. values and these values is called the absolute variation. For CB-9 Family VX/VM type devices, delay time coefficients are described under the three conditions of MIN., TYP. , and MAX.

The absolute variation of each block is considered separately when calculating more precise delay times for CB-9 Family VX/VM type devices. Therefore, it is not possible to use a uniform absolute delay coefficient as was done for previous devices. As a reference, parts (a) to (h) of Table 4-6 describe the power supply voltage and operating junction temperature dependencies pertaining to the delay coefficient. The absolute variation coefficient can be revised based on limitations on ambient temperature or power consumption (for example, limiting temperature rise due to power consumption to about 10°C). The following formula can be used to calculate the operating junction temperature when ambient temperature and/or power consumption are limited. When the operating junction temperature is suppressed, the absolute variation coefficient approaches a value of 1 (speed is about 5% faster when the operating junction temperature is suppressed to 100°C than when it is set at 125°C).

$T_J = T_{AMAX.} + P_D \times \theta_{ja}$ (°C)

Where,

T_J: Operating junction temperature

$T_{AMAX.}$: Maximum value of ambient temperature

P_D: Power consumption as estimated using formula described in 4.3.3 above.

θ_{ja}: Thermal resistance from Table 4-5

Table 4-6. Propagation Delay Time Characteristics (1/3)

(a) Derating factors (MIN. condition)

Operating junction temperature	Voltage				
	3.30	3.45	3.60	3.75	3.90
–40	1.111	1.052	1.000	0.988	0.978
–20	1.163	1.104	1.062	1.042	1.029
0	1.218	1.164	1.125	1.101	1.084

(b) Setup (MIN. condition)

Operating junction temperature	Voltage				
	3.30	3.45	3.60	3.75	3.90
–40	0.00	0.00	0.00	0.07	0.12
–20	0.00	0.00	0.00	0.09	0.15
0	0.00	0.00	0.00	0.12	0.18

Table 4-6. Propagation Delay Time Characteristics (2/3)

(c) Hold (MIN. condition)

Operating junction temperature	Voltage				
	3.30	3.45	3.60	3.75	3.90
–40	0.00	0.00	0.00	0.08	0.15
–20	0.00	0.00	0.00	0.11	0.18
0	0.00	0.00	0.00	0.13	0.20

(d) Minimum pulse width (MIN. condition)

Operating junction temperature	Voltage				
	3.30	3.45	3.60	3.75	3.90
–40	0.00	0.00	0.00	0.00	0.00
–20	0.00	0.00	0.00	0.04	0.03
0	0.00	0.00	0.00	0.08	0.07

(e) Derating factors (MAX. condition)

Operating junction temperature	Voltage				
	2.70	2.85	3.00	3.15	3.30
75	1.132	1.040	0.967	0.914	0.877
100	1.152	1.059	0.985	0.936	0.905
125	1.174	1.080	1.000	0.967	0.940

(f) Setup (MAX. condition)

Operating junction temperature	Voltage				
	2.70	2.85	3.00	3.15	3.30
75	0.35	0.18	0.00	0.00	0.00
100	0.33	0.16	0.00	0.00	0.00
125	0.32	0.15	0.00	0.00	0.00

(g) Hold (MAX. condition)

Operating junction temperature	Voltage				
	2.70	2.85	3.00	3.15	3.30
75	0.23	0.16	0.00	0.00	0.00
100	0.19	0.11	0.00	0.00	0.00
125	0.15	0.08	0.00	0.00	0.00

Table 4-6. Propagation Delay Time Characteristics (3/3)

(h) Minimum pulse width (MAX. condition)

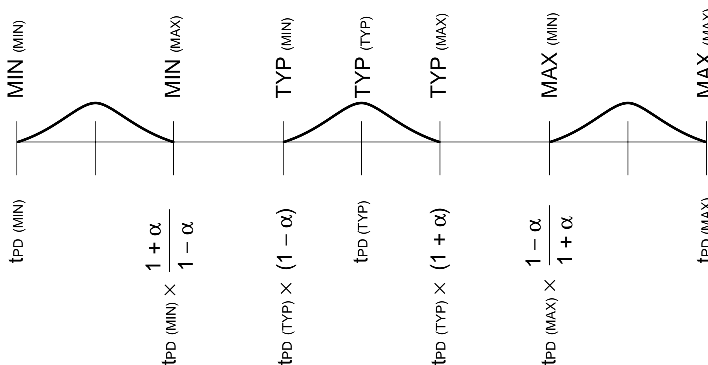
Operating junction temperature	Voltage				
	2.70	2.85	3.00	3.15	3.30
75	0.21	0.07	0.00	0.00	0.00
100	0.24	0.10	0.00	0.00	0.00
125	0.27	0.13	0.00	0.00	0.00

In addition to the absolute variation that is applied as the device rating, relative variation occurs depending on the types of paths and the characteristics of the chip's P-channel and N-channel transistors. This relative variation is an important factor to be considered when confirming circuit timing. The relative variation is calculated as follows for CB-9 Family VX/VM type devices.

Relative variation $\alpha = 10\%$

Figure 4-11 describes variations centered on a TYP. value for t_{PD}.

Figure 4-11. t_{PD} Variations



4.5 Output Buffer Characteristics

4.5.1 Output buffer rise and fall times

Output buffer rise and fall times differ greatly depending on output level-related drive capacity differences and connected load capacitance. An approximate calculation of output buffer rise (t_r) and fall (t_f) times can be obtained via the following formula.

$$t_r = t_{r0} + F_{tr} \times C_L \quad \text{(ns)}$$
$$t_f = t_{f0} + F_{tf} \times C_L \quad \text{(ns)}$$

t_{r0}: Basic rise time (load capacitance $C_L = 0$ pF)
t_{f0}: Basic fall time (load capacitance $C_L = 0$ pF)
F_{tr}, F_{tf}: Load capacitance coefficients
C_L: Load capacitance (pF) ($0 < C_L \leq 300$pF)

The various output buffer coefficients are listed in Tables 4-7 to 4-10.

Table 4-7. List of Coefficients for LVTTL Output Buffer t_r and t_f Calculations

(a) When output level is between $V_{DD} \times 10\%$ and $V_{DD} \times 90\%$ (MAX.)

Buffer Type	Example	Drive Capacity	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FO09	I_{OL} = 3.0 mA	1.81	0.394	1.32	0.288
	FO04	I_{OL} = 6.0 mA	1.01	0.196	0.85	0.142
	FO01	I_{OL} = 9.0 mA	0.72	0.130	0.68	0.094
	FO02	I_{OL} = 12.0 mA	0.60	0.096	0.59	0.071
	FO03	I_{OL} = 18.0 mA	0.44	0.064	0.42	0.048
	FO06	I_{OL} = 24.0 mA	0.40	0.048	0.39	0.036
	FOIO	PCI	1.37	0.059	1.19	0.050
Low noise	FE04	I_{OL} = 6.0 mA	1.51	0.192	1.42	0.137
	FE01	I_{OL} = 9.0 mA	1.33	0.125	1.24	0.091
	FE02	I_{OL} = 12.0 mA	1.23	0.093	1.12	0.069
	FE03	I_{OL} = 18.0 mA	1.13	0.063	1.02	0.049
	FE06	I_{OL} = 24.0 mA	1.11	0.049	0.96	0.039

Remark The output buffer rise and fall times are rated under the following conditions.
V_{DD} = 3.0 V, T_A = 85°C, and input signal t_r/t_f = 0.4 ns/3.0 V

(b) When output level is between 0.8 V and 2.0 V (MAX.)

Buffer Type	Example	Drive Capacity	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FO09	I_{OL} = 3.0 mA	0.76	0.161	0.59	0.125
	FO04	I_{OL} = 6.0 mA	0.40	0.081	0.36	0.069
	FO01	I_{OL} = 9.0 mA	0.29	0.054	0.28	0.041
	FO02	I_{OL} = 12.0 mA	0.23	0.040	0.25	0.031
	FO03	I_{OL} = 18.0 mA	0.18	0.027	0.17	0.021
	FO06	I_{OL} = 24.0 mA	0.16	0.020	0.16	0.015
	FOIO	PCI	0.66	0.023	0.53	0.020
Low noise	FE04	I_{OL} = 6.0 mA	0.63	0.079	0.60	0.060
	FE01	I_{OL} = 9.0 mA	0.57	0.051	0.51	0.040
	FE02	I_{OL} = 12.0 mA	0.55	0.037	0.45	0.030
	FE03	I_{OL} = 18.0 mA	0.48	0.025	0.43	0.020
	FE06	I_{OL} = 24.0 mA	0.50	0.019	0.42	0.016

Remark The output buffer rise and fall times are rated under the following conditions.
V_{DD} = 3.0 V, T_A = 85°C, and input signal t_r/t_f = 0.4 ns/3.0 V

Table 4-8. List of Coefficients for TTL 5-V Tolerant Output Buffer t_r and t_f Calculations

(a) When output level is between $V_{DD} \times 10\%$ and $V_{DD} \times 90\%$ (MAX.)

Buffer Type	Example	Drive Capacity	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FV0A	I_{OL} = 1.0 mA	7.30	0.414	16.6	0.889
	FV0B	I_{OL} = 2.0 mA	7.28	0.414	8.22	0.449
	FV09	I_{OL} = 3.0 mA	2.55	0.161	5.45	0.295
	FV04	I_{OL} = 6.0 mA	2.56	0.161	1.91	0.104
	FV01	I_{OL} = 9.0 mA	2.01	0.132	1.40	0.082
	FV02	I_{OL} = 12.0 mA	1.27	0.093	0.85	0.048
	FP14	5 V PCI	1.10	0.048	0.72	0.017
Low noise	FW09	I_{OL} = 3.0 mA	3.56	0.154	5.50	0.295
	FW04	I_{OL} = 6.0 mA	3.54	0.154	3.35	0.099
	FW01	I_{OL} = 9.0 mA	3.17	0.125	2.99	0.077
	FW02	I_{OL} = 12.0 mA	2.76	0.092	2.52	0.049
	FW03	I_{OL} = 18.0 mA	2.81	0.092	2.48	0.040
	FW06	I_{OL} = 24.0 mA	2.79	0.092	2.51	0.036

Remark The output buffer rise and fall times are rated under the following conditions.
V_{DD} = 3.0 V, T_A = 85°C, and input signal t_r/t_f = 0.4 ns/3.0 V

(b) When output level is between 0.8 V and 2.0 V (MAX.)

Buffer Type	Example	Drive Capacity	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FV0A	I_{OL} = 1.0 mA	3.10	0.164	7.22	0.383
	FV0B	I_{OL} = 2.0 mA	3.09	0.164	3.63	0.193
	FV09	I_{OL} = 3.0 mA	1.05	0.059	2.36	0.128
	FV04	I_{OL} = 6.0 mA	1.06	0.059	0.82	0.045
	FV01	I_{OL} = 9.0 mA	0.80	0.045	0.61	0.036
	FV02	I_{OL} = 12.0 mA	0.46	0.027	0.36	0.021
	FP14	5 V PCI	0.44	0.020	0.31	0.007
Low noise	FW09	I_{OL} = 3.0 mA	1.46	0.055	2.35	0.128
	FW04	I_{OL} = 6.0 mA	1.43	0.055	1.36	0.042
	FW01	I_{OL} = 9.0 mA	1.35	0.041	1.22	0.033
	FW02	I_{OL} = 12.0 mA	1.19	0.024	1.04	0.020
	FW03	I_{OL} = 18.0 mA	1.20	0.024	1.05	0.016
	FW06	I_{OL} = 24.0 mA	1.19	0.024	1.07	0.015

Remark The output buffer rise and fall times are rated under the following conditions.
V_{DD} = 3.0 V, T_A = 85°C, and input signal t_r/t_f = 0.4 ns/3.0 V

Table 4-9. List of Coefficients for 5-V Output Buffer t_r and t_f Calculations

When output level is between $V_{DD} \times 10\%$ and $V_{DD} \times 90\%$ (MAX.)

Buffer Type	Example	Drive Capacity	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FV0AAL	I_{OL} = 1.0 mA	4.72	0.877	4.76	0.894
	FV0BAL	I_{OL} = 2.0 mA	2.42	0.439	2.46	0.447
	FV09AL	I_{OL} = 3.0 mA	1.70	0.292	1.73	0.298
	FV04AL	I_{OL} = 6.0 mA	1.08	0.144	1.20	0.163
	FV01AL	I_{OL} = 9.0 mA	0.97	0.107	1.07	0.114
	FV02AL	I_{OL} = 12.0 mA	0.90	0.076	1.07	0.083
	FV03AL	I_{OL} = 18.0 mA	0.90	0.052	1.09	0.055
Low noise	FW09AL	I_{OL} = 3.0 mA	2.11	0.288	2.50	0.290
	FW04AL	I_{OL} = 6.0 mA	1.67	0.140	2.06	0.160
	FW02AL	I_{OL} = 12.0 mA	1.62	0.078	1.94	0.093
	FW03AL	I_{OL} = 18.0 mA	1.64	0.058	1.92	0.070

Remark The output buffer rise and fall times are rated under the following conditions.
V_{DD} = 3.0 V / 4.5 V, T_A = 85°C, input signal t_r/t_f = 0.4 ns/3.0 V

Table 4-10. List of Coefficients for 3.3 V-to-2.0 V Output Buffer t_r and t_f Calculations

(a) When output level is between $V_{DD} \times 10\%$ and $V_{DD} \times 90\%$ (MAX.)

Buffer Type	Example	Drive Capacity	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FO09AS	I_{OL} = 3.0 mA	1.47	0.402	1.05	0.294
	FO04AS	I_{OL} = 6.0 mA	0.77	0.201	0.62	0.144
	FO01AS	I_{OL} = 9.0 mA	0.53	0.133	0.45	0.096
	FO02AS	I_{OL} = 12.0 mA	0.43	0.099	0.39	0.072
	FO03AS	I_{OL} = 18.0 mA	0.34	0.066	0.33	0.048
	FO06AS	I_{OL} = 24.0 mA	0.30	0.049	0.31	0.036

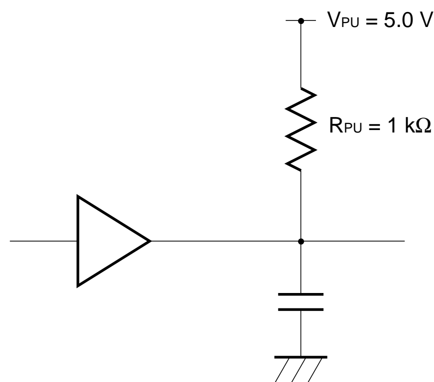
Remark The output buffer rise and fall times are rated under the following conditions.
V_{DD} = 3.0 V, T_A= 85°C, and input signal t_r/t_f = 0.4 ns/3.0 V

(b) When output level is between 0.8 V and 2.0 V (MAX.)

Buffer Type	Example	Drive Capacity	t_{r0}	F_{tr}	t_{f0}	F_{tf}
Normal type	FO09AS	I_{OL} = 3.0 mA	0.59	0.167	0.46	0.128
	FO04AS	I_{OL} = 6.0 mA	0.31	0.083	0.26	0.064
	FO01AS	I_{OL} = 9.0 mA	0.21	0.055	0.19	0.043
	FO02AS	I_{OL} = 12.0 mA	0.17	0.041	0.16	0.032
	FO03AS	I_{OL} = 18.0 mA	0.13	0.027	0.13	0.021
	FO06AS	I_{OL} = 24.0 mA	0.12	0.020	0.12	0.016

Remark The output buffer rise and fall times are rated under the following conditions.
V_{DD} = 3.0 V, T_A= 85°C, and input signal t_r/t_f = 0.4 ns/3.0 V

Equivalent circuit



4.5.2 Recommended load capacitance range for output buffers

The recommended load capacitance range $C_{L\ (MAX.)}$ for output buffers is $C_{L\ (MAX.)} \leq 300$ pF. Table 4-10 lists recommended load capacitance ranges for various output buffer drive capacities. Select the appropriate output buffer from among those listed in Table 4-11. If you use a load capacitance that is above or below the recommended load capacitance range, a larger overshoot or undershoot may occur in the output signal.

Table 4-11. Recommended Load Capacitance Ranges (pF) for Output Buffers

Buffer Type	Example	Drive Capacity	Recommended Load Capacitance Range (pF)
LVTTL interface Normal type	FO09	I_{OL} = 3.0 mA	0 to 40
	FO04	I_{OL} = 6.0 mA	0 to 80
	FO01	I_{OL} = 9.0 mA	10 to 125
	FO02	I_{OL} = 12.0 mA	30 to 170
	FO03	I_{OL} = 18.0 mA	75 to 250
	FO06	I_{OL} = 24.0 mA	110 to 300
LVTTL interface Low noise type	FE04	I_{OL} = 6.0 mA	0 to 95
	FE01	I_{OL} = 9.0 mA	0 to 143
	FE02	I_{OL} = 12.0 mA	0 to 191
	FE03	I_{OL} = 18.0 mA	0 to 200
	FE06	I_{OL} = 24.0 mA	0 to 200
TTL 5-V tolerant interface Normal type	FV0A	I_{OL} = 1.0 mA	0 to 5
	FV0B	I_{OL} = 2.0 mA	0 to 25
	FV09	I_{OL} = 3.0 mA	0 to 40
	FV04	I_{OL} = 6.0 mA	0 to 110
	FV01	I_{OL} = 9.0 mA	0 to 150
	FV02	I_{OL} = 12.0 mA	35 to 200
TTL 5-V tolerant interface Low noise type	FW09	I_{OL} = 3.0 mA	0 to 48
	FW04	I_{OL} = 6.0 mA	0 to 88
	FW01	I_{OL} = 9.0 mA	0 to 102
	FW02	I_{OL} = 12.0 mA	0 to 126
	FW03	I_{OL} = 18.0 mA	0 to 126
	FW06	I_{OL} = 24.0 mA	0 to 126
5-V interface Normal type	FV0AAL	I_{OL} = 1.0 mA	0 to 25
	FV0BAL	I_{OL} = 2.0 mA	0 to 50
	FV09AL	I_{OL} = 3.0 mA	0 to 85
	FV04AL	I_{OL} = 6.0 mA	0 to 150
	FV01AL	I_{OL} = 9.0 mA	5 to 230
	FV02AL	I_{OL} = 12.0 mA	20 to 290
	FV03AL	I_{OL} = 18.0 mA	50 to 300
5-V interface Low noise type	FW09AL	I_{OL} = 3.0 mA	0 to 87
	FW04AL	I_{OL} = 6.0 mA	0 to 160
	FW02AL	I_{OL} = 12.0 mA	0 to 200
	FW03AL	I_{OL} = 18.0 mA	0 to 200

4.5.3 Maximum operating frequency of output buffers

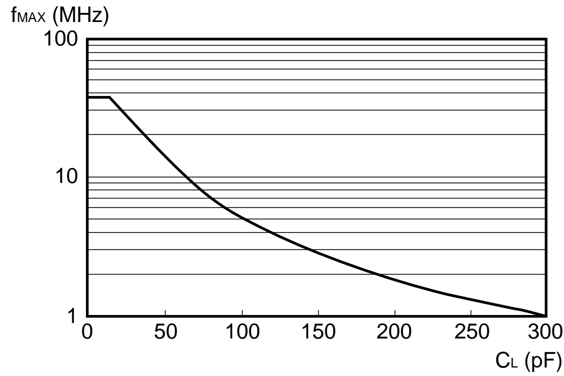
The output buffers' maximum operating frequency is determined based on the drive capacity and load capacitance. As was described above in **4.5.2 Recommended load capacitance range for output buffers**, there are recommended ranges for load capacitance. Refer to Figures 4-12 to 4-17.

Note with caution that a larger overshoot or undershoot may occur in the ranges indicated by diagonal lines.

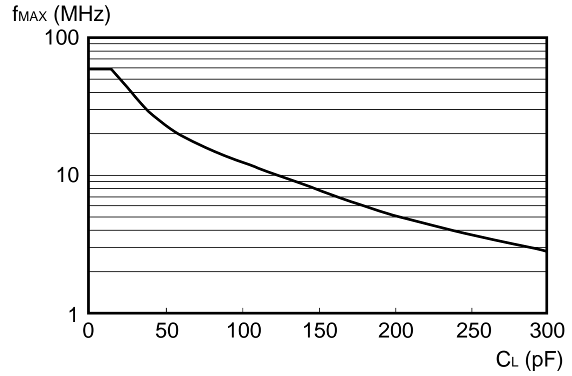
The maximum operating frequency values shown in Figures 4-12 to 4-17 are rated assuming that the capacitance is connected only to the output pin. Therefore, results will vary slightly in cases where inductance is also considered. Also, the output waveform of the 5-V interface may vary greatly depending on the pull-up resistance, so the output waveform shown here only applies to certain conditions.

Figure 4-12. $f_{MAX.}$ vs. C_L Restriction (LVTTL Interface, Normal Type)

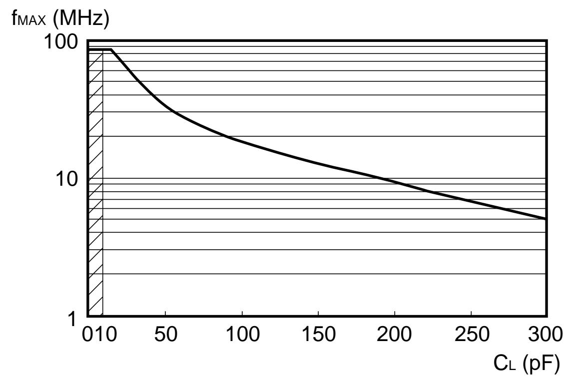
(a) FO09 (I_{OL} = 3.0 mA)



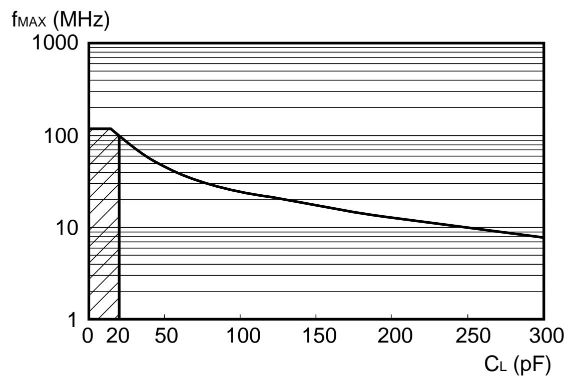
(b) FO04 (I_{OL} = 6.0 mA)



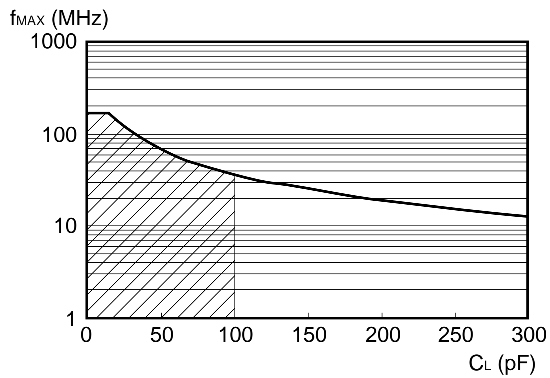
(c) FO01 (I_{OL} = 9.0 mA)



(d) FO02 (I_{OL} = 12.0 mA)



(e) FO03 (I_{OL} = 18.0 mA)



(f) FO06 (I_{OL} = 24.0 mA)

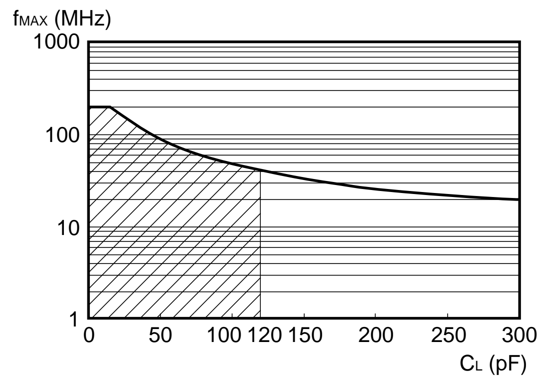
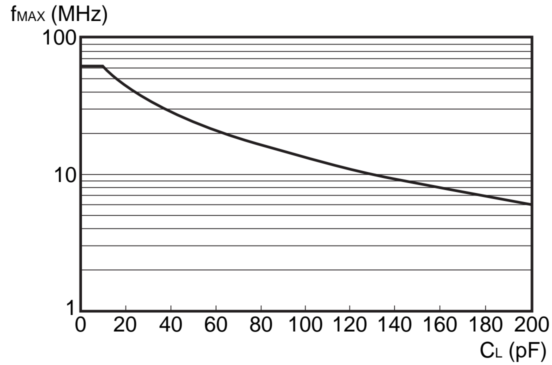
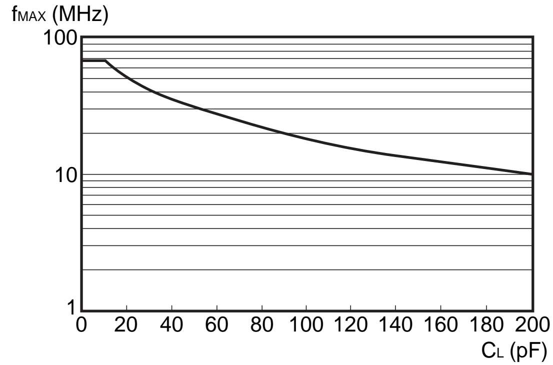


Figure 4-13. $f_{MAX.}$ vs. C_L Restriction (LVTTL Interface, Low Noise)

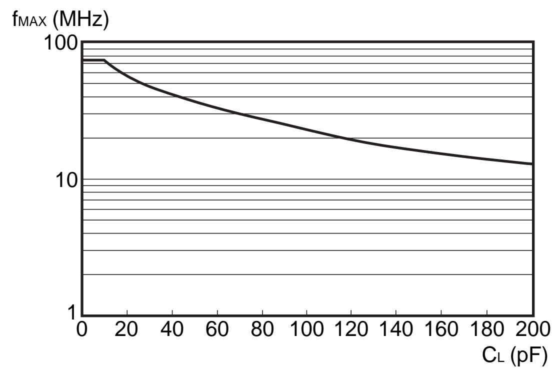
(a) FE04 (I_{OL} = 6.0 mA)



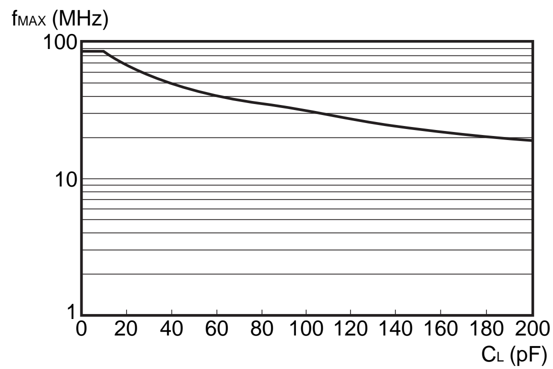
(b) FE01 (I_{OL} = 9.0 mA)



(c) FE02 (I_{OL} = 12.0 mA)



(d) FE03 (I_{OL} = 18.0 mA)



(e) FE06 (I_{OL} = 24.0 mA)

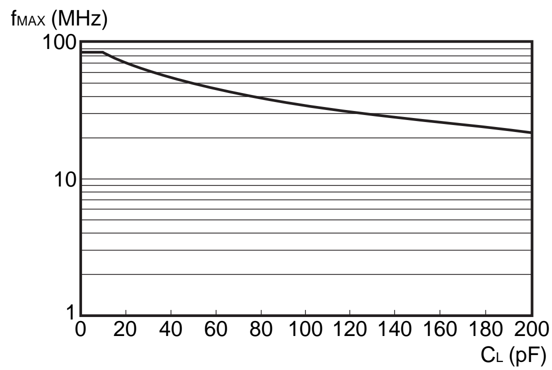
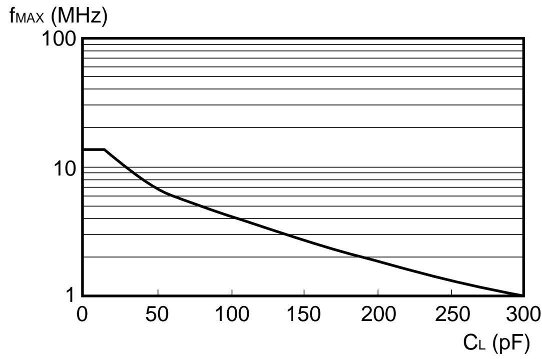
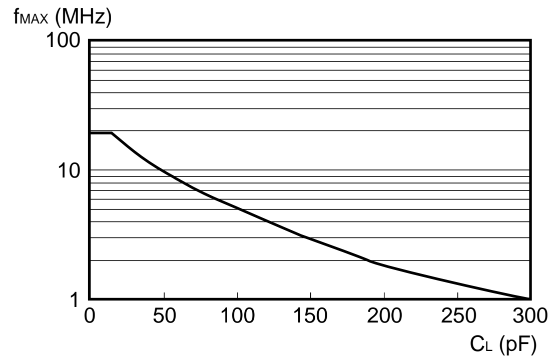


Figure 4-14. $f_{MAX.}$ vs. C_L Restriction (TTL 5-V Tolerant Interface, Normal Type)

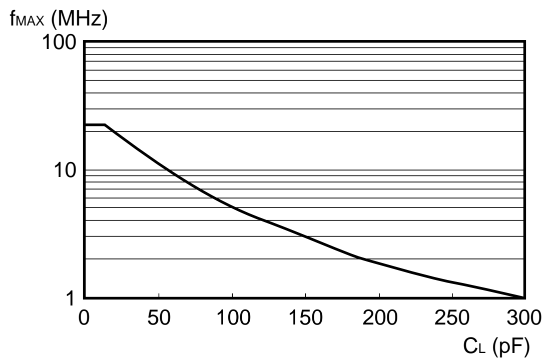
(a) FV0A (I_{OL} = 1.0 mA)



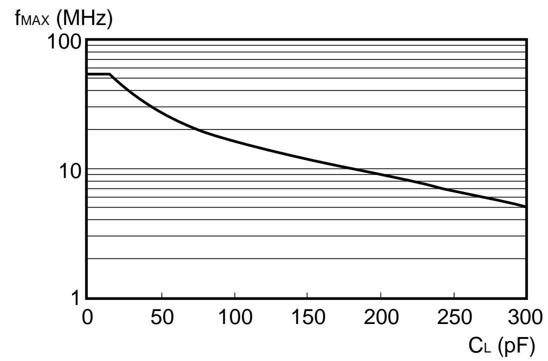
(b) FV0B (I_{OL} = 2.0 mA)



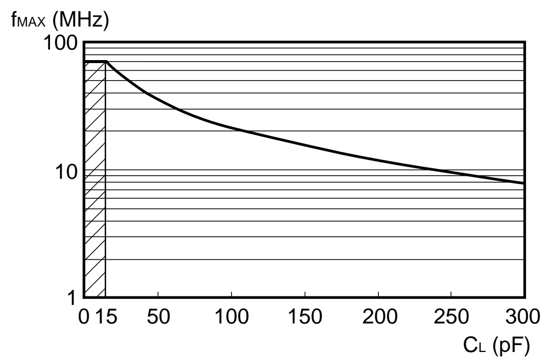
(c) FV09 (I_{OL} = 3.0 mA)



(d) FV04 (I_{OL} = 6.0 mA)



(e) FV01 (I_{OL} = 9.0 mA)



(f) FV02 (I_{OL} = 12.0 mA)

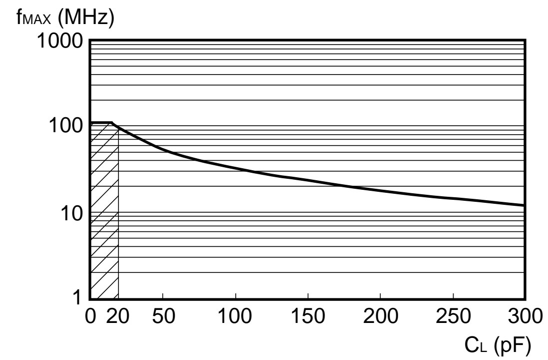
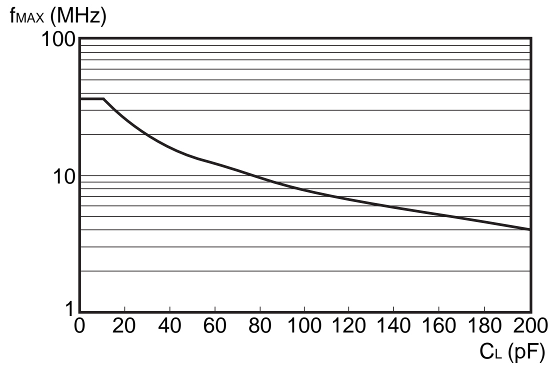
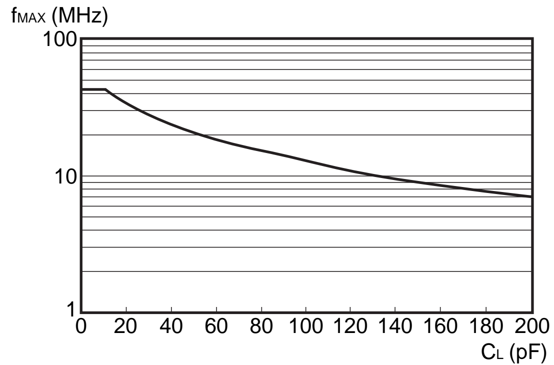


Figure 4-15. $f_{MAX.}$ vs. C_L Restriction (TTL 5-V Tolerant Interface, Low Noise)

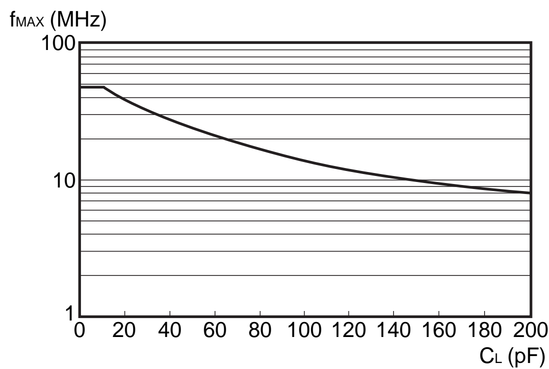
(a) FW09 (I_{OL} = 3.0 mA)



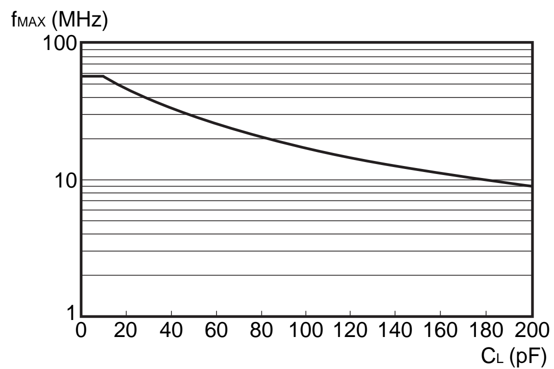
(b) FW04 (I_{OL} = 6.0 mA)



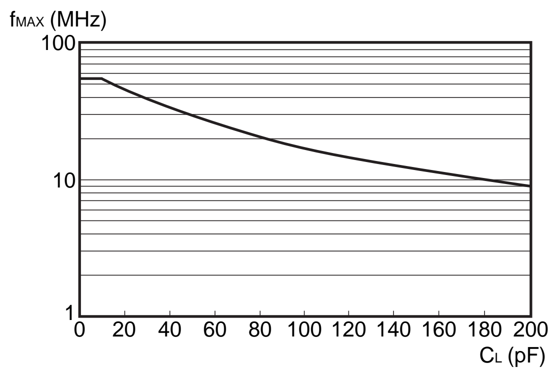
(c) FW01 (I_{OL} = 9.0 mA)



(d) FW02 (I_{OL} = 12.0 mA)



(e) FW03 (I_{OL} = 18.0 mA)



(f) FW06 (I_{OL} = 24.0 mA)

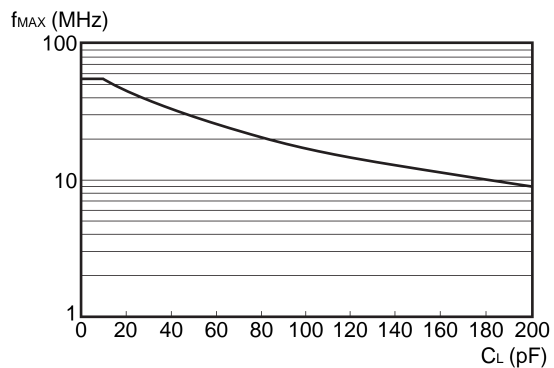
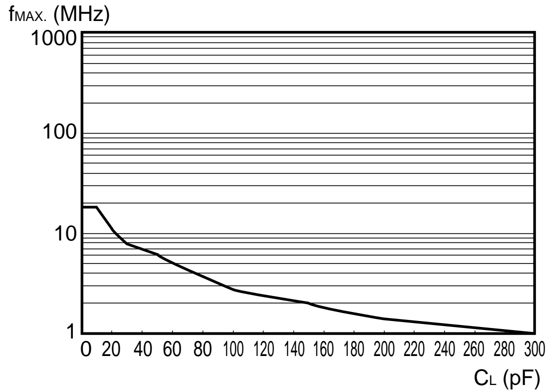
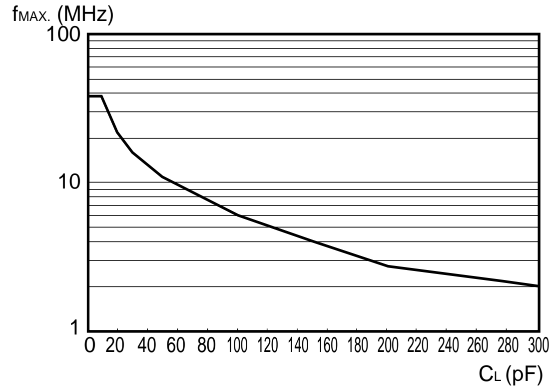


Figure 4-16. $f_{MAX.}$ vs. C_L Restriction (5-V Interface, Normal Type) (1/2)

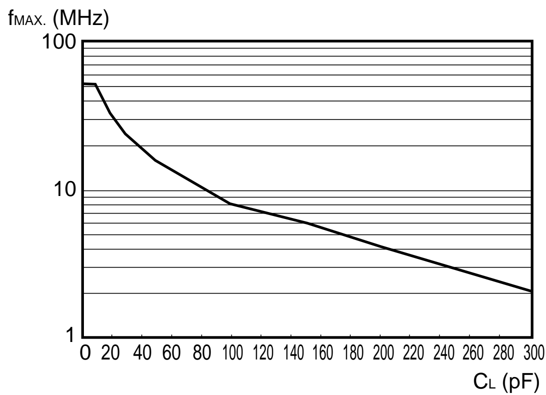
(a) FV0AAL (I_{OL} = 1.0 mA)



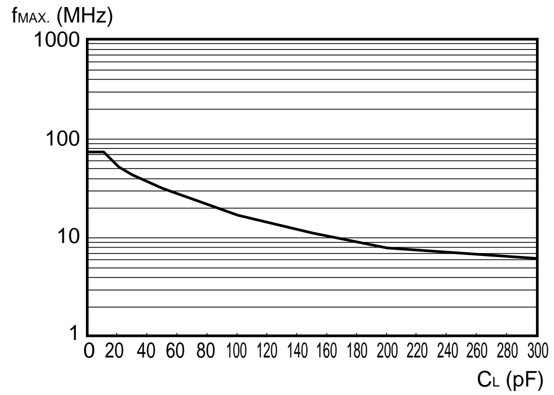
(b) FV0BAL (I_{OL} = 2.0 mA)



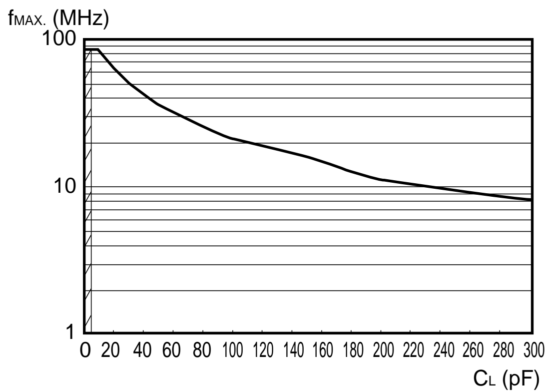
(c) FV09AL (I_{OL} = 3.0 mA)



(d) FV04AL (I_{OL} = 6.0 mA)



(e) FV01AL (I_{OL} = 9.0 mA)



(f) FV02AL (I_{OL} = 12.0 mA)

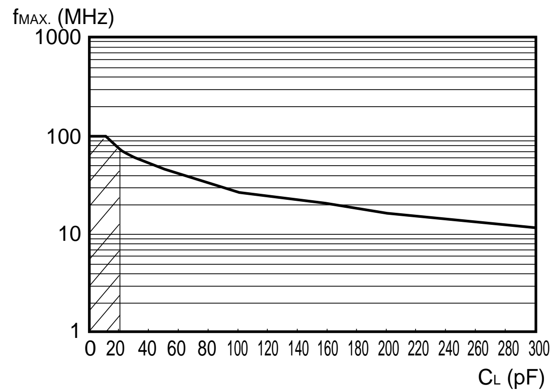


Figure 4-16. $f_{MAX.}$ vs. C_L Restriction (5-V Interface, Normal Type) (2/2)

(g) FV03AL (I_{OL} = 18.0 mA)

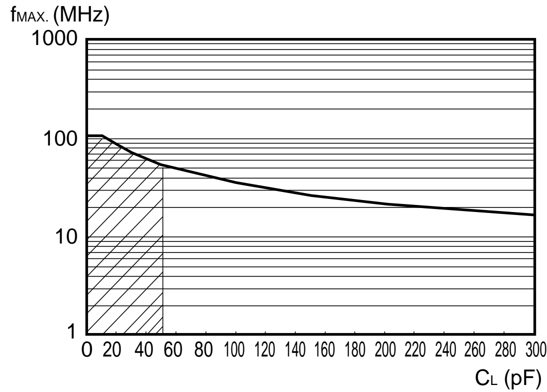
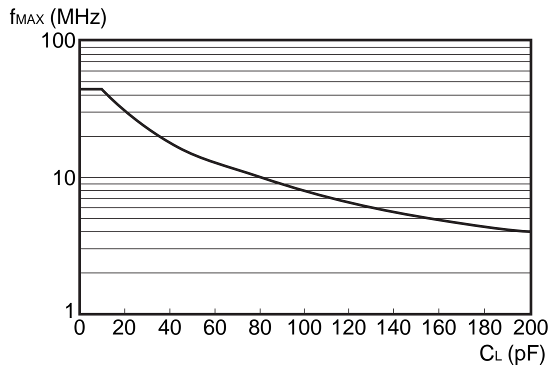
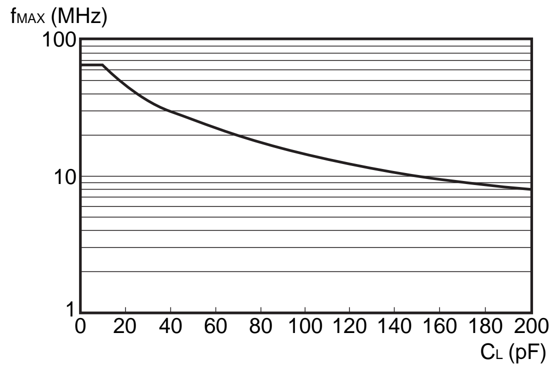


Figure 4-17. $f_{MAX.}$ vs. C_L Restriction (5-V Interface, Low Noise)

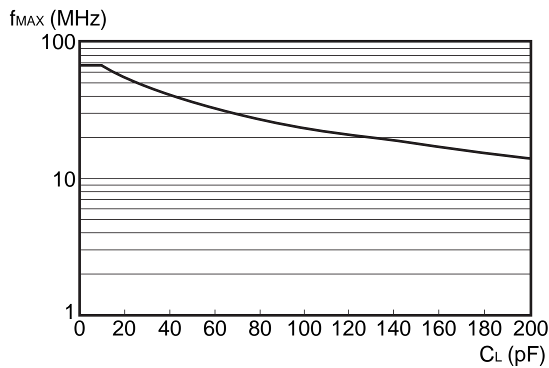
(a) FW09AL (I_{OL} = 3.0 mA)



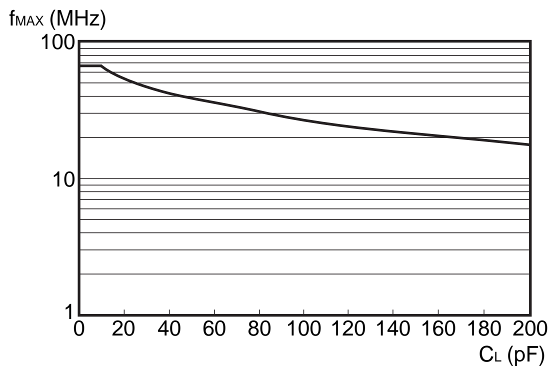
(b) FW04AL (I_{OL} = 6.0 mA)



(c) FW02AL (I_{OL} = 12.0 mA)



(d) FW03AL (I_{OL} = 18.0 mA)



4.5.4 Output buffer output currents (I_{OL}, I_{OH})

At NEC, the output currents of cell-based ICs are defined as V_{OL} = 0.4 V and V_{OH} = 2.4 V. However, since it is possible to use different V_{OL} and V_{OH} values in actual applications, the following coefficient should be used to estimate the I_{OL} and I_{OH} characteristics according to the use conditions.

- Dependence corresponding to output voltage

  V_{OL} = 0.4 V to 0.6 V, V_{OH} = (V_{DD} – 0.4 V) to (V_{DD} – 0.6 V)

  Since I_{OL} and I_{OH} change almost in proportion to the output voltage, direction approximation can be used. However, the TTL-level output buffer's I_{OH} value is excluded.

  Approximation method

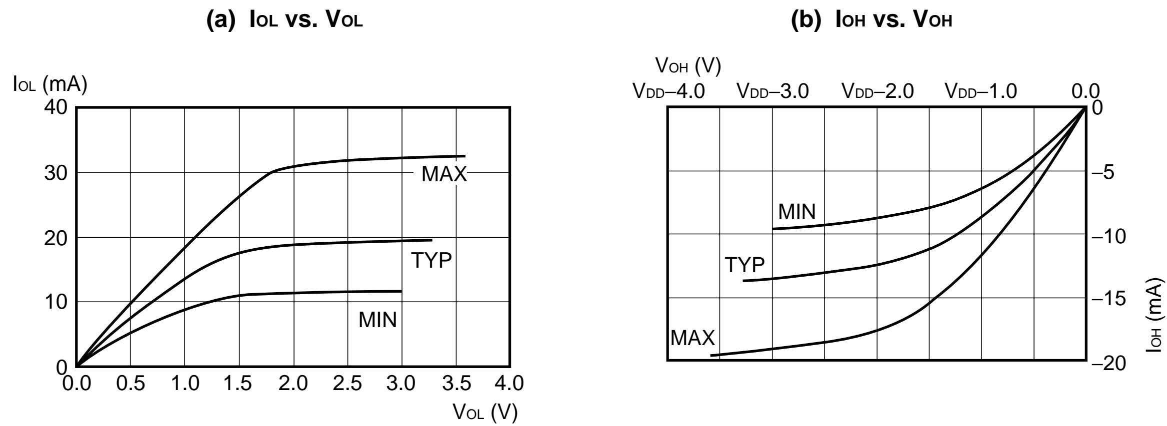
$I_{OL}' = I_{OL} \times V_{OL} / 0.4$	(mA)
$I_{OH}' = I_{OH} \times (V_{DD} - V_{OH}) / 0.6$	(mA)

  I_{OL}: I_{OL} specification when V_{OL} = 0.4 V
  V_{OL}: V_{OL} value being used
  I_{OH}: I_{OH} specification when V_{OH} = 2.4 V
  V_{OH}: V_{OH} value being used

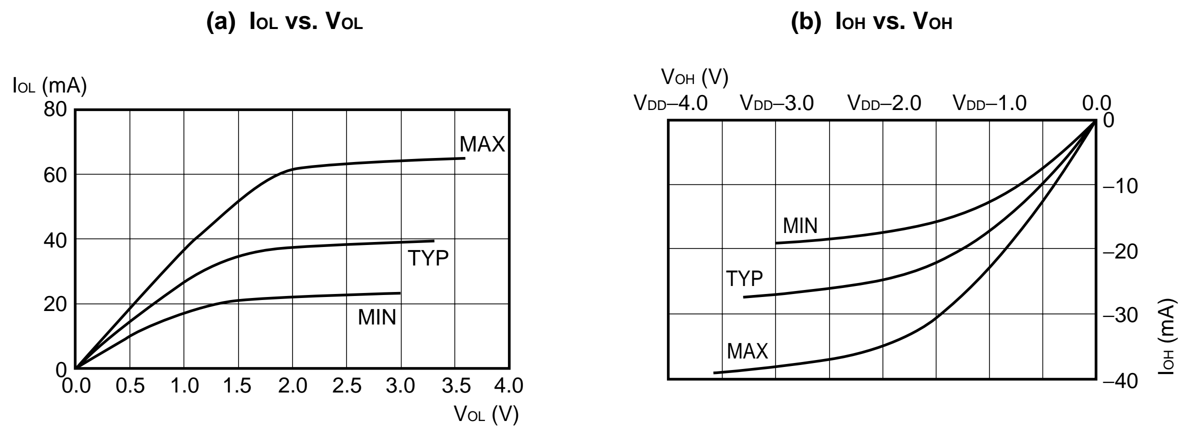
I_O vs. V_O curves are shown below. In each graph, the MIN. curve corresponds to the conditions "V_{DD} = 3.0 V, T_J = 125°C", the TYP. curve corresponds to the conditions "V_{DD} = 3.3 V, T_J = 25°C", and the MAX. curve corresponds to the conditions "V_{DD} = 3.6 V, T_J = –40°C". The actually used DC I_{OH} and I_{OL} must be within the absolute maximum ratings. The 5-V output buffer uses a configuration in which the DC I_{OH} is interrupted, and therefore curves cannot be shown for I_O vs. V_O under MIN. and MAX. conditions.

Figure 4-18. I_O vs. V_O (1/7)

(1) LVTTL interface I_{OL} = 3 mA (typical block type: FO09)



(2) LVTTL interface I_{OL} = 6 mA (typical block type: FO04, FE04)



(3) LVTTL interface I_{OL} = 9 mA (typical block type: FO01, FE01)

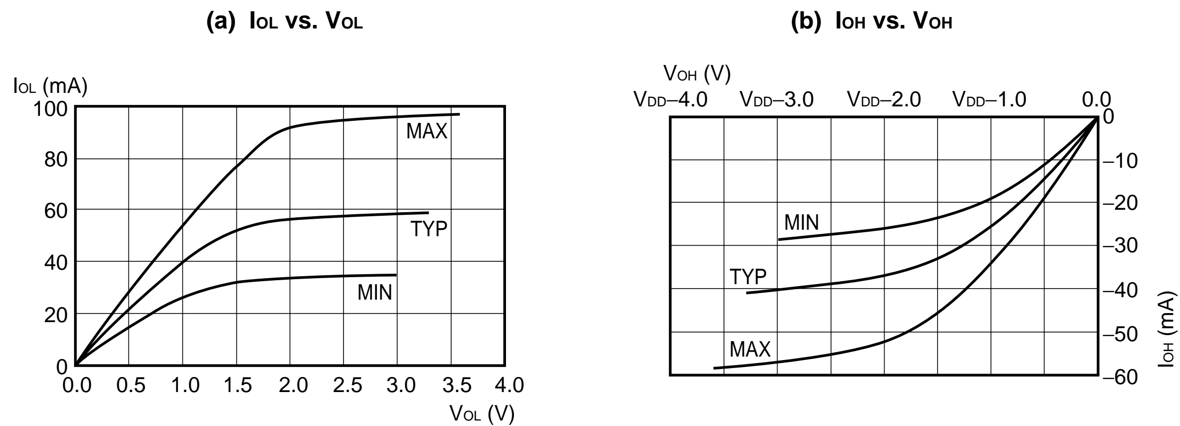
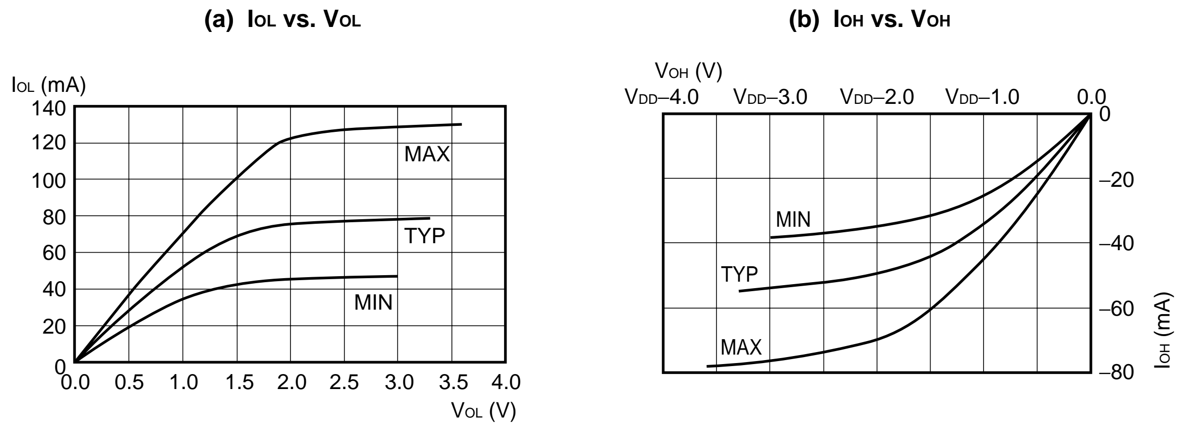
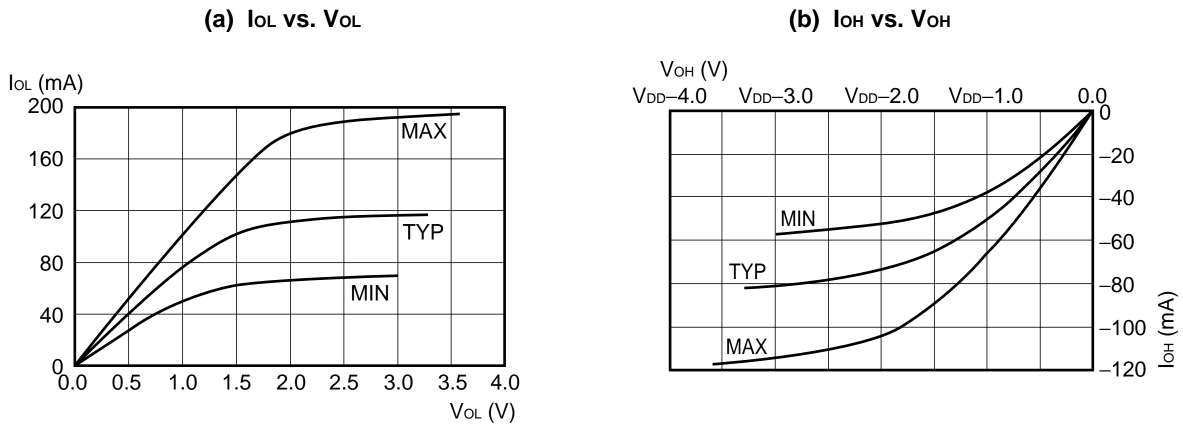


Figure 4-18. I_O vs. V_O (2/7)

(4) LVTTL interface I_{OL} = 12 mA (typical block type: FO02, FE02)



(5) LVTTL interface I_{OL} = 18 mA (typical block type: FO03, FE03)



(6) LVTTL interface I_{OL} = 24 mA (typical block type: FO06, FE06)

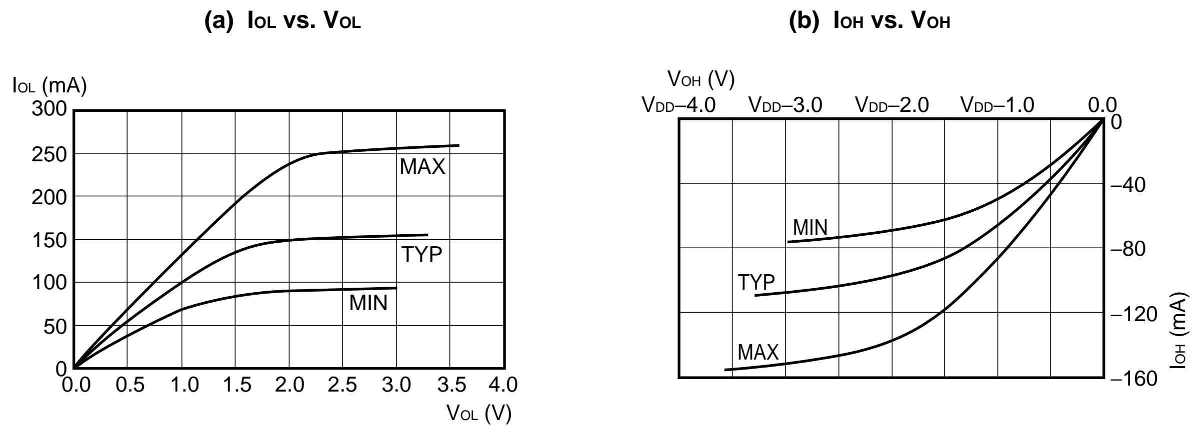
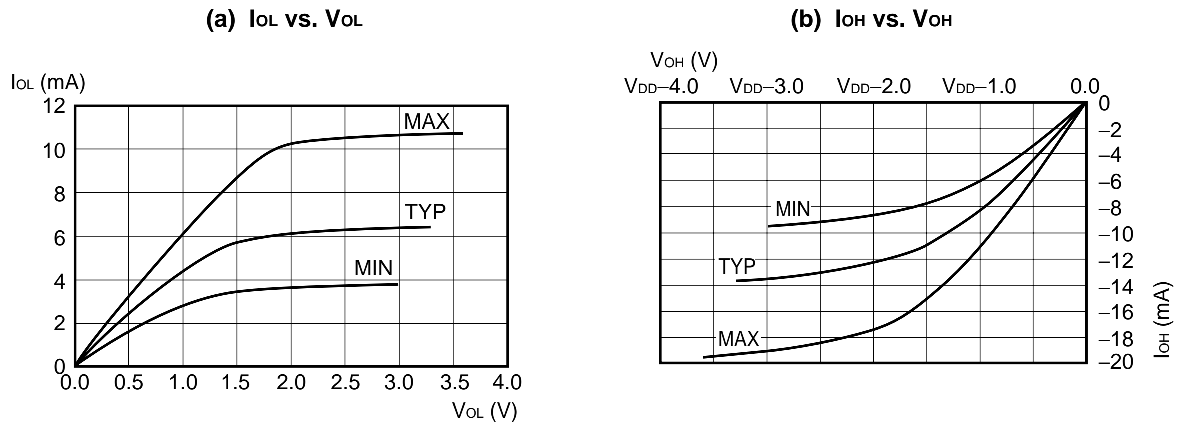
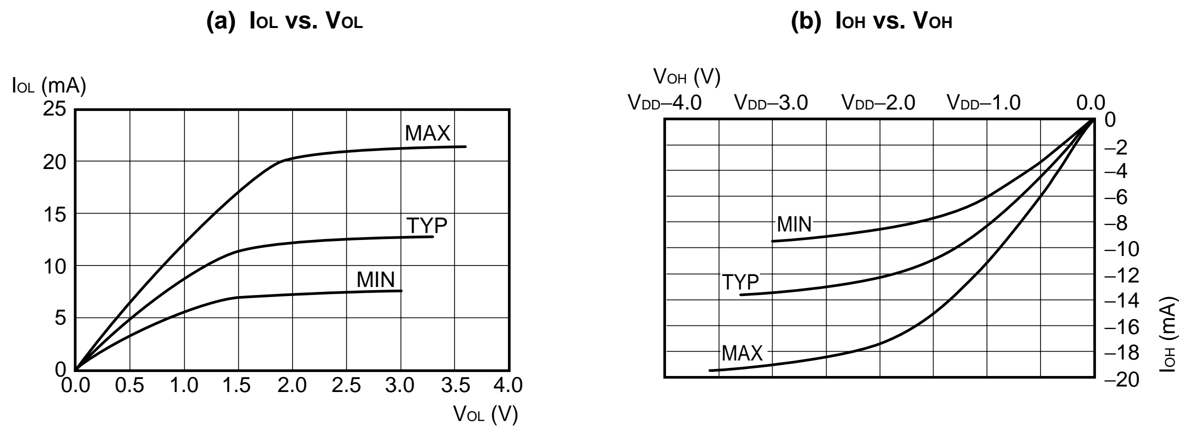


Figure 4-18. I_O vs. V_O (3/7)

(7) TTL 5-V tolerant I_{OL} = 1 mA (typical block type: FV0A)



(8) TTL 5-V tolerant I_{OL} = 2 mA (typical block type: FV0B)



(9) TTL 5-V tolerant I_{OL} = 3 mA (typical block type: FV09, FW09)

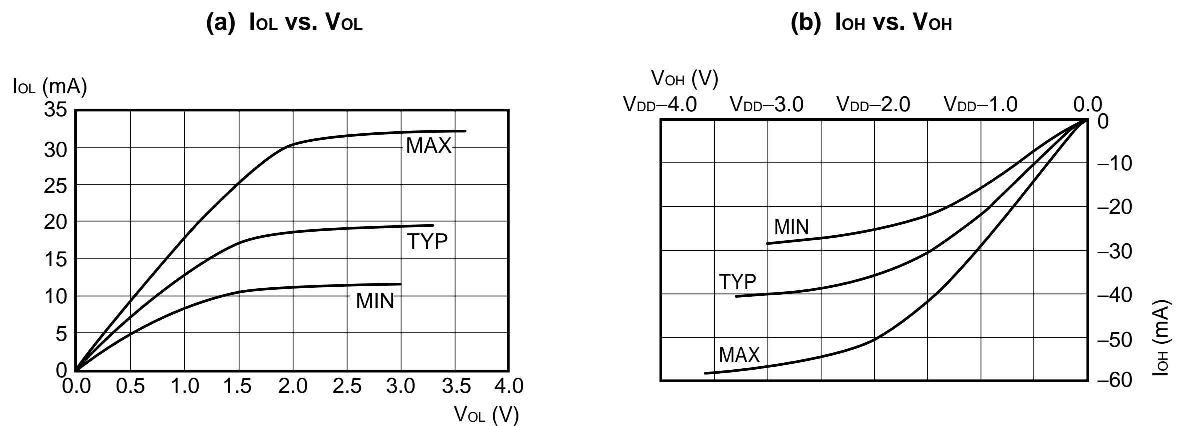
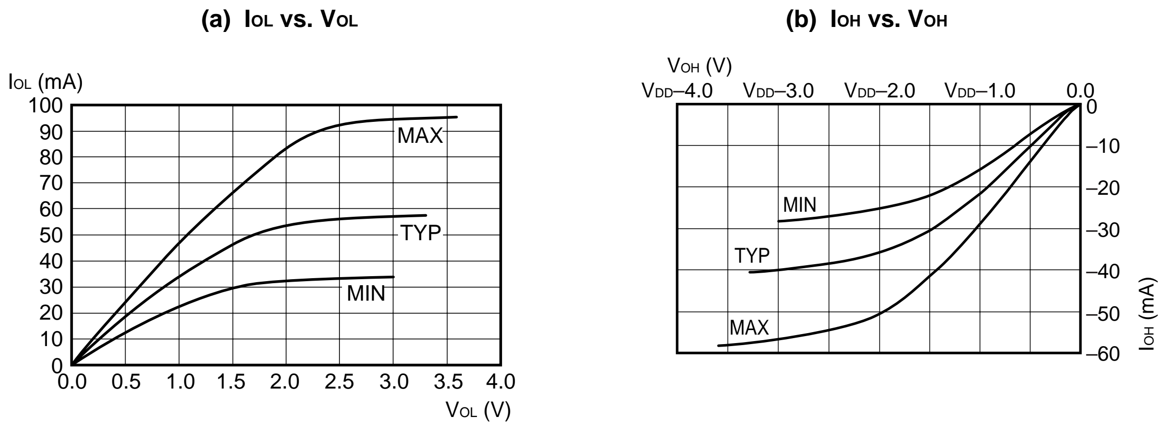
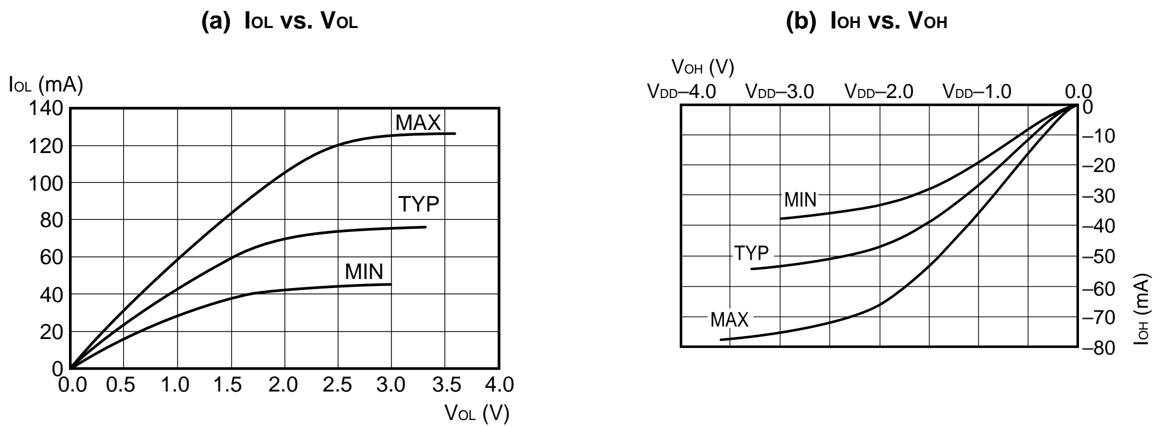


Figure 4-18. I_O vs. V_O (4/7)

(10) TTL 5-V tolerant I_{OL} = 6 mA (typical block type: FV04, FW04)



(11) TTL 5-V tolerant I_{OL} = 9 mA (typical block type: FV01, FW01)



(12) TTL 5-V tolerant I_{OL} = 12 mA (typical block type: FV02, FW02)

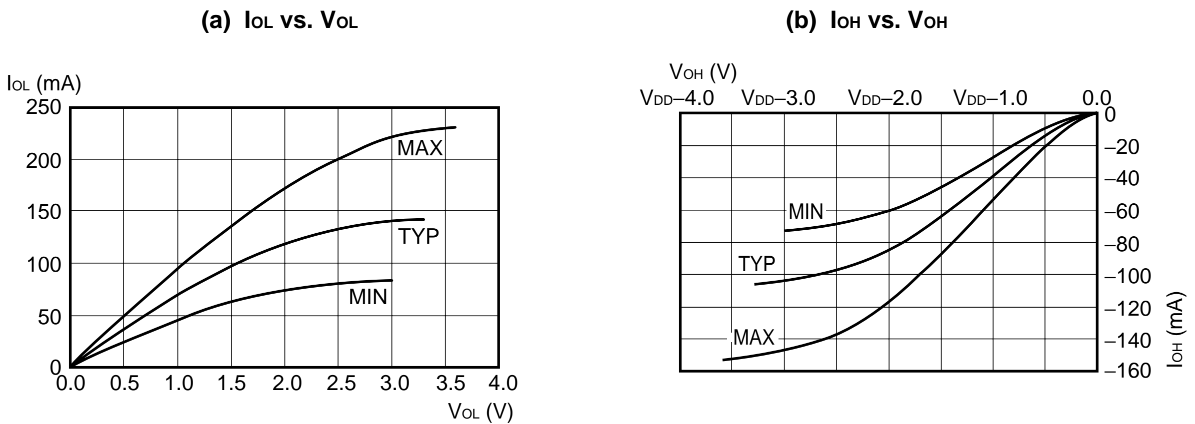
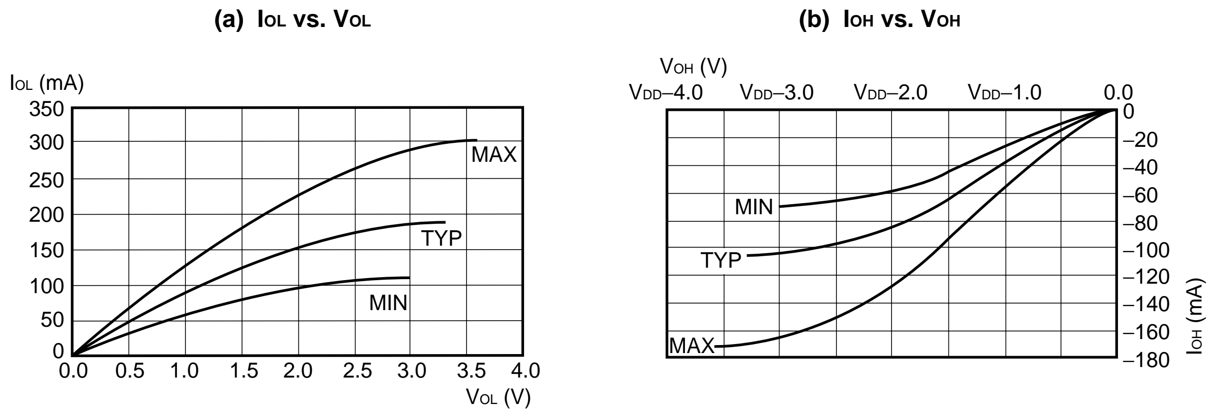
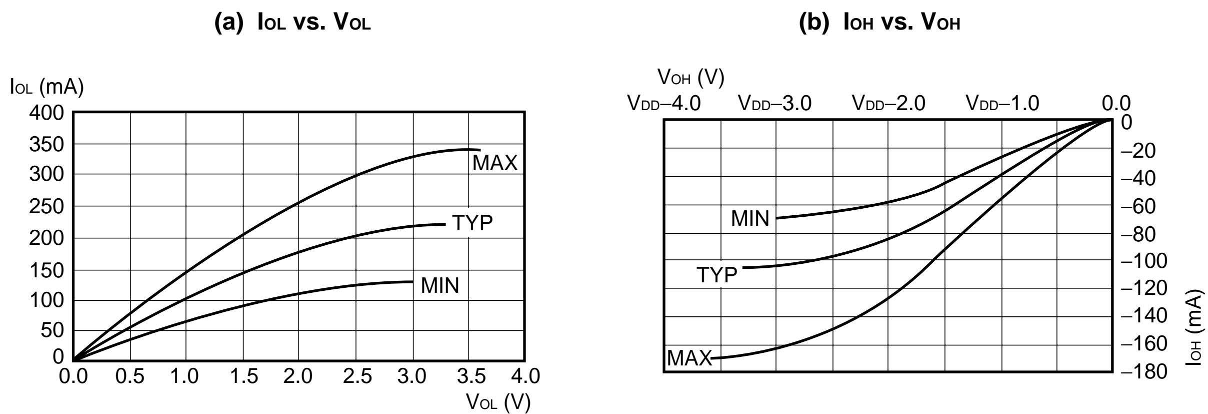


Figure 4-18. I_O vs. V_O (5/7)

(13) TTL 5-V tolerant I_{OL} = 18 mA (typical block type: FW03)



(14) TTL 5-V tolerant I_{OL} = 24 mA (typical block type: FW06)



(15) 5-V interface I_{OL} = 1 mA (typical block type: FV0AAL)

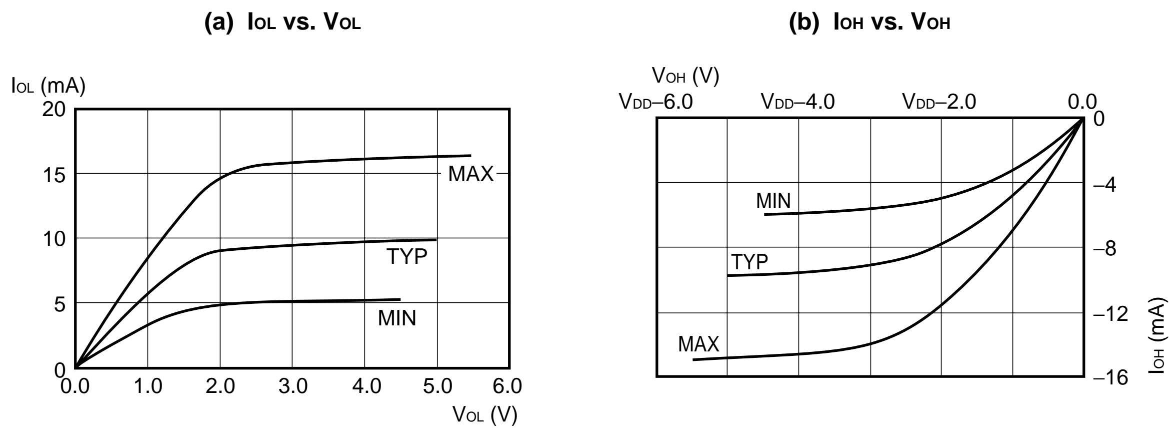
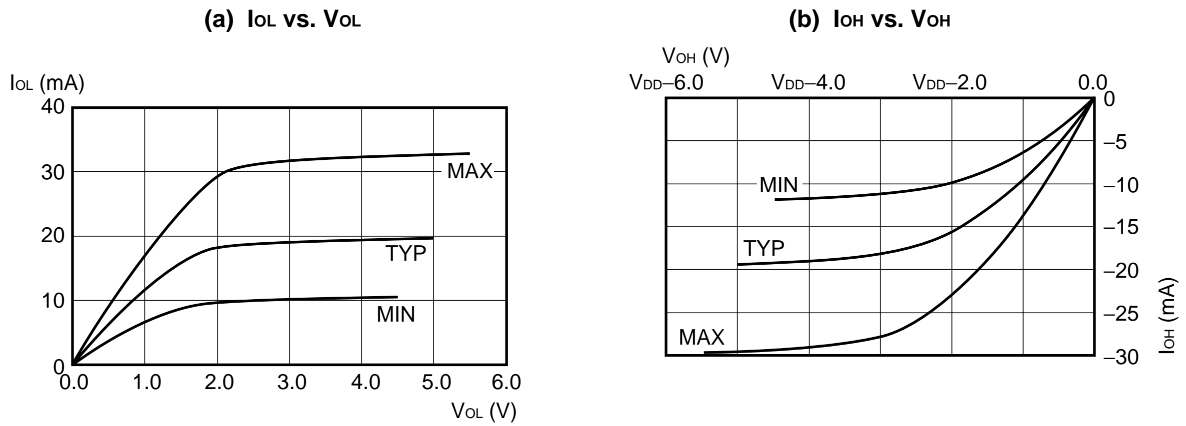
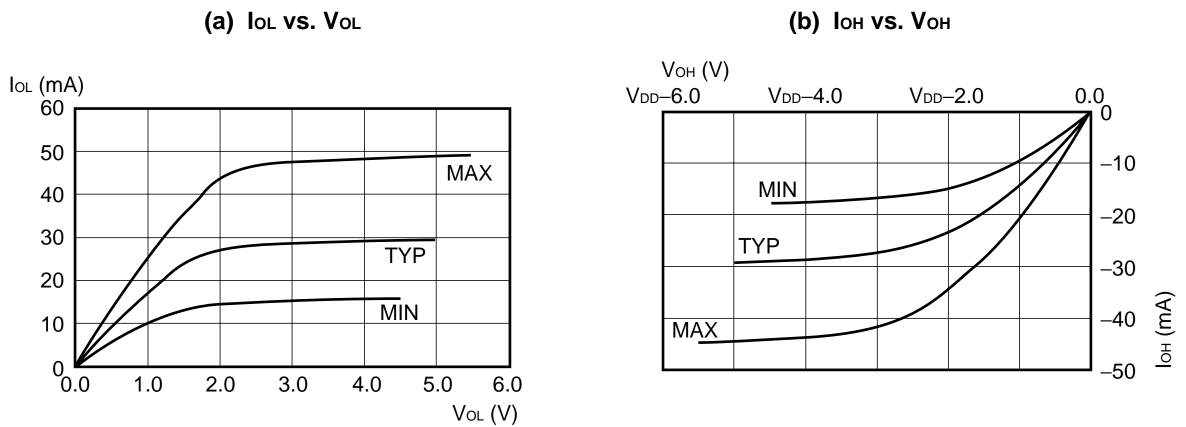


Figure 4-18. I_O vs. V_O (6/7)

(16) 5-V interface I_{OL} = 2 mA (typical block type: FV0BAL)



(17) 5-V interface I_{OL} = 3 mA (typical block type: FV09AL, FW09AL)



(18) 5-V interface I_{OL} = 6 mA (typical block type: FV04AL, FW04AL)

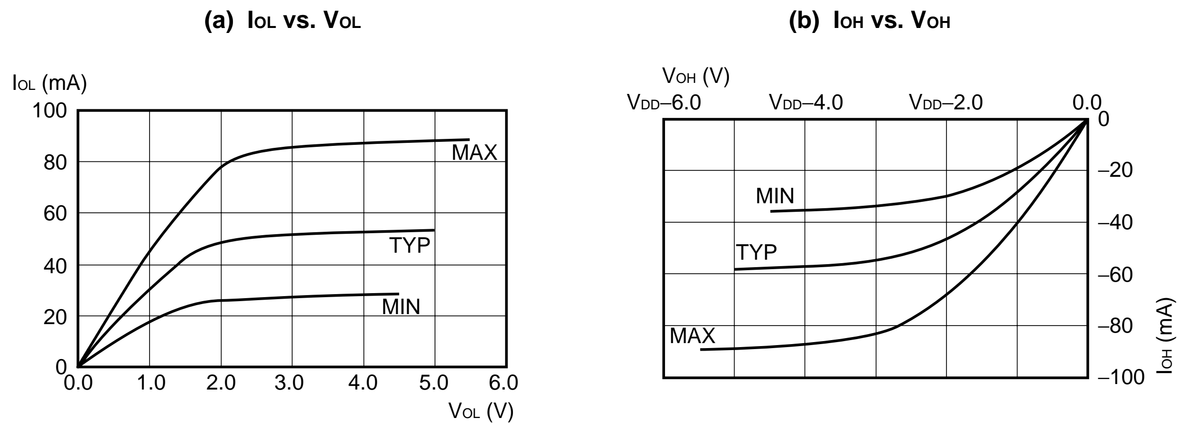
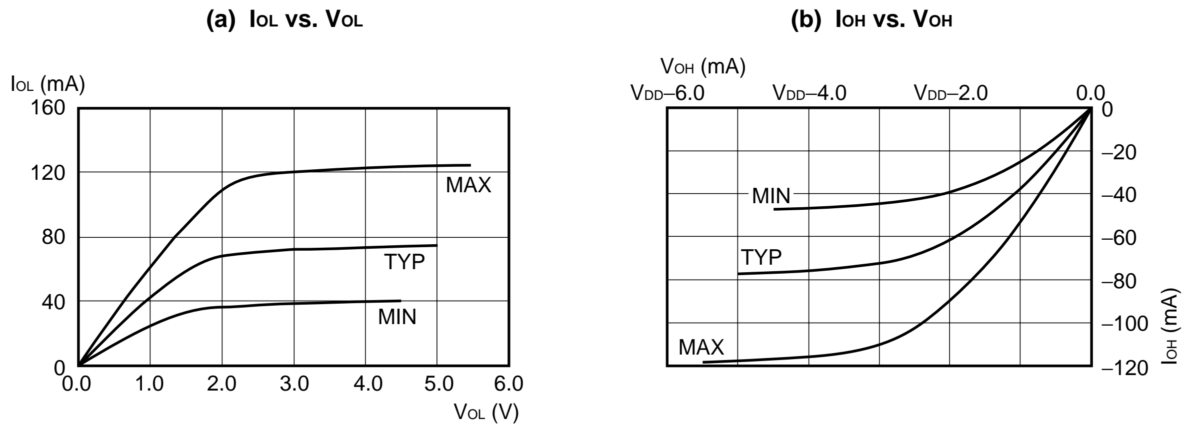
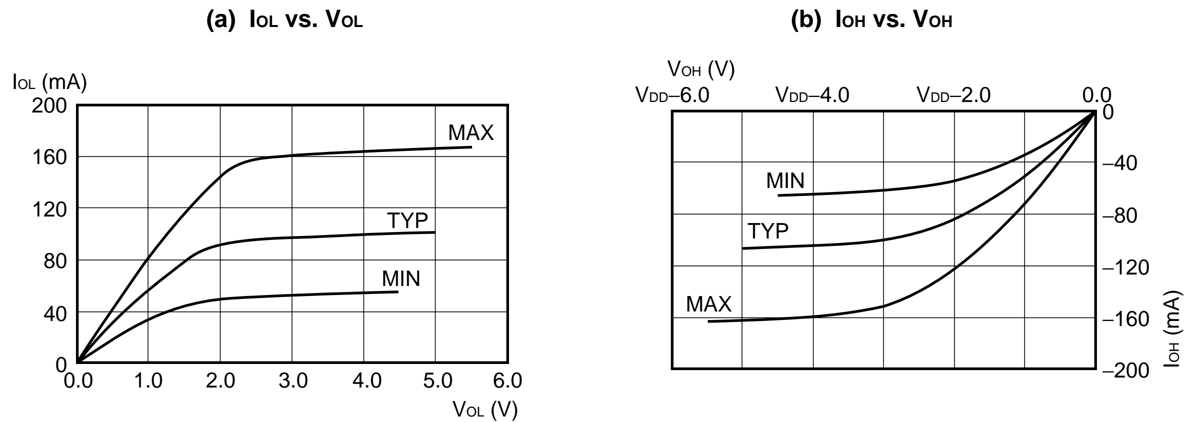


Figure 4-18. I_O vs. V_O (7/7)

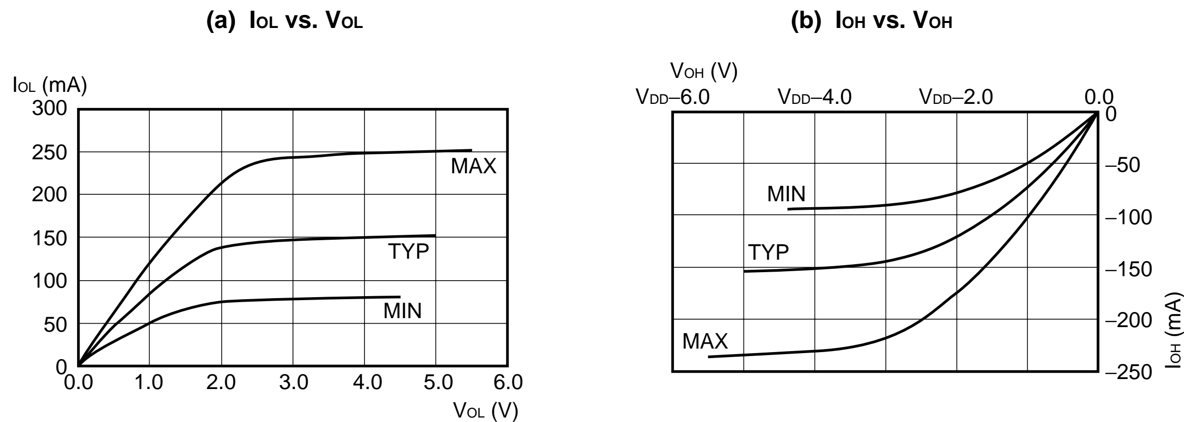
(19) 5-V interface I_{OL} = 9 mA (typical block type: FV01AL, FW01AL)



(20) 5-V interface I_{OL} = 12 mA (typical block type: FV02AL, FW02AL)



(21) 5-V interface I_{OL} = 18 mA (typical block type: FV03AL, FW03AL)



4.6 Simultaneous Switching Limits of Output Buffers

In recent years, the number of bus lines in systems has increased from 32 to 64. Moreover, because higher speed has been required of systems, the signal switching speed of the bus lines has also increased. Consequently, the frequency at which simultaneous switching takes place has significantly increased, causing the likelihood of systems to misoperate due to noise to increase. This section explains simultaneous switching.

4.6.1 Misoperation caused by simultaneous switching

When an output buffer switches from low to high or high to low, the current that charges or discharges the output load capacitance momentarily flows into the power supply or GND line via the output buffer. Where the charge/discharge current is i and the inductance of power supply is L, the noise that may be generated is expressed as $-L \times \Delta i/\Delta t$. This reveals that the noise that may be generated increases in proportion to changes in the charge/discharge current and the inductance of the power supply. The value of $\Delta i/\Delta t$ is determined by the type of the output buffer. Generally, the higher the drive capability of the output buffer, the greater the value of di/dt (more accurately, because the value of $\Delta i/\Delta t$ is determined by the drive capability of a large-size transistor at the output stage and the input rise and fall times (t_r/t_f) of that transistor, the value of $\Delta i/\Delta t$ of the low noise is lower than the output buffer having the same drive capability). As the number of bus lines that switches simultaneously increases, this transient charge/discharge current increases, causing the noise superimposed on the power supply or GND line to increase. As a result, the system misoperates.

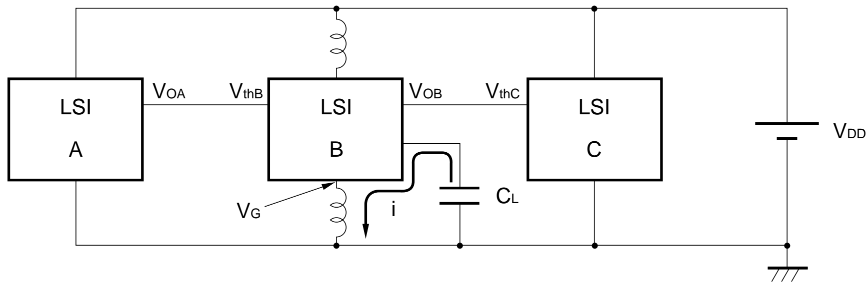
These are two types of misoperations as follows:

<1> Misoperation due to fluctuation in LSI input threshold level
<2> Next stage circuit misoperation due to noise appearing at LSI output pin

The circuit in Figure 4-19 (a) can be considered when the LSI B output buffer is switched from “H” to “L”. When this happens, the load discharge current flows to the GND line of the printed circuit board via the output buffer of LSI B and the internal GND line of the LSI. As a result of this discharge current, a counter electromotive force is generated by the inductance of the GND line and the GND level V_G inside the LSI rises, causing misoperation as shown in Figures 4-19 (b) and (c). If the output buffer is switched from “L” to “H”, the charge current flows into the load capacitance, noise is generated on the power supply line, and consequently, the internal V_{DD} level of the LSI temporarily falls.

Figure 4-19. Misoperation Due to Simultaneous Switching

(a) Circuit diagram



V_{OA}: Output level of LSI A

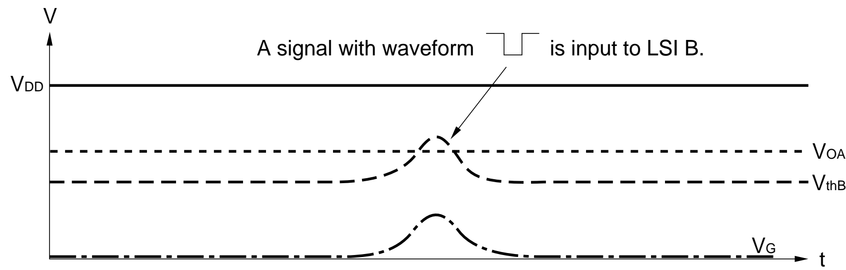
V_{OB}: Output level of LSI B

V_{thB}: Input threshold level of LSI B

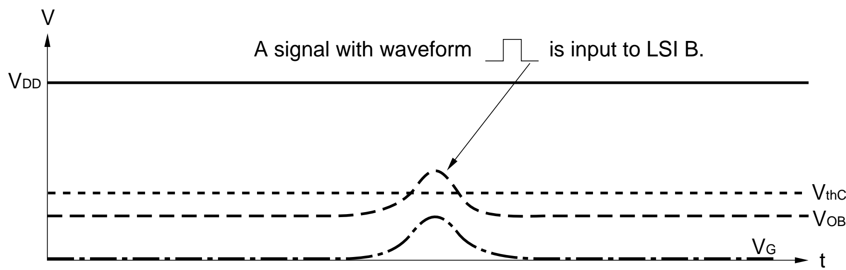
V_{thC}: Input threshold level of LSI C

V_G: GND level of LSI B

(b) Fluctuation of input threshold level of LSI B



(c) Noise generation on output pin of LSI B



4.6.2 SSO factors

When an output buffer operates, a current that charges and discharges the load capacitance runs between the load and the LSI. When this charge/discharge current exceeds the standard value, noise is caused in the power supply line, the input threshold fluctuates, and noise occurs at the output pin.

The SSO (Simultaneous Switching Output) limits for output buffers vary according to the following factors.

- Number of power supply pins (V_{DD} and GND)
- Load capacitance value (C_L)
- Load driving potential of used output buffer
- Input interface level type
- Output interface level type

Refer to **4.6.4 Method for judging SSO limit** for various SSO limits for output buffers . Moreover, SSO is influenced by the GND and power supply wiring pattern on the mounting board, and therefore, noise may be generated even when NEC-specified limits are observed. When performing board design, be sure to implement adequate noise countermeasures.

4.6.3 Determining number of SSO

Judging SSO is done by observing several output buffers that swing in the same direction within the limitation time. (See Table 4-12). When there are several SSO combinations, judge each on its own.

The method for counting changes in the same direction differs depending on the type of buffers.

<1> Normal output buffer

- The changes “1” → “0”, “X” → “0”, or “1” → “X” are counted as signal changes in the “0” direction.
- The changes “0” → “1”, “X” → “1”, or “0” → “X” are counted as signal changes in the “1” direction.

<2> 3-state buffer

- The changes “1” → “0”, “HZ” → “0”, “X” → “0”, or “1” → “X” are counted as signal changes in the “0” direction.
- The changes “0” → “1”, “HZ” → “1”, “X” → “1”, or “0” → “X” are counted as signal changes in the “1” direction.

<3> Bidirectional buffer

- The output changes “1” → “0” , “X” → “0” , or “1” → “X” and the pin status change from “1” input to “0” output are counted as signal changes in the “0” direction.
- The output changes “0” → “1”, “X” → “1”, “0” → “X” and the pin status change from “0” input to “1” output are counted as signal changes in the “1” direction.

Table 4-12. SSO Limitation Time Range (TYP.)

Buffer Type	Load Capacitance C_L [pF]		
	$0 \leq C_L \leq 50$	$50 < C_L \leq 200$	$200 < C_L \leq 300$
3.0 mA	≤ 2.5 ns	≤ 4.0 ns	≤ 6.0 ns
6.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
9.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
12.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
18.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns
24.0 mA	≤ 3.0 ns	≤ 4.0 ns	≤ 6.0 ns

4.6.4 Method for Judging SSO limits

In judging SSO, pin placement must be considered. A simplified judgement method and a judgement method when driving potential and load capacitance differ are explained below.

(1) Judgement method

Judging SSO is performed based on the output buffer type, output load capacitance, and the number of valid GND pins. The number of pins that can be operated simultaneously between 3 consecutive effective GND pins is shown in Table 4-13.

This number indicates the limited number of pins that can be operated simultaneously when 12 mA, 3V output buffers are used. If buffers with different drive performances and output levels are used, calculate the limited number of pins by using the conversion coefficients listed in Table 4-14.

Table 4-13. Limited Number of SSO Pins between 3 GND Pins (3.3-V Output Buffer, I_{OL} = 12 mA)

No. of Valid GND pins	Output Load Capacitance CL			
	≤ 50 pF	≤ 100 pF	≤ 150 pF	≤ 200 pF
3	19.8	18.0	17.4	16.0

Table 4-14. SSO Pin Conversion Coefficients

Output Level	Buffer Type	I_{OL} (mA)	Conversion Coefficient
LVTTL buffer	Normal	3.0	0.34
		6.0	0.63
		9.0	0.86
		12.0	1.00
		18.0	1.30
		24.0	1.48
	Low noise	6.0	0.22
		9.0	0.28
		12.0	0.32
		18.0	0.36
		24.0	0.37
TTL 5-V tolerant buffer	Normal	1.0	0.24
		2.0	0.42
		3.0	0.65
		6.0	0.82
		9.0	1.11
		12.0	1.50
	Low noise	3.0	0.22
		6.0	0.28
		9.0	0.36
		12.0	0.48
		18.0	0.48
		24.0	0.50
5-V buffer	Normal	1.0	0.25
		2.0	0.45
		3.0	0.75
		6.0	0.90
		9.0	1.12
		12.0	1.50
		18.0	2.00
	Low noise	3.0	0.25
		6.0	0.31
		12.0	0.45
		18.0	0.75
5-V PCI			2.00
3-V PCI			1.30

(2) Judgement method when driving potential and load capacitance differ

In the case of buffers with a different driving potential, judgement must be made using the following equation, employing the limited number of SSO pins (M) in Table 4-13, taking into consideration the number of SSO pins for each driving potential (m_i) and the SSO pin conversion coefficient (β_i)

$$\Sigma\, m_i \times \beta_i \leq M$$

m_i: Number of SSO pins per driving potential

β_i: Number of simultaneous operation pin conversion coefficient per buffer type

Moreover, if the load capacitance also differs, use the following equation, taking into consideration the limited number of SSO pins (M_i) per load capacitance.

$$\Sigma\, m_i \times \beta_i / M_i \leq 1$$

M_i: Limited number of SSO pins

4.6.5 Cautions on pin layout

- Place input pins that are easily affected by noise (especially clock input pins) as near as possible to the GND pin.
- Place output buffers to be operated simultaneously as far apart as possible from input pins. Placing GND pins around them is most effective.
- If surrounding output buffers to be operated simultaneously with GND pins is difficult, place the output buffers as dispersed as possible, and also keep them as far apart as possible from input pins.
- If adding GND/V_{DD} pins, add two GND pins for one V_{DD} pin.

4.6.6 Handling when SSO limit is exceeded

<1> Adding V_{DD} and GND pins

Add V_{DD} and GND pins to fulfill the required number of SSO pins.
Be sure to make the ratio of the added V_{DD} pin to the added GND pin one to two.

<2> Changing buffer type

The peak value of the output charge/discharge current depends on the buffer type and driving potential. Changing the low driving output buffer or the Low Noise type should be considered.

<3> Lowering the output load capacitance

The amplitude of the noise generated by the charge/discharge current that flows during output transitions depends on the load capacitance of the output pin. Therefore, the noise generation can be reduced by lowering the output load capacitance, thus increasing the limited number of SSO pins.

<4> Reducing the number of simultaneous operation pins by changing the timing

The number of SSO output pins can be reduced by delay the timing to the SSO output pins to shift the timing in relation to that of other SSO output pins.

5.1 Circuit Design for Testing

A test circuit design method that uses test buses (similar to the method for CB-8 Family) has been introduced for use when performing separate tests for cores in devices where cores have been implemented. However, the test specifications differ from the CB-8 Family's test specifications in the following ways.

(1) The interface block does not include any test signal input pins (TIN) or output pins (TOUT). Consequently, the customer must design the circuit which switches the signals (normal signals and test signals) that are input to and output from external pins when performing separate tests for cores.

(2) CB-9 Family VX/VM type devices do not include the TMC1 and TMC2 input pins that are for test mode settings, such as are found in CB-8 Family devices. This is because the connection for setting the interface block's I_{DD} test mode and LFT test mode is made automatically when the input buffers (FM11 and FM21) for test mode settings are used.

LFT test mode: This mode is used to minimize the output current for target devices that are simultaneously ON during product shipment testing.

I_{DD} test mode: Test mode in which pull-up/pull down resistors are disconnected to permit accurate measurement of static consumption current during product shipment testing.

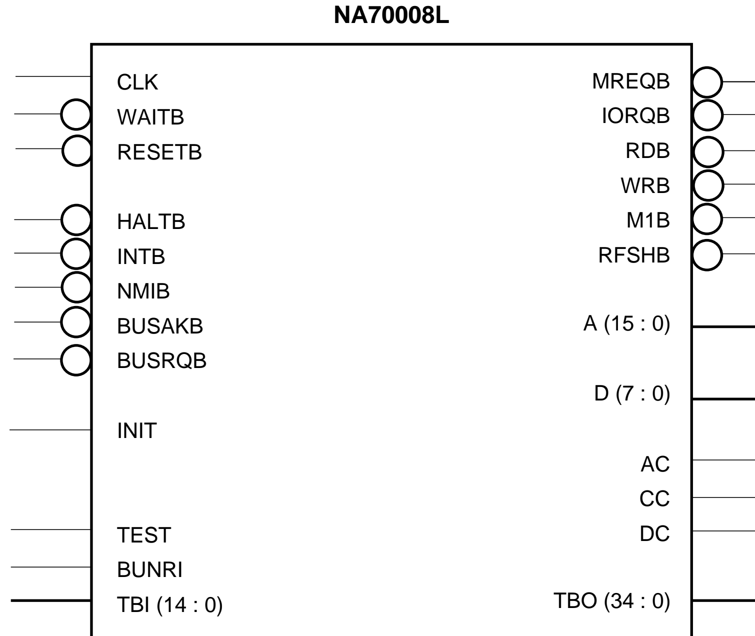
5.1.1 Circuit for core separate tests

A test circuit design method that uses test buses has been introduced to facilitate the design of the circuit used for separate testing of cores. This test circuit design method is described in detail below.

Note, however, that some cores include an exceptional test circuit. For details, see the CB-9 Family VX/VM Type Manuals.

(1) Cores

As shown in the figure below, the released cores (with a few exceptions) include five types of pins.



- Normal pins: Pins such as CLK and RESET that are used for normal operations
- BUNRI: Mode selection pin, used to select between normal mode and test mode
- TEST: Control pin that is used with the BUNRI pin to control the test buses
- TBI×××: Input test bus pin
- TBO××: Output test bus pin

In cores, the normal pins are valid when the BUNRI pin is at low level. When the BUNRI pin is at high level, the input pins among the normal pins are not valid, the output pins are undefined, the bidirectional pins are set to input mode, and the mode switches from normal mode to test mode.

If the TEST pin is at low level while in test mode (BUNRI pin is at high level), the test input pin (TBI××) is not valid and the test output pin (TBO××) has fixed high impedance. If the TEST pin is at high level, both the test input pin (TBI××) and the test output pin (TBO××) are valid.

The above information is summarized in the following table.

Mode Switch		Normal Pins				Test Bus Pins		Mode	
BUNRI	TEST	Input	Output	Three-State Output	Bidirectional	Input	Output		
0	X	Valid	Valid	Valid	Valid	Ignored Note	Hi-Z	Normal mode	
1	0	Ignored Note	X	Hi-Z	Input Note	Ignored Note	Hi-Z	Test mode	Standby
	1	Ignored Note	X	Hi-Z	Input Note	Valid	Valid		Test

Note High-impedance input enabled

Remarks 1. Do not apply high-impedance input to input pins in functional cells and cores unless they are the input pins for which high-impedance input is allowed, as specified in Block Library and **CB-9 Family VX/VM Type CPU, Peripheral Design Manual (A14304E)**.

2. Hi-Z: High-impedance

(2) Interface blocks for mode setting

Two mode-setting interface blocks, FM11 and FM21, are used to control the three modes listed in the following table.

FM11	FM21	Mode	Target Simulation
0	0	Normal mode (actual operation mode)	Used by user
0	1	LFT (I_{OL}, I_{OH} MIN.) test mode Note 1	Used by NEC (user use prohibited)
1	0	I_{DD} test mode Note 2	Used by NEC (user use prohibited)
1	1	Prohibited	Prohibited

Notes 1. LFT test mode: This mode is used to minimize the output current for target devices that are simultaneously ON during product shipment testing.

2. I_{DD} test mode: Test mode in which pull-up/pull-down resistors are disconnected to permit accurate measurement of the static current consumption during product shipment testing.

(3) Circuit design for core separate test

Next, specific examples are provided as part of the description of the test circuit design method when cores have been implemented. The following type of chip design is used as an example.

Example: Circuit configuration

- Cores: NA70008L (1 unit)
  NA71055L (1 unit)
- User logic (1 unit)

Modes to be considered

<1> Normal mode
<2> Separate test mode for NA70008L
<3> Separate test mode for NA71055L
<4> Separate test mode for user logic

(a) Estimation of test mode selection pins

The following is an example of test mode selection pin count estimations that is based on the circuit example described above.

(i) When minimizing the number of dedicated pins used as test mode selection pins

Input pin used as LFT test mode selection pin:	1 pin (dedicated)
Input pin used as I_{DD} test mode selection pin:	1 pin (dedicated)
Input pin used as normal mode/test mode selection pin:	1 pin (dedicated)
Input pin used as other required test mode selection pins:	M pins (shared)
	3 pins + M pins

From the above example:

Normal mode 1 type

Test mode 3 types → implemented as "M"

M = $\log_2$ (number of test modes) Note = rounding ($\log_2 3$) = 2

Note Numbers in decimal places are rounded off.

In this case, three dedicated test mode selection pins and two shared test mode selection pins are required. The shared pins can be shared as function pins when in normal mode, but they cannot be shared as test bus pins (pins used for separate tests of macros).

(ii) When minimizing the total number of test mode selection pins

Input pin used as LFT test mode selection pin:	1 pin (dedicated)
Input pin used as I_{DD} test mode selection pin:	1 pin (dedicated)
Input pins used as mode selection pin:	N pins (dedicated)
	2 pins + N pins

From the above example:

Mode selections to be considered 4 types → implemented as "N"

N = $\log_2$ (number of mode selections to be considered) Note = rounding ($\log_2 4$) = 2

Note Numbers in decimal places are rounded off.

In this case, four dedicated test mode selection pins are required.

(b) Count of required test bus pins (can be shared as pins used by user)

First, check the number of test bus pins (divided into TBI×× and TBO×× types) to be actually used for each core.

Core	TBIxx	TBOxx
NA70008L	15	35
NA71055L	38 (MAX.)	42 (MAX.)

Next, use the above table to determine the maximum numbers of input test bus pins and output test bus pins.

In this case, since these numbers are 38 for TBI×× (MAX.) and 42 for TBO×× (MAX.), the total number of required test bus pins is 80.

(c) Allocation of interface block

Enter the interface block according to the number of required test bus pins determined in (b) above. In this example, 80 test bus pins are needed as the interface block. These test bus pins can basically be shared as either input pins or output pins for normal signals.

Note, however, that using these pins as alternate function pins will slightly increase the delay time for connected buses. Therefore, avoid using critical path pins as alternate function pins.

If the number of normal signal pins that can be shared is less than the sum of the core's test input pins and output pins, new test pins must be established.

(d) Connection of test bus

The interface blocks' pins are connected to the cores' TBI×× and TBO×× pins (see Figure 5-1). However, the following circuit configuration features are required to test the cores while in test mode.

<1> The circuit configuration must enable signals to be applied directly from external input pins to all of the core test input pins (TBI××, TBE, TDI××, etc.). Do not insert any sequential circuits (such as flip-flops or latches) or signal inversions between the external input pins and the core's test input pins.

<2> The circuit configuration must also enable signals to be fetched directly from the core test output pins (TBO××, TDO××, etc.) to the external output pins. Do not insert any sequential circuits (such as flip-flops or latches) or signal inversions between the external input pins and the core's test output pins.

The characteristics of this test circuit configuration example are described below.

(i) Dedicated pins for core testing are added independently from normal signal pins.

Advantages …… In this configuration, the test circuit has the least effect on the delay time of the signal route to be actually used. The configuration is simple.

Disadvantages …… Extra pins are needed as test pins.

(ii) Normal signal input (or output) pins are used as core test input (or output) pins.

Advantages …… Since the test pins are shared as normal signal pins, there is no need for extra pins as test pins (except for TEST input).

Disadvantages …… The delay time of the signal route to be actually used is increased due to the effect of the test circuit shown below. Therefore, avoid using this configuration for a critical path.

- Delay time increased by extra fan-outs and wire length needed for core test inputs
- Delay time increased by output selector

(iii) Normal signal input (or output) pins are used as bidirectional pins and the corresponding output (or input) pins are used as test pins during core testing.

Advantages …… Since the test pins are shared as normal signal pins, there is no need for extra pins as test pins (except for TEST input). Compared to the configuration method described in (ii) above, this configuration's test circuit has less effect on the delay time of the signal route to be actually used.

Disadvantages …… The delay time of the signal route to be actually used is increased due to the effect of the test circuit shown below. Therefore, avoid using this configuration for a critical path.

- Delay time differential when input-only buffer is changed to bidirectional buffer
- Delay time differential when output-only buffer is changed to bidirectional buffer
- Delay time increased by extra fan-outs and wire length needed for branching of output signals

Actually, we recommend selecting the best combination of the above three configuration methods in view of the number of input-only and output-only pins for normal signals, the total number of pins, critical path considerations, etc.

(e) Selection of input pins for controlling TMC1 and TMC2

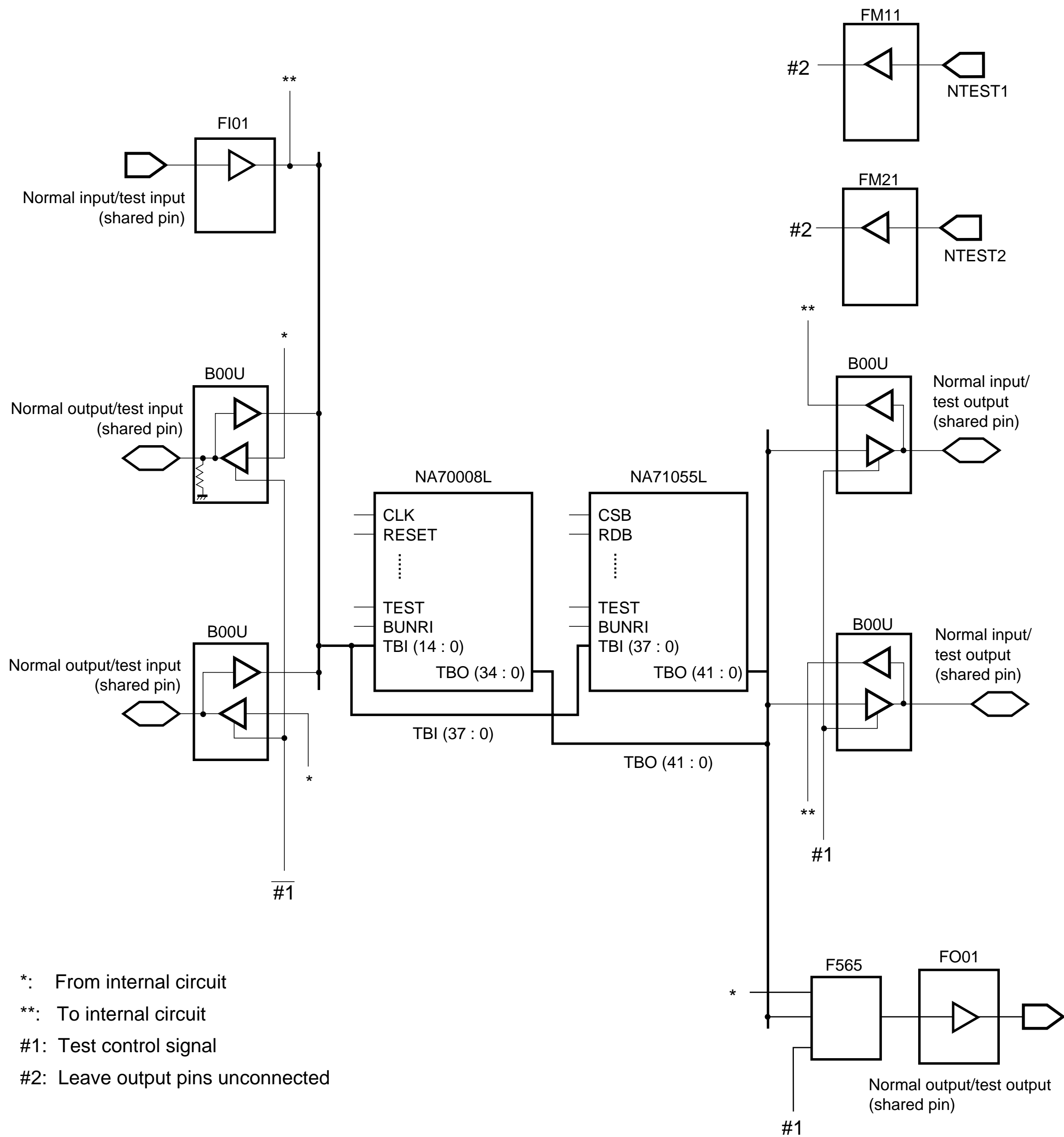
Input pins that are dedicated for controlling TMC1 and TMC2 must be externally attached to control the interface block's mode selection pins TMC1 and TMC2. TMC1 and TMC2 are controlled from an external source via these input pins.

When externally attaching these input pins for controlling TMC1 and TMC2, be sure to use the special interface block described below.

- Dedicated input buffer for controlling TMC1 pin: FM11
- Dedicated input buffer for controlling TMC2 pin: FM21

Also, leave the output pins unconnected in the netlist (circuit).

Figure 5-1. Test Bus Connection Example



(f) Creation of test bus control circuit

The creation of decoders to select modes is described below.

In the circuit shown in **Figure 5-1**, if you wish to test the NA70008L, set the control pins as shown below for the block settings.

Block	Setting	Control Pin Setting
NA70008L	Test mode Test bus: valid	BUNRI = 1 TEST = 1
NA71055L	Test mode Input test bus: ignored Output test bus: Hi-Z	BUNRI = 1 TEST = 0

When the above settings are made, signals that are input from an external pin are input via the TIN pin to the NA70008L's input test bus (TBI××) and the results that are output from the output test bus (TBO××) are output to the external pin via the TOUT pin. This enables the NA70008L to be tested.

Similarly, decoder circuits for setting test modes are also created for other test modes.

The control pin settings for these various tests are shown below.

	Interface Block		NA70008L		NA71055L	
	FM11	FM21	BUNRI	TEST	BUNRI	TEST
Normal mode	0	0	0	X	0	X
NA70008L test	0	0	1	1	1	0
NA71055L test	0	0	1	0	1	1
User logic test	0	0	1	0	1	0
	0 Note	1 Note				
LFT test Note	0	1	0	X	0	X
IDD test Note	1	0	0	X	0	X

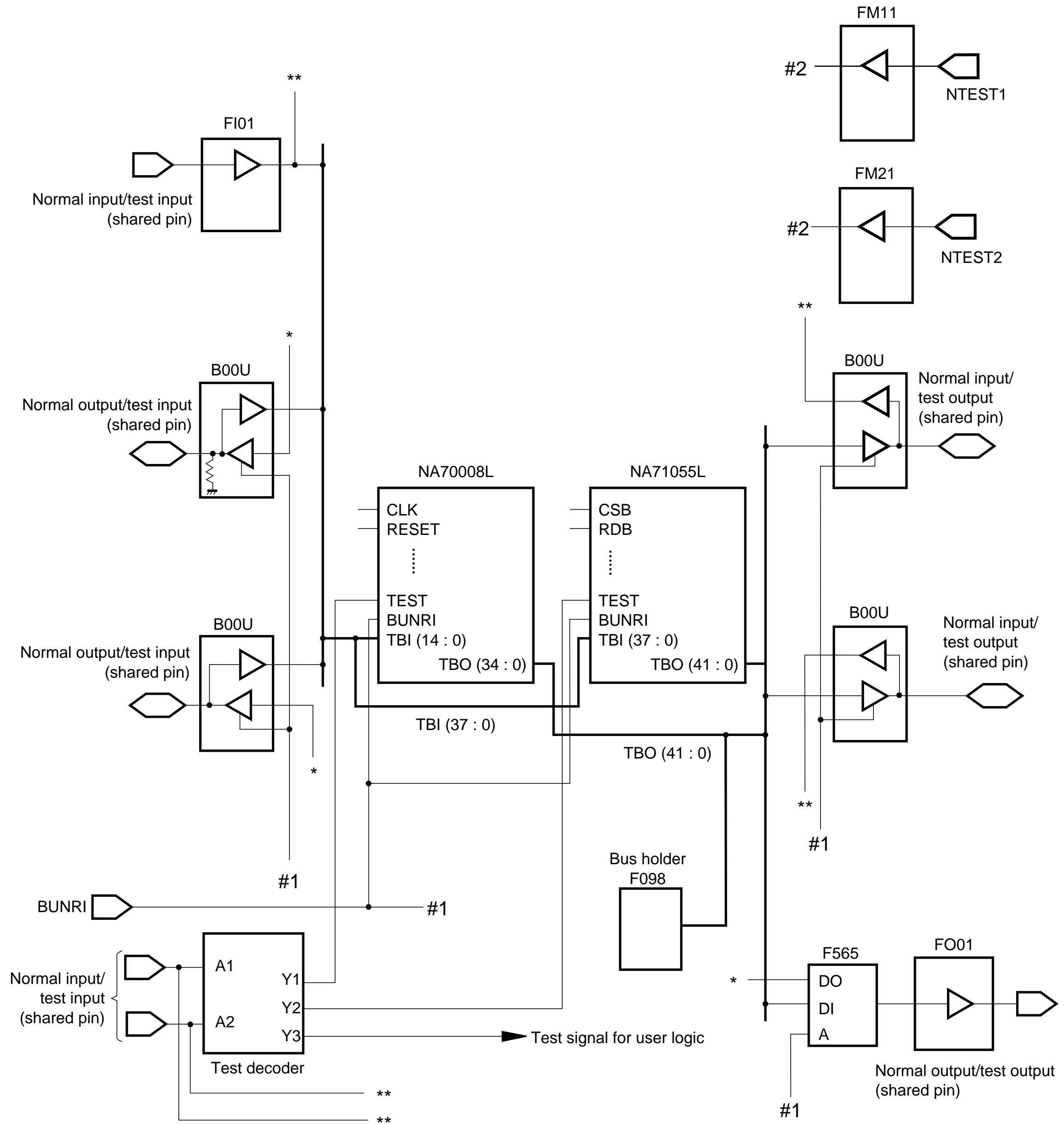
Note These are used for tests performed by the tester at NEC.

Remark For details of the user logic test, see **5.1.3 User logic circuit design for testing**.

Figure 5-2 shows test bus connection examples using the test bus control circuits described in the above table.

Figure 5-2. Test Bus Control Circuit Connection Example (1/2)

(a) When test mode selection pins are shared



*: From internal circuit

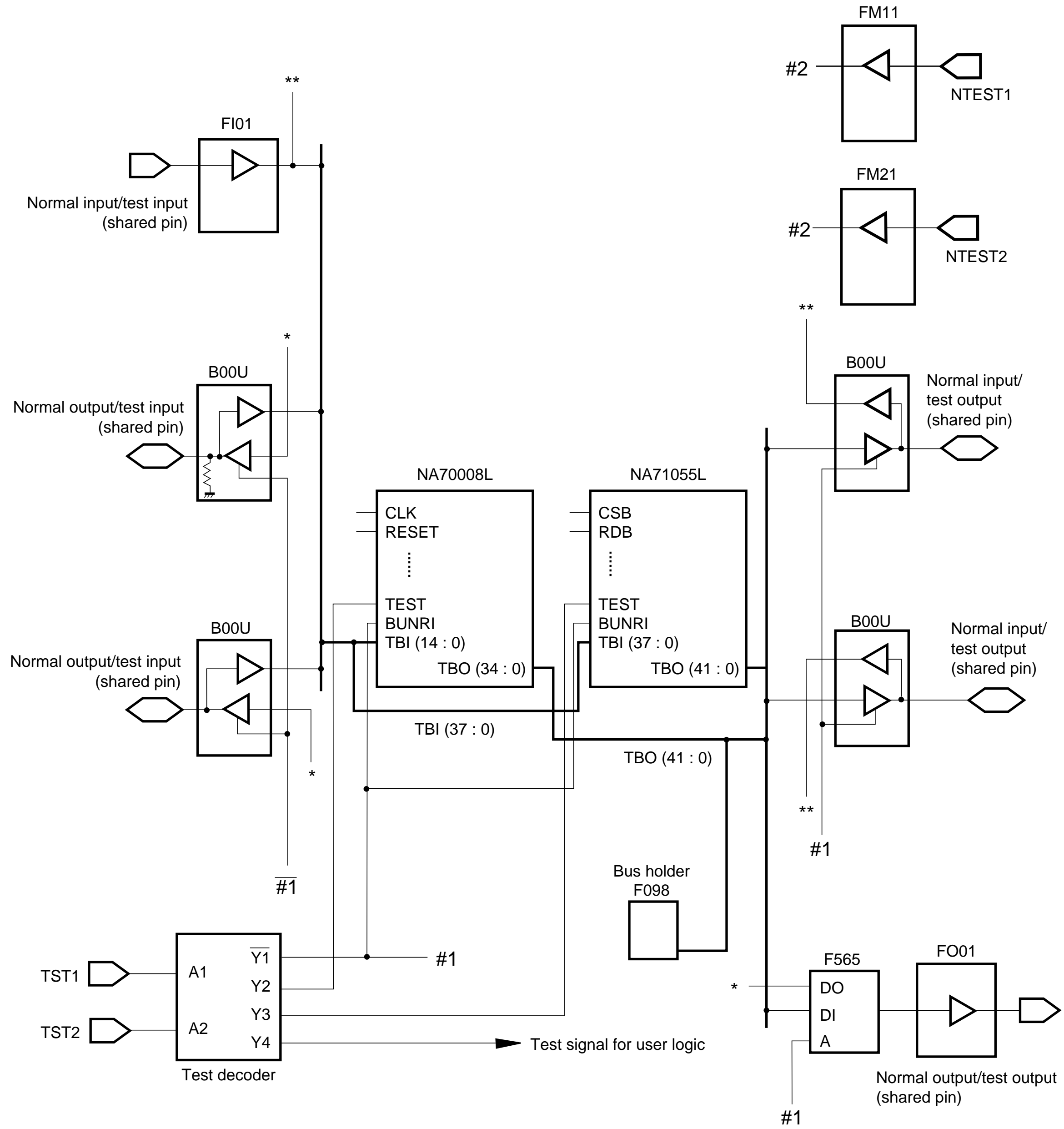
**: To internal circuit

#1: Test control signal

#2: Leave output pins unconnected

Figure 5-2. Test Bus Control Circuit Connection Example (2/2)

(b) When test mode selection pins are dedicated



*: From internal circuit

**: To internal circuit

#1: Test control signal

#2: Leave output pins unconnected

5.1.2 Core control pins

Control pins are established for cores to control the I/O direction or status of bidirectional pins and three-state output pins.

(1) Core control pin functions

There are four types of core (NA70008L) pin attributes, as shown below.

- Input pin (CLK pin, etc.)
- Output pin (HALTB pin, etc.)
- Bidirectional pin (data bus, etc.)
- Three-state output pin (sets pin output to high impedance when there is a hold request for the WRB pin, etc.)

Control output pins that indicate the pin's I/O direction status are provided for two of these pin types: bidirectional pins and three-state output pins.
The correspondences between pin statuses and control signals are shown in the following table.

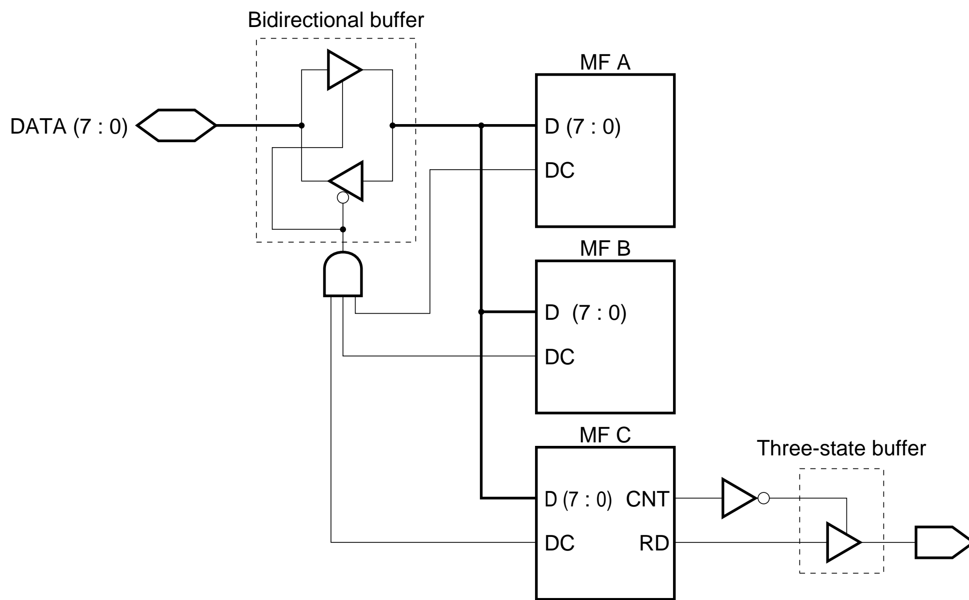
	Control Pin	Status
Bidirectional pin	H	Input mode
	L	Output mode
Three-state output pin	H	High impedance
	L	Output active

(2) Use of control pins

(a) Control of bidirectional buffer or three-state buffer

As shown in Figure 5-3, control pins are basically used for control signals sent to a bidirectional buffer or three-state buffer.

Figure 5-3. Control of Bidirectional Buffer or Three-state Buffer



Remark DC and CNT are control pins.

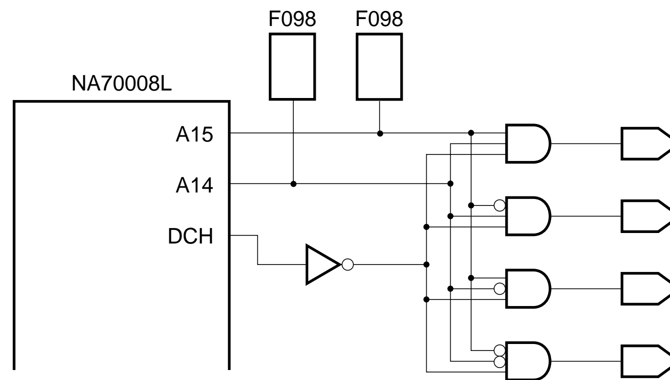
★ **(b) Countermeasures against high-impedance output**

A core's three-state pin and bidirectional pin may enter the high-impedance (hereafter, "Hi-Z") state during separate testing of the core. Therefore Hi-Z countermeasures are required, at least during testing. An example of such a countermeasure is shown in Figure 5-4.

Note with caution that if this countermeasure is inadequate for some reason, a through current will flow and may cause defects.

Also, control pins should not be used for any purpose other than as a countermeasure against high-impedance output.

★ **Figure 5-4. Example of Countermeasure against High-Impedance Output**



Remark F098: Bus holder

5.1.3 User logic circuit design for testing

The following three points need to be considered when creating a user logic circuit for testing.

- The test patterns used for the user logic test must have high testability.
- There should be as few test pins as possible.
- Test patterns should be as short as possible.

To meet the above requirements, we recommend that the test circuit be configured to enable separate tests of user logic.

There should be no problem as long as the user logic block is completely separate and the configuration enables separate simulation from external pins.

5.2 Circuit Design for Debugger

At NEC, software debuggers are not provided for particular cell-based ICs. Consequently, customers are asked to use a general-purpose emulator and standard LSIs to set up their own emulators.

The CPU cores that NEC releases on its cell-based ICs include some pins that are not found on standard CPUs. For example, in the case of the NA70008L, such pins include a bidirectional buffer control pin. Such pins are not included in general-purpose emulators. Therefore, when using these macros to design circuits, be extra careful about which pins are supported.

5.3 Circuit Design for Total Chip Simulation

See **CHAPTER 7 TOTAL CHIP SIMULATION FOR CHIP WITH CPU CORE**.

5.4 Design of Clock Lines

5.4.1 Asynchronous circuits and synchronous circuits

There are three types of circuit design methods: (1) single-phase synchronous circuit design that is normally used for circuit design using general-purpose LSIs; (2) multi-phase synchronous circuit design that is often used for CPU design; and (3) asynchronous circuit design. The characteristics of these three circuit design methods are listed below.

Table 5-1. Circuit Design Characteristics

	Advantages	Disadvantages
Asynchronous circuit design	Total circuit size is smaller. Power consumption is lower.	Operation faults occur easily due to spikes. Abnormalities occur during post delay simulation.
Single-phase synchronous circuit design	Circuit is simple. Method is suited for high-speed circuits.	Wiring skew of clock signals must be considered.
Multi-phase synchronous circuit design	Hold time of flip-flops is easy to secure (enables circuit design that is not dependent on technology).	Method is not suited for high-speed operation.

Note that, of these three methods, circuit design using asynchronous circuits is not suited for design of CB-9 Family VX/VM type devices due to the occurrence of operation faults caused by wiring skew. Instead, we recommend either the multi-phase synchronous circuit design method or the single-phase circuit design method using clock tree synthesis.

(1) Asynchronous circuit design

Asynchronous circuit design is a design method that uses control signals such as clock and reset signals for circuit control and also uses combination circuits. Since there are fewer control signals than there are data signals, using control signals enables a smaller total chip size. It also makes the circuits more visible and enables a reduction in the circuits' power consumption.

However, when combination circuits (basically, circuits such as decoders, selectors, etc.) are used to control the control signals, there is a very high risk of spike noise which can easily affect the wiring delay.

When processes (such as those for CB-9 Family VX/VM type) device are easily affected by wiring delay, simulation results from before and after the wiring layout may differ, which can lead to abnormalities. Therefore, asynchronous circuits should basically be avoided in cell-based circuit design.

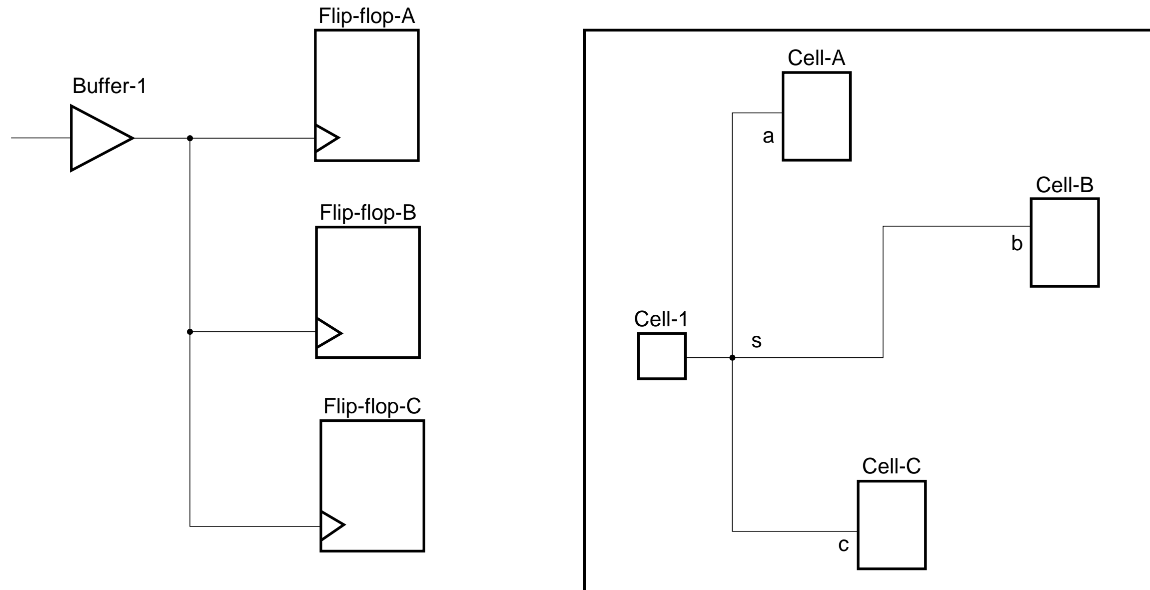
However, asynchronous circuits can be created when the circuits are certain to operate regardless of delays related to wire length.

Even when the circuit specifications require asynchronous circuits, their operation can still be guaranteed by specifying critical paths. Note with caution that only up to six critical paths can be specified.

(2) Single-phase synchronous circuit design

Single-phase synchronous circuit design is a method whereby sequential circuits are operated using only one type of clock signal. This design method makes for a comparatively simple circuit configuration, but timing adjustments such as for clock skew between sequential circuits are required.

Figure 5-5. Clock Skew

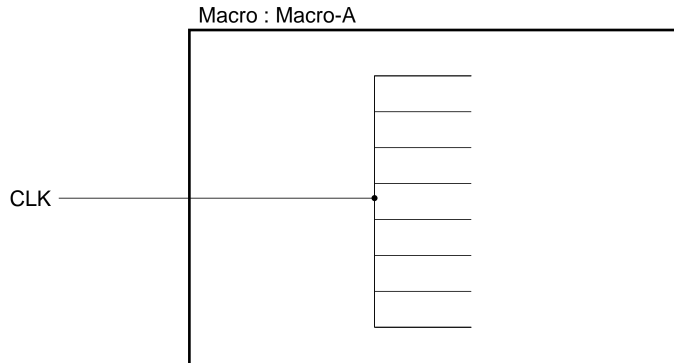


“Clock skew” refers to the skewing of clock signals between sequential circuits.
Skewing of these signals increases as the wiring resistance increases. It also depends on the wire length after a branch point. Such clock skew must be considered when performing single-phase circuit design and can be handled via the following methods.

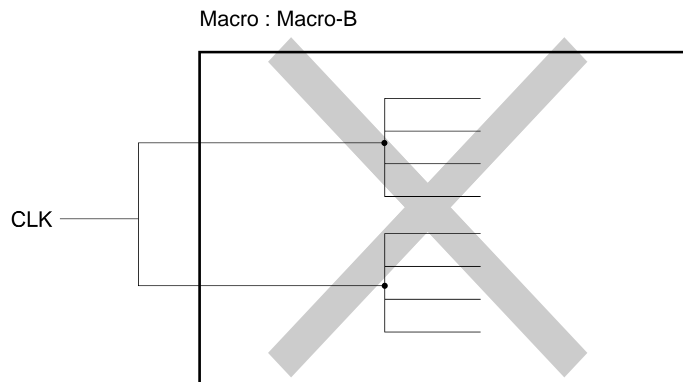
(A) Lay out the same clock lines within the same macro (see Figure 5-6).
(B) When laying out several clock lines, lay out so as to prevent clock skew between clock lines.
(C) Within the configuration of synchronous counters and shift registers, set faster operation at the later registers.
(D) Use clock tree synthesis (see **5.4.4 Clock tree synthesis**).

Figure 5-6. Clock Layout

(a) Example of correct layout



(b) Example of incorrect layout



(3) Synchronous circuit design using multi-phase clocks

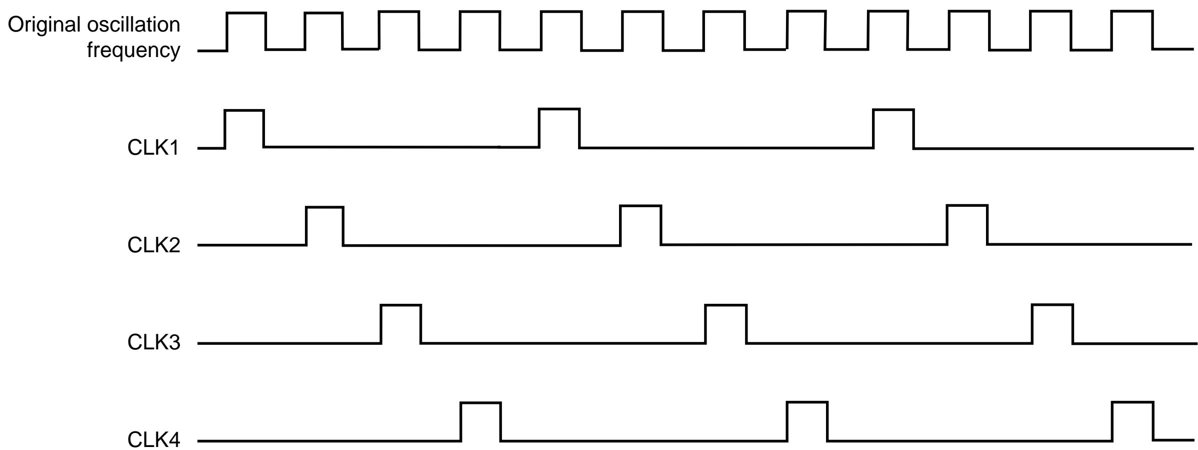
When there are no processing speed-related problems, we recommend a synchronous circuit design using multi-phase clocks. However, when implementing a function, there are many more difficulties to overcome when using multi-phase synchronous circuits than when using asynchronous circuits, so design using synchronous circuits is not very common.

The following is an introduction to a general method that is widely used among LSI manufacturers when designing synchronous circuits using multi-phase clocks.

Figure 5-7 shows an example of a multi-phase clock (in this example, it is a four-phase clock). Multi-phase clocks are the most commonly used method even when designing general-purpose LSIs (CPUs, etc.).

For example, if a particular CPU has three clocks per state, then that CPU uses a three-phase clock.

Figure 5-7. Example of Multi-phase Clock



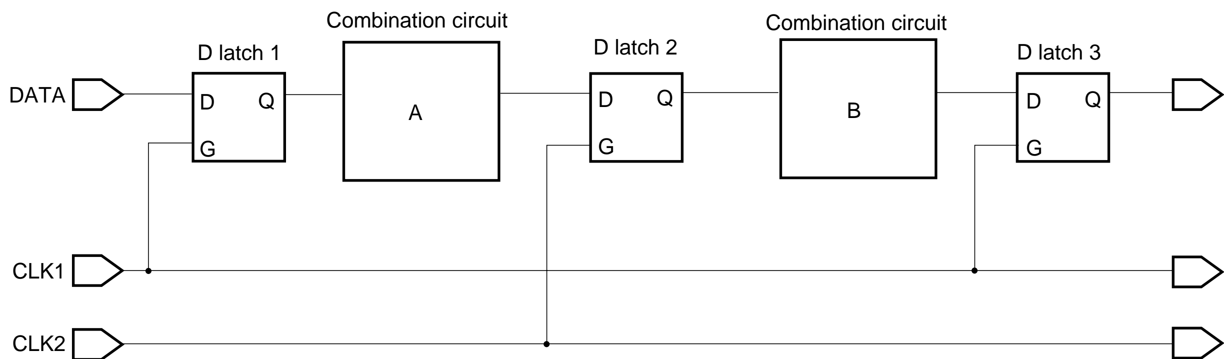
Note the following points to increase effectiveness when using multi-phase clocks.

(a) It becomes easier to secure the setup/hold times for latches and flip-flops.

Using CLK1 and CLK2 alternately as shown below makes it easier to secure the setup/hold times for latches.

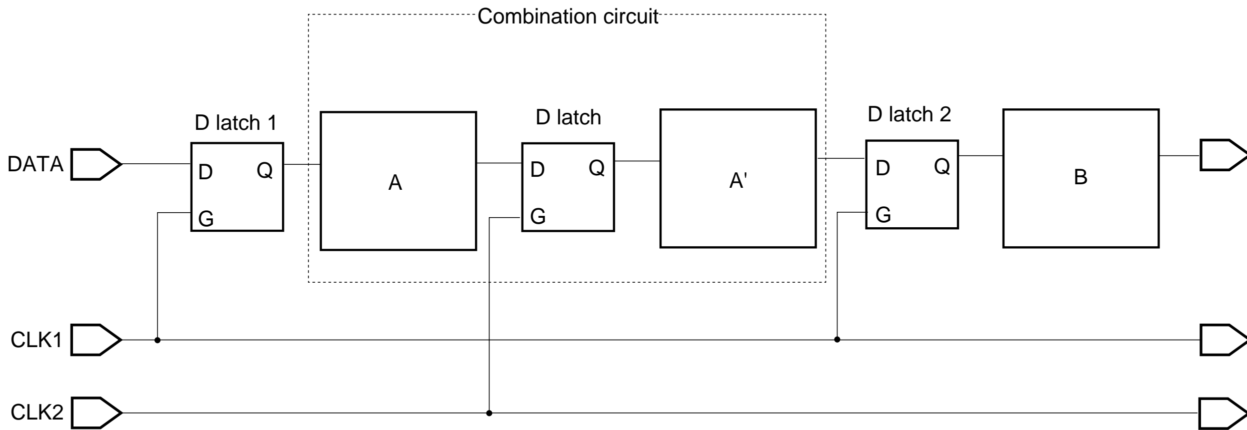
For example, in the circuit shown in Figure 5-8, the setup time for latch 2 is (cycle period of original oscillation frequency – delay time of combination circuit A).

Figure 5-8. Setup/Hold Times for Latches



If the delay time of combination circuit A is too long to secure the setup time for latch 2, combination circuit A can be split in two, as shown in Figure 5-9, and an additional latch can be inserted between the two parts (A and A’) to secure the setup time for latch 2. The same is true for hold times.

Figure 5-9. Division of Combination Circuit



(b) When creating a complicated synchronous circuit, simplify the circuit by assigning a role to each clock.

This results in having fewer gates than when a single-phase clock is used. For example, when data is sent from ROM via serial input, the circuit can be designed to sequentially add accumulated data. Figure 5-10 shows a simple synchronous circuit design that uses a three-phase clock.

Figure 5-10. Addition Circuit (Using Three-Phase Clock)

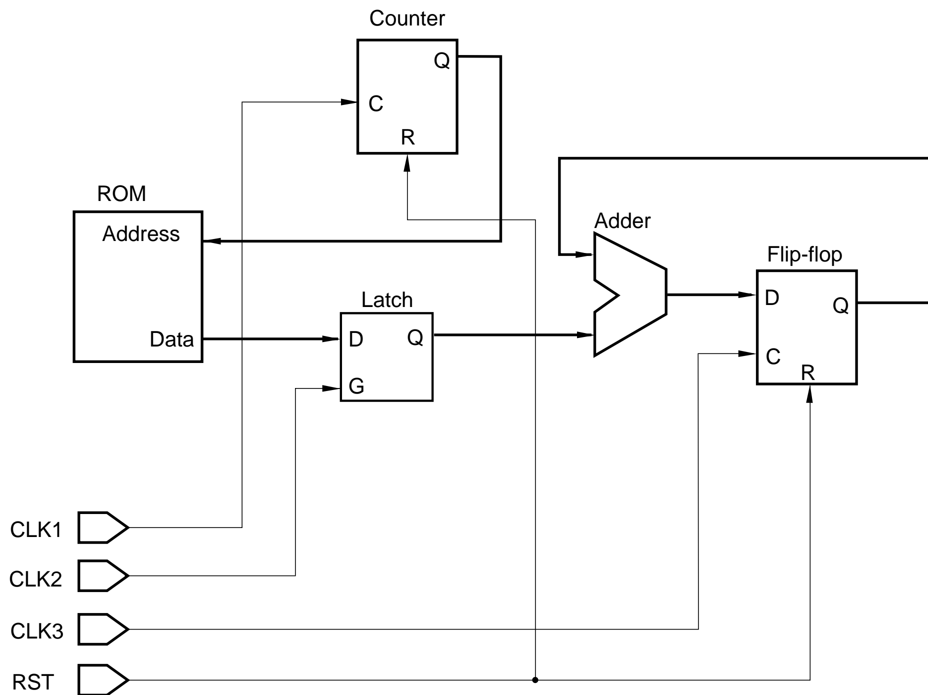
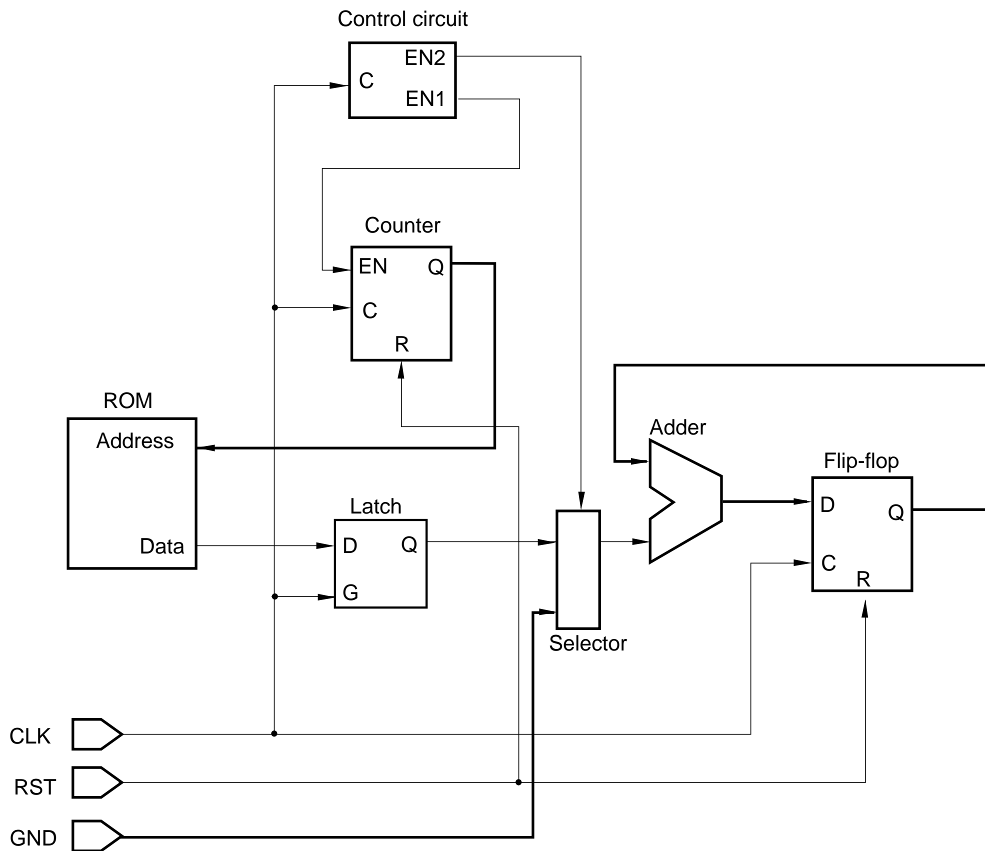


Figure 5-11 shows a synchronous circuit design that uses a single-phase clock, which is more complicated than the circuit shown in Figure 5-10 and tends to have a greater number of gates.

Figure 5-11. Addition Circuit (Using Single-Phase Clock)

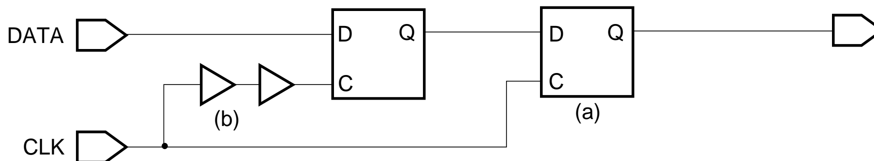


(c) This method enables process-independent (technology-independent) designs.

When designing a synchronous circuit that uses a multi-phase clock, basically the only impact the process has on the circuit is in relation to the maximum clock frequency. Since the design does not use any delay gates to secure the flip-flop hold time, it can be designed without reference to the process.

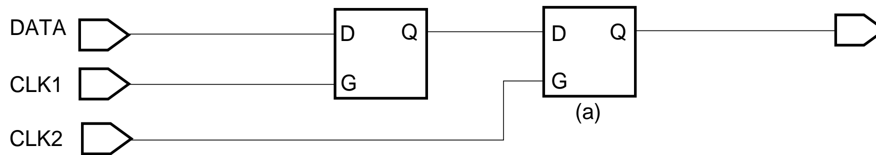
Figure 5-12 shows a circuit that is commonly seen in diagrams of the 74LS circuit, which is designed using a single-phase clock. In this case, the hold time for flip-flop (a) is secured by delay gate (b). If the process changes, the delay value of delay gate (b) also changes, which means that it may no longer secure the flip-flop's hold time.

Figure 5-12. Common Circuit in 74LS Circuit Diagram



In the multi-phase clock circuit shown in Figure 5-13, the hold time for flip-flop (a) is secured as (rising edge of CLK2 – rising edge of CLK1) and is not process-dependent.

Figure 5-13. Circuit Using Two-phase Clock



Caution concerning use of multi-phase clock

Although the circuit design becomes simpler as the number of phases is increased, adding phases also slows down processing speed. Therefore, the desired function should be implemented using as few clock phases as possible.

5.4.2 Clock skew

Clock skew is generated by factors such as variation in actual wiring length. Such clock skew can lead to hold time errors in sequential circuits. Normally, during the simulation that is performed prior to placement and routing stage it is not possible to anticipate variations caused by such abnormalities. Therefore, the design must take clock skew into consideration.

(1) Design using a clock line within a macro

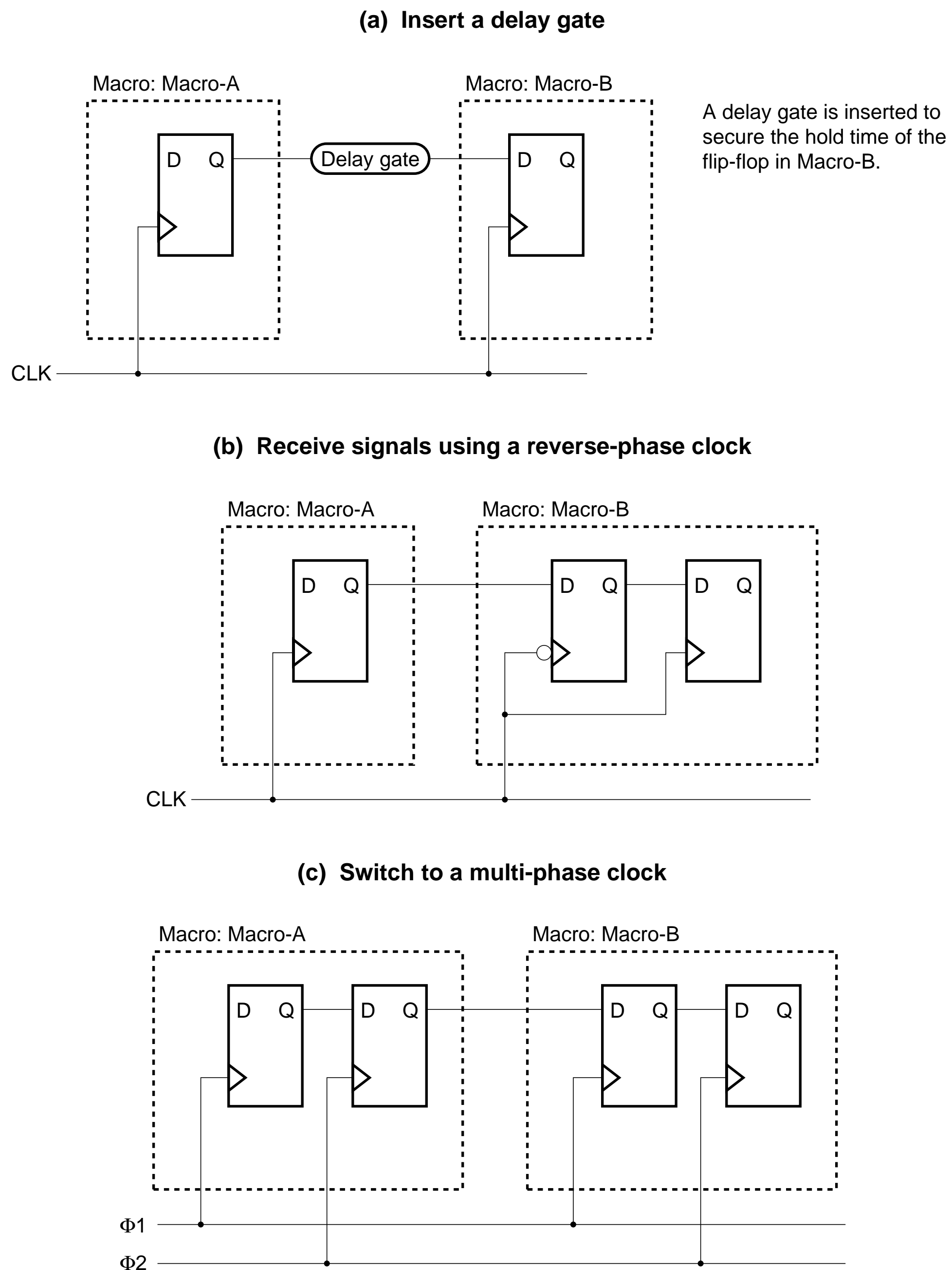
In a single-phase synchronous circuit design, clock signals are supplied via a single clock line.

In a multi-phase synchronous circuit design, it is basically not necessary to consider clock skew. However, the operating frequency should be considered.

(2) Design using clock lines between macros

In a single-phase synchronous circuit design, clock skew is a problem, especially clock skew between macros. Countermeasures against this problem are shown below.

Figure 5-14. Countermeasures for Clock Lines between Macros



The reverse phase of the clock is used in part (b) of Figure 5-14 to establish a margin for the hold time. When using this method, caution is required concerning the clock frequency and duty.

Part (c) of Figure 5-14 shows a countermeasure that uses a multi-phase clock. In this case, caution is also required concerning the clock frequency. Be sure to include a clock driver in the clock line's design.

5.4.3 Enable control

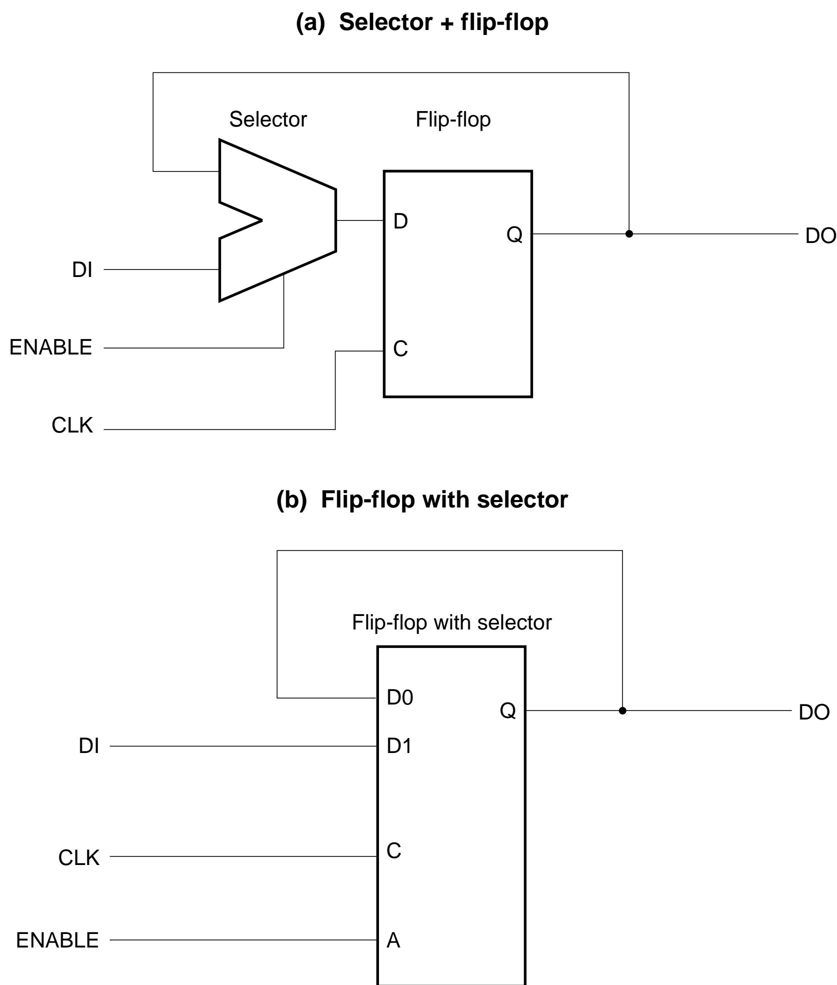
Circuits are designed to generate enable signals which disable operation of flip-flops in the system as a means of stopping operation of the system. There are two types of enable signals: data enable signals and clock enable signals.

(1) Data enable

The circuit is designed so that output signals are fed back to prevent signal changes. Use the opposite edge of the flip-flop to change the enable signal. This is the most common method and it is suitable for synchronous circuit designs.

Figure 5-15. Data Enable Flip-flop

(a) Selector + flip-flop



(b) Flip-flop with selector

(2) Clock enable

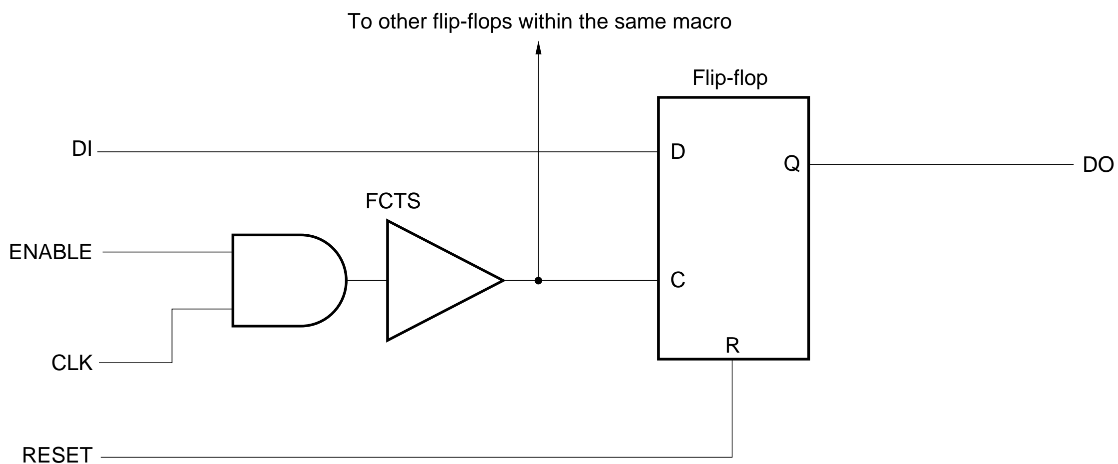
When using a data enable flip-flop, the clock signal continues to be supplied to the flip-flop even when the flip-flop has stopped. Consequently, in systems that have a sleep mode (a state in which the clock signal to the circuit is stopped to reduce power consumption) power consumption may become a problem. A clock enable flip-flop can be used as a countermeasure for such problems.

Specifically, inserting a logic gate (such as an AND gate) before the clock input, as shown in Figure 5-16, keeps the clock signal from being supplied to the flip-flop.

However, this method is also problematic in that the inserted logic gate may generate spike noise that is input to the clock and may cause operation faults. However, this type of operation fault can be prevented by initializing the flip-flop when recovering from sleep mode.

We recommend using data enable flip-flops when designing ordinary systems.

Figure 5-16. Configuration Example Using Clock Enable



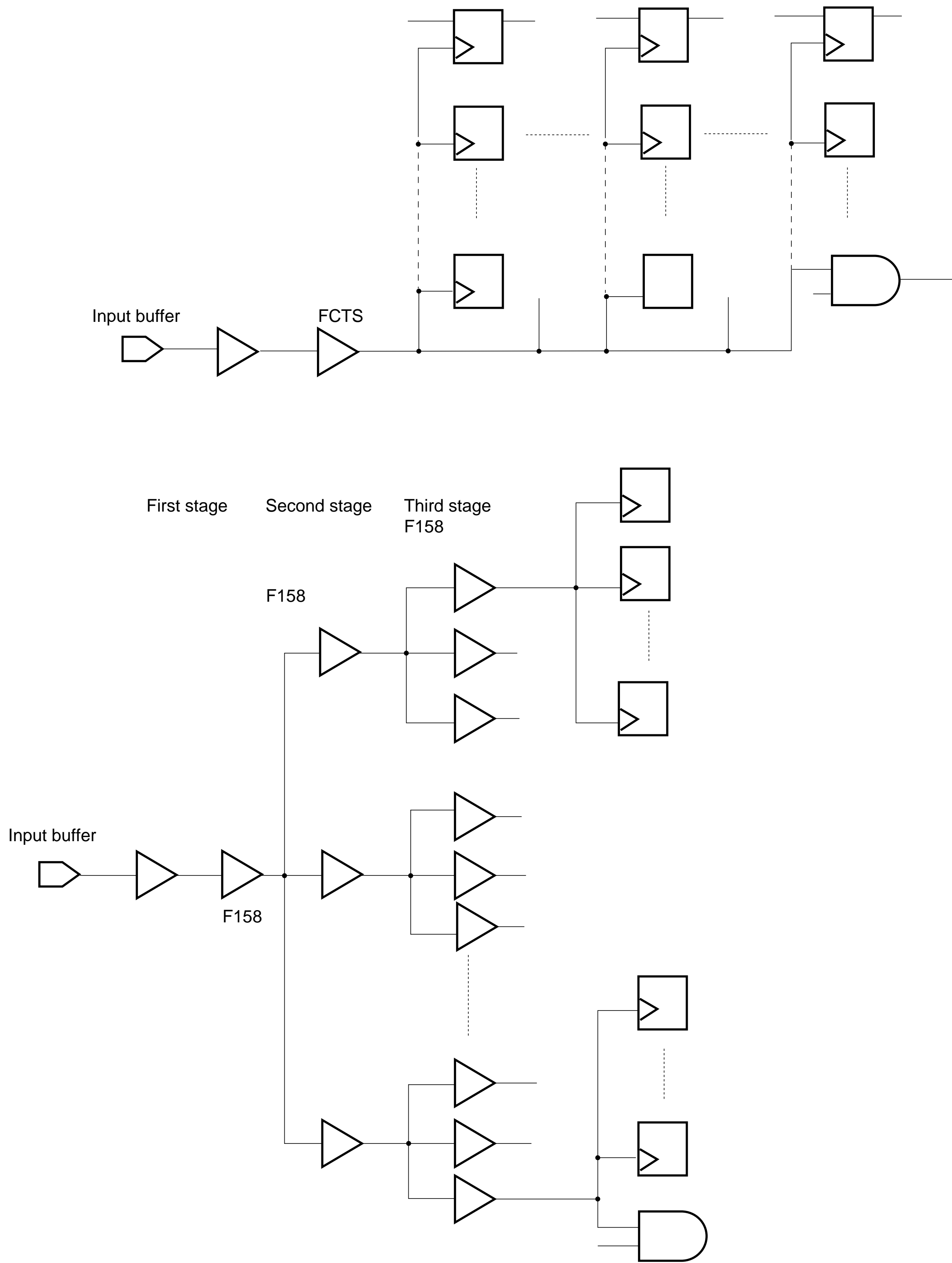
5.4.4 Clock tree synthesis

Clock tree synthesis refers to a program which uses a tree-like structure of high-drive buffers that are inserted along clock lines during chip layout to suppress skew corresponding to clock input to various blocks. In the circuit diagram, a virtual function block (“FCTS”) having an infinite number of fan-outs is used, and the clock tree (high-drive buffer tree) is synthesized during the layout for the output net.

Although the recommended number of FCTS blocks is one per chip, if more than one per chip is needed, up to 15 FCTS blocks per chip can be used. Note, however, that adding more FCTS blocks means that a corresponding amount of additional time will be need to be scheduled for clock tree synthesis and placement and wiring.

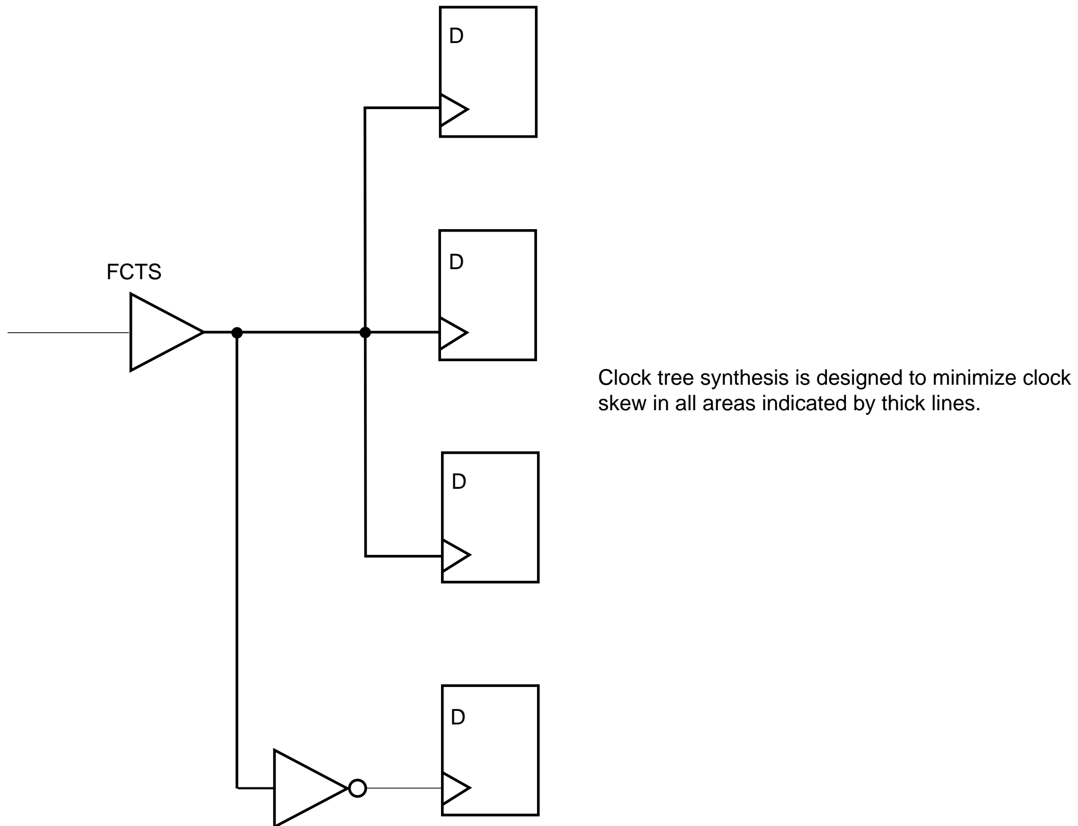
Figure 5-17 shows a layout image used for clock tree synthesis.

Figure 5-17. Layout Image for Clock Tree Synthesis



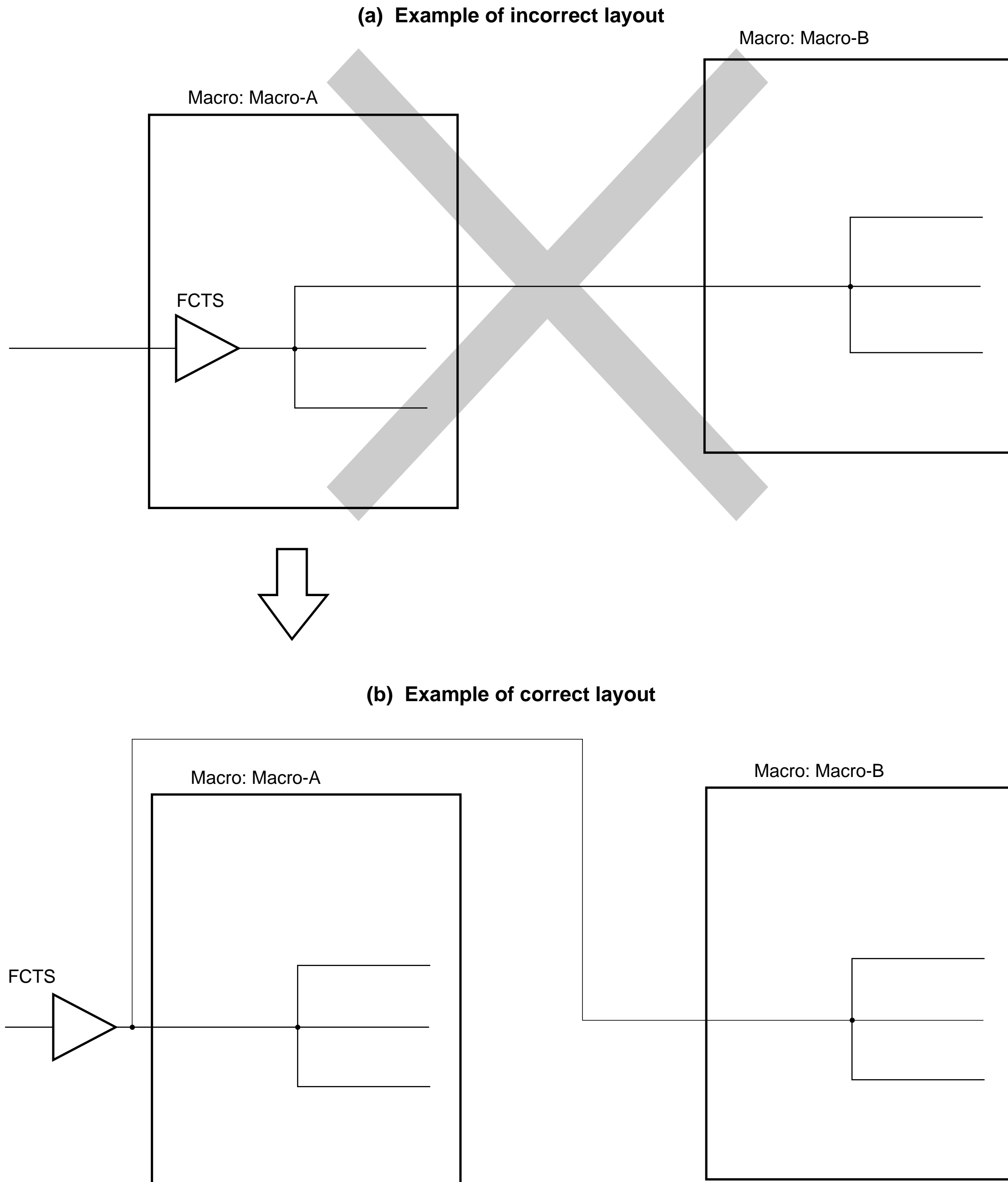
(a) As shown below, one net includes everything from the output of the clock tree synthesis block (hereafter called an "FCTS block") to the number of blocks needed to minimize clock skew. If a function block is inserted on a bus, clock skew will be suppressed as far as the inserted function block.

Figure 5-18. Clock Tree Synthesis



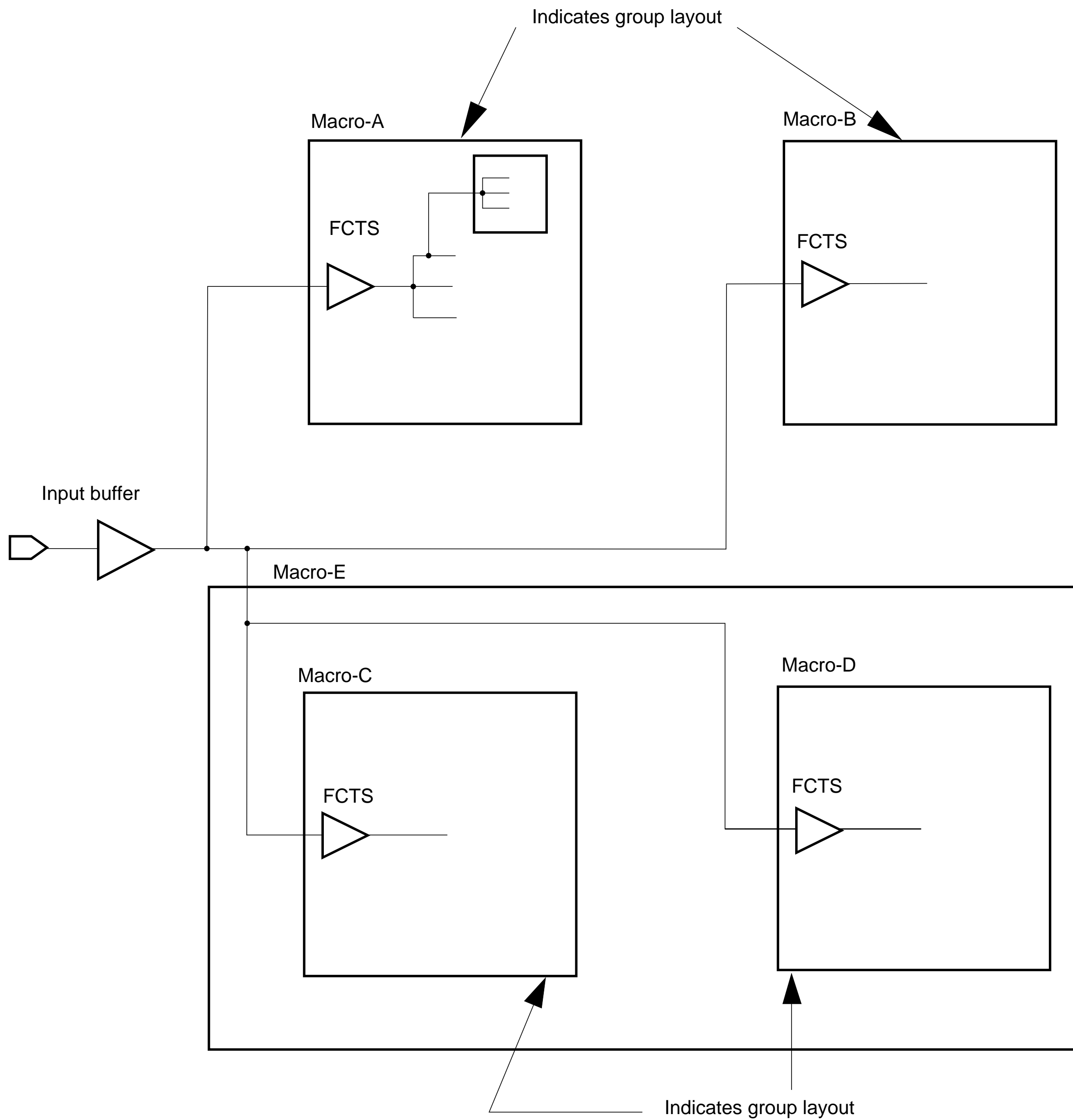
(b) When using one FCTS block to control an entire circuit, the FCTS should be laid out at the uppermost level being used and should not be within a macro.

Figure 5-19. FCTS Layout Restriction



(c) When using an FCTS block for each macro, the delay values vary depending on the macro sizes and loads (i.e., the number of connected blocks), so clock skew suppression cannot be guaranteed between FCTS blocks.
However, if the design takes into consideration the timing of signals transferred between macros, skew within macros can be reduced. When presenting the interface to NEC, be sure to group together the macros that use FCTS blocks. Also, the total number of FCTS blocks used should not exceed 15.

Figure 5-20. FCTS Layout Diagram



(1) Clock skew values and reference delay values when using clock tree synthesis.

In CB-9 Family VX/VM type devices, clock skew can be determined according to the step size, as shown below.

Table 5-2. FCTS Clock Skew (V_{DD} = 3.3 V, T_A = –40 to +85°C)

No. of Blocks Connected to FCTS Output	To D01	To E54	To G08	To H87	To K92
to 1279	±110 ps	±115 ps	±135 ps	±160 ps	±255 ps
1280 to 2559	±115 ps	±125 ps	±145 ps	±170 ps	±275 ps
2560 to 5119	±135 ps	±150 ps	±165 ps	±180 ps	±305 ps
5120 to 10239	±155 ps	±175 ps	±185 ps	±195 ps	±310 ps
10240 to 20479		±190 ps	±210 ps	±225 ps	±355 ps
20480 to 40959			±220 ps	±235 ps	±380 ps

Table 5-3. FCTS Clock Skew (V_{DD} = 2.0 V, T_A = –40 to +85°C)

No. of Blocks Connected to FCTS Output	To D01	To E54	To G08	To H87	To K92
to 1279	±190 ps	±200 ps	±245 ps	±285 ps	±455 ps
1280 to 2559	±205 ps	±220 ps	±260 ps	±300 ps	±490 ps
2560 to 5119	±240 ps	±265 ps	±295 ps	±325 ps	±545 ps
5120 to 10239	±275 ps	±310 ps	±325 ps	±350 ps	±550 ps
10240 to 20479		±340 ps	±370 ps	±395 ps	±625 ps
20480 to 40959			±395 ps	±420 ps	±680 ps

The above values are values that were synthesized via clock tree synthesis for a rectangular area. There is a possibility that the above values cannot be met in cases where the layout area is not an ideal shape due to distortion of the layout area, the prioritization of macros being laid out, etc.

As for the absolute delay time of part of the clock tree, this value can be guaranteed by checking (via simulation) the actual wiring length. The following reference values should be used as a yardstick for the design.

Table 5-4. FCTS Clock Tree Block Predicted Delay Time Reference Values (V_{DD} = 3.3 V: TYP.)

No. of Blocks Connected to FCTS Output	To D01	To E54	To G08	To H87	To K92
to 1279	2.19 ns	2.35 ns	2.56 ns	2.79 ns	3.36 ns
1280 to 2559	2.23 ns	2.40 ns	2.61 ns	2.85 ns	3.43 ns
2560 to 5119	2.30 ns	2.48 ns	2.70 ns	2.96 ns	3.58 ns
5120 to 10239	2.44 ns	2.65 ns	2.90 ns	3.19 ns	3.88 ns
10240 to 20479		2.80 ns	3.06 ns	3.36 ns	4.08 ns
20480 to 40959			3.32 ns	3.65 ns	4.41 ns

Table 5-5. FCTS Clock Tree Block Predicted Delay Time Reference Values (V_{DD} = 2.0 V: TYP.)

No. of Blocks Connected to FCTS Output	To D01	To E54	To G08	To H87	To K92
to 1279	3.95 ns	4.24 ns	4.61 ns	5.05 ns	6.09 ns
1280 to 2559	4.02 ns	4.32 ns	4.70 ns	5.15 ns	6.22 ns
2560 to 5119	4.15 ns	4.47 ns	4.88 ns	5.36 ns	6.50 ns
5120 to 10239	4.40 ns	4.78 ns	5.24 ns	5.78 ns	7.05 ns
10240 to 20479		5.05 ns	5.53 ns	6.10 ns	7.42 ns
20480 to 40959			6.02 ns	6.63 ns	8.02 ns

Although these are not guaranteed values, the range of variation tends to be within the following minimum and maximum values.
From “MIN. value = TYP. value × 0.6” to “MAX. value = TYP. value × 1.8”

Caution When simulating the assumed wiring length, the simulation uses the values shown in Tables 5-6 and 5-7, not the values shown in Tables 5-2 to 5-5.

Table 5-6. FCTS Specifications (V_{DD} = 3.3 V)

Path	Intrinsic (ns)			Extrinsic (ns/pF)		
IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
(LL)	6	6	6	0	0	0
(HH)	6	6	6	0	0	0

Table 5-7. FCTS Specifications (V_{DD} = 2.0 V)

Path	Intrinsic (ns)			Extrinsic (ns/pF)		
IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
(LL)	6	6	6	0	0	0
(HH)	6	6	6	0	0	0

(2) Cautions concerning the use of clock tree synthesis

<1> Circuit overhead must be taken into consideration. The extent of overhead can be estimated with the following formula. However, since the addition of buffers depends on the circuit configuration, the actual overhead is predicted to be smaller than the value obtained with the following formula.
In the following formula, round up decimals to the next integer.

No. of clock buffers: B = N/40 + 9

N ... No. of blocks connected to FCTS
Use the following formula to determine the number of grids.

Overhead grid number = $\alpha \times$ B [grids]

$\alpha = 21$

<2> When calculating the power consumption, be sure to consider the clock frequency at which the above buffers are operating.

<3> Note in advance that, since NEC performs the clock tree synthesis for the layout process, up to one week should be scheduled as the period between when NEC receives the assumed wiring length simulation data and when it produces the actual wiring delay data output.

<4> An increase in alternate wiring due to a large macro or a high cell utilization rate may not prevent adequate suppression of clock skew.

<5> During the actual wiring length simulation, the delay value of the F158 clock tree is divided up as the delay of each branch.
Accordingly, be sure to use the same netlist (the one used for the FCTS block) when performing the actual wiring length simulation.

<6> Clock tree synthesis is used to control the clock line's relative delay, not its absolute delay. The absolute delay depends on factors such as the circuit configuration and chip size, and it may vary greatly from the predicted delay (the above-listed reference values and assumed wiring length delay).
When creating test patterns, be careful that changes in the valid edge of the clock tree's input signal do not have the same timing as changes in other signals; otherwise a test pattern conflict may occur.

5.4.5 Setting and resetting latches and flip-flops

Setting or resetting of latches and flip-flops should be performed only when initializing (except for RS latches). The following problems may occur when it is performed for other purposes.

(1) The ATG (Automatic Test-pattern Generator) for scan paths cannot be used effectively.

(2) Because the signal path becomes complicated, it is hard to verify the circuits, so verification may be less than complete. We therefore recommend the method described above as a means of minimizing hours spent on verification while ensuring complete verification.

(3) The circuit configuration may end up being process-dependent (such as when delay gates are added to secure the minimum pulse width for a reset).

Accordingly, avoid the type of circuit configuration (commonly seen in 74LS circuits) that is shown in Figure 5-22 and instead use the type of circuit configuration shown in Figure 5-21 below.

Figure 5-21. Divide by 5 Counter (Example of Correct Configuration)

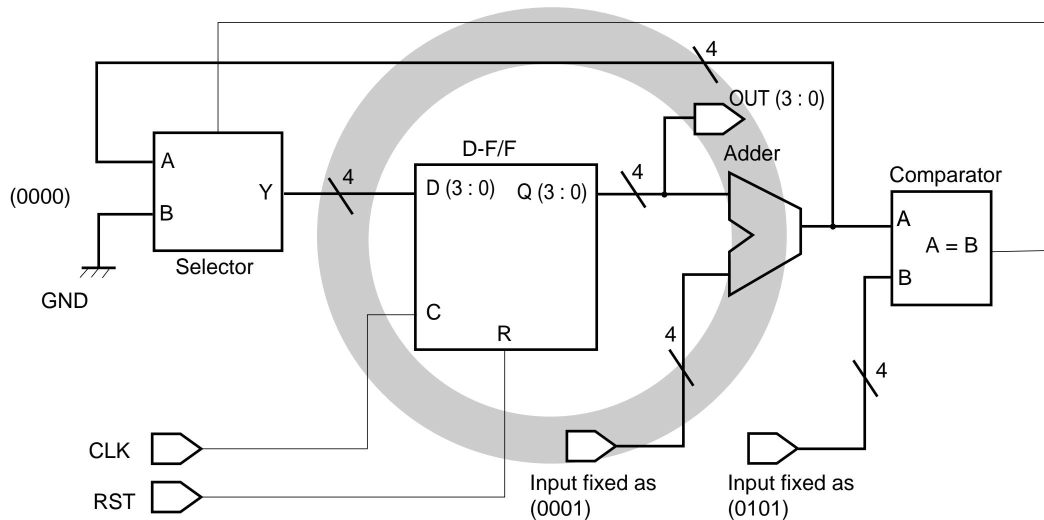
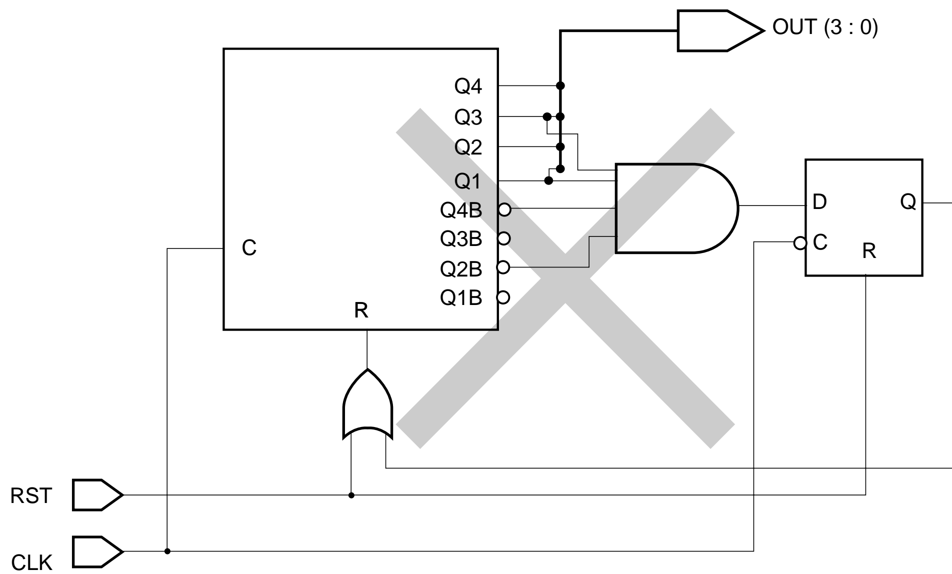


Figure 5-22. Divide by 5 Counter (Example of Incorrect Configuration)



5.5 User Logic Circuit Design for Layout

When designing the user logic, remember that the wiring length between functional cells generally increases in proportion to the user logic size.

When entering data in the circuit drawings, the block allocation data for the second layer can be taken into account as a group entry in the layout.

Consequently, when creating large-scale user logic (over 10,000 gates), do not use just one block for the user logic-instead, we recommend dividing the user logic among several function-specific blocks containing several thousand gates each.

When the user logic has been divided into several blocks containing several thousand gates each, it is possible that the wiring length between blocks will be longer than when only one block is used for the user logic, but the wiring length within each block will tend to be much shorter.

When calculating the assumed wiring length for the simulation, support is provided for programs that calculate the assumed wiring length for each block based on the number of gates in each block and the block allocation information for the second layer.

5.6 Modular Design

When designing a large-scale LSI, a more efficient design can be produced by dividing the chip into modules in a hierarchical design.

This section presents some caution points related to hierarchical design.

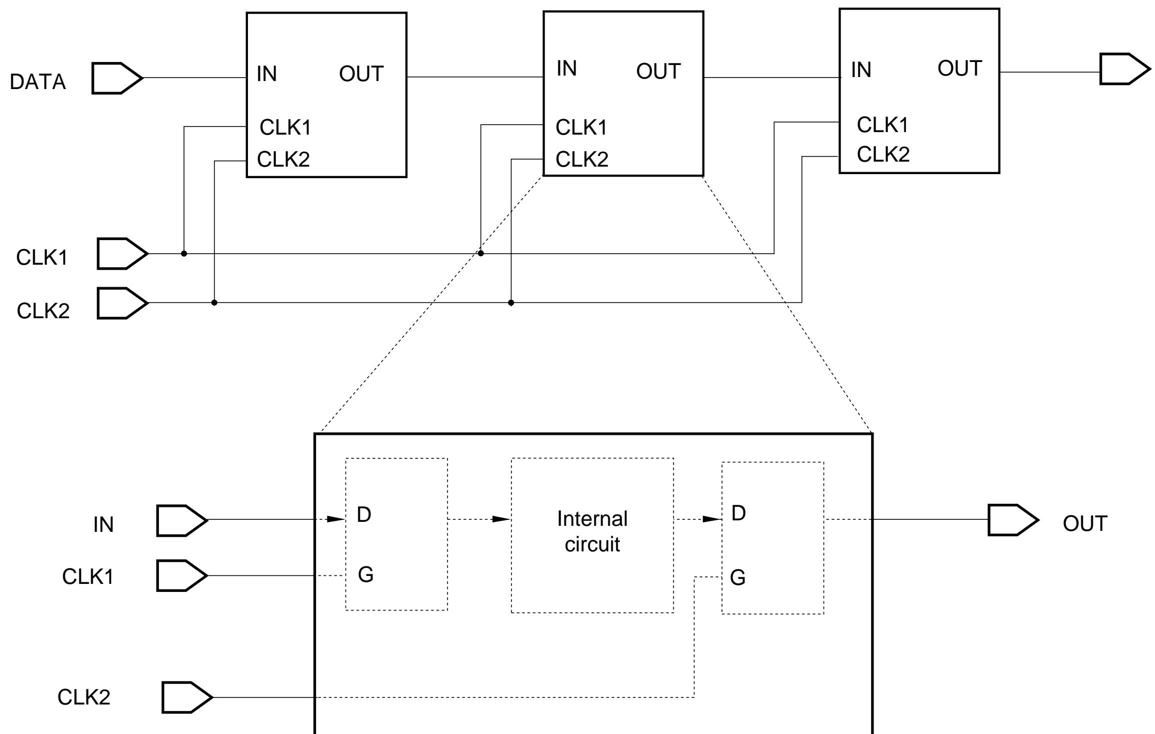
Standardization of interface between macros

One of the greatest problems encountered in hierarchical designs is the inability to complete the design due to incompatible interfaces between macros that are all connected on the same chip.

Therefore, we recommend standardizing the interface between macros to avoid this problem.

Figure 5-23 shows a simple example. In this example, all of the output data from each macro is output after being latched via the CLK2 pin. This means that all input data must be latched via CLK1 before being received. This prevents conflict among data being passed between macros and also standardizes the interface used to pass the data between macros.

Figure 5-23. Standardization of Interface between Macros



In Figure 5-23, the only standardized interface is the one for the control bus for the CLK1 and CLK2 pins. Table 5-8 lists examples of standardized interfaces for all buses.

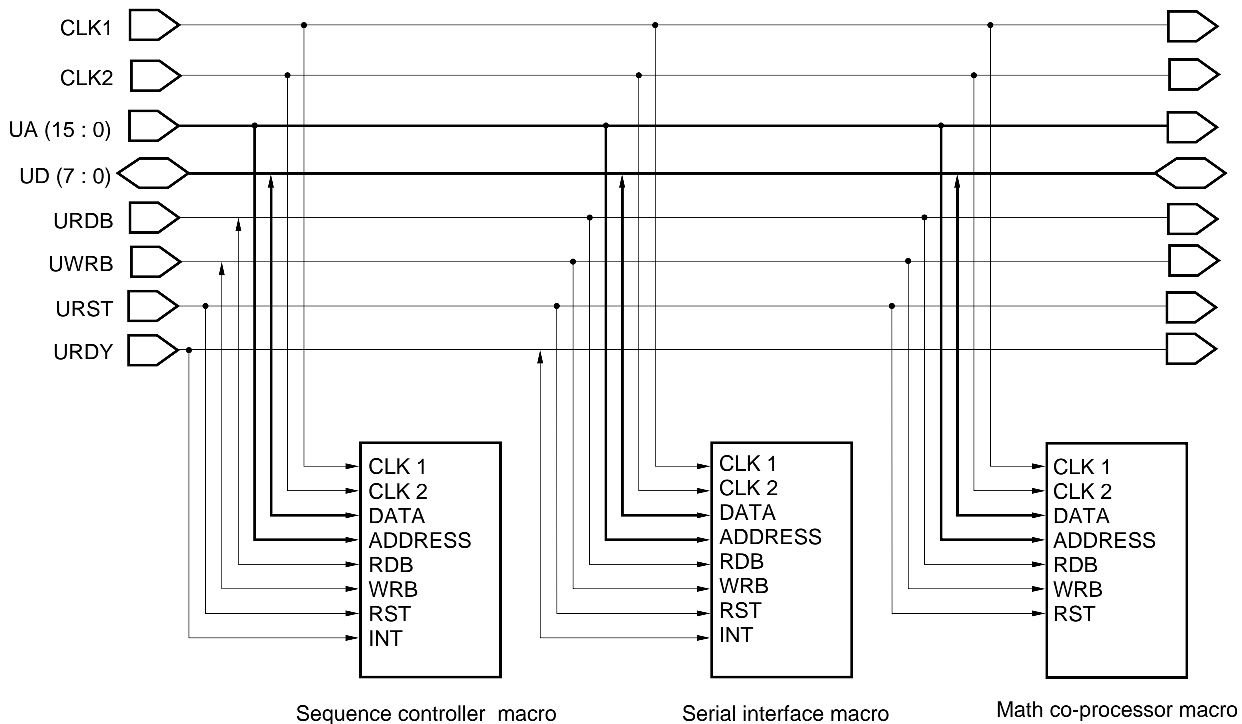
Table 5-8. Example of Standard Bus Interfaces for Single-Chip Design

Pin	Active Level	Pin Function
CLK1		Internal system clock 1
CLK2		Internal system clock 2
UA (15 : 0)		Address bus
UD (7 : 0)		Data bus
URDB	L	Read signal
UWRB	L	Write signal
URST	H	Reset signal
URDY	L	Ready signal for other macros
UALE	H	Address strobe signal

A design whereby standardized buses are defined and various macros are strung from those buses is exactly what is meant by “modular design”.

Once standard interfaces have been defined for all of the buses listed above, the macros can be modularized as shown in Figure 5-24, which is conducive to macro reutilization.

Figure 5-24. Modular Design



CHAPTER 6 USER LOGIC DESIGN

This chapter presents cautions and restrictions related to circuit design.

Unlike when using a TTL-level or CMOS-level standard ICs, when using a CMOS-level cell-based IC in an LSI design, the design cannot be easily revised once it has been made.

Consequently, extra caution is needed when designing this type of LSI, with special attention paid to the various restrictions and design rules described in the chapters entitled **CHAPTER 2 INTRODUCTION TO CELL-BASED ICs, CHAPTER 4 ESTIMATION METHODS FOR CHARACTERISTIC VALUES, CHAPTER 5 SYSTEM DESIGN**, and **CHAPTER 6 USER LOGIC DESIGN** (this chapter).

If a design is done without heeding the design rule, not only can development after interfacing with NEC be expected to take longer, it may even be necessary to rework model-specific designs that have neared completion – so caution is indeed warranted.

6.1 Basic Circuit Configuration

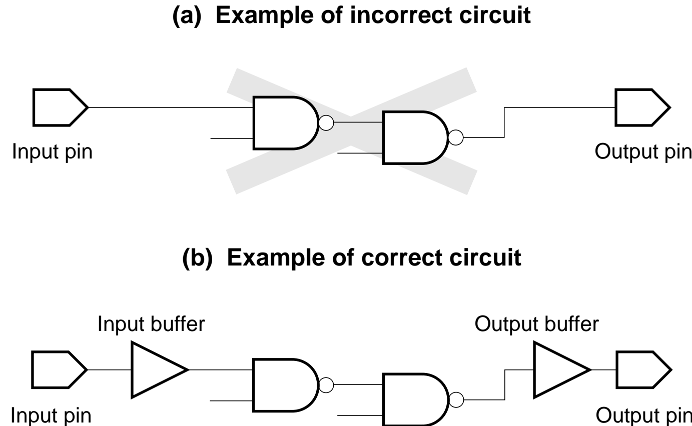
6.1.1 Use of input and output buffers

Be sure to insert input and output buffers between the LSI circuits and the I/O pins (see Figure 6-1).

Reasons: <1> To protect the LSI from damage by static electricity

<2> To gain sufficient drive capacity for output.

Figure 6-1. Basic Circuit Configuration



6.1.2 Handling of unused pins

Note that, regardless of the block, unused input pins cannot be left unconnected. When using an F091 (high/low level generator), be sure to input either a high level or low level to each pin. If any of a block's input pins is left unconnected, its input level will not be defined, which can lead to function defects or increased leakage current (I_L). Therefore, when using the F091, improve wiring characteristics by avoiding the use of too many fan-outs. If several blocks are clamped by one block, too many lines will be concentrated in that section, which will make the placement and routing more difficult. In such cases, divide the circuits into groups of a certain size to avoid such concentration of wiring.

If any of block's output pins are left unconnected, a warning error will be output when a tool is used for the design rule check. Therefore, try to eliminate all unnecessary blocks.

6.1.3 Restriction on fan-out capacity

There are set limits on the number of fan-outs that can be connected to a block's output pins, and the block library specifies the allowable load capacitance for each block.

When the load capacitance to be driven increases, signal rise and fall times become longer and estimations of propagation delay times become imprecise. If the signal rise and fall times become very long, data-through may occur among the flip-flops, which may make it impossible to maintain correct logic operations.

Therefore, be sure to always observe fan-out capacity restrictions when designing circuits.

Also, you should assume a limit of about one-third the load capacitance when designing circuits with strict speed specifications.

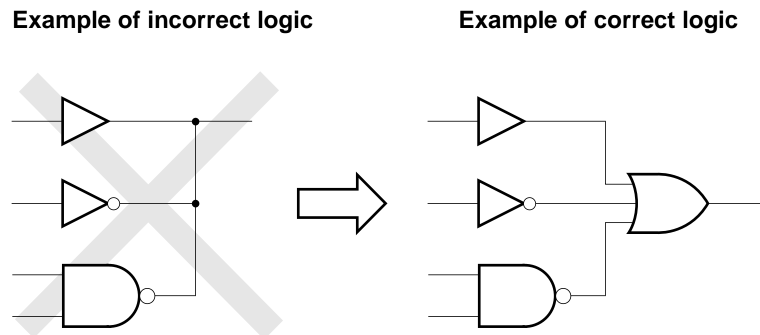
Caution Note that the load capacitance includes not only the fan-in capacitance of subsequently connected blocks but also the wire capacitance.

6.1.4 Prohibition of wired logic

Except for 3-state output, it is not possible to have wired logic configurations in which block outputs are mutually connected.

When block outputs are mutually connected, both P-ch transistors and N-ch transistors become conductive according to the logic state. This sets output to intermediate level and enables a regular current to flow between the V_{DD} and GND pins, which adversely affects the low power consumption feature of conventional CMOS circuits. Therefore, be sure to remain within this restriction.

Figure 6-2. Prohibition of Wired Logic

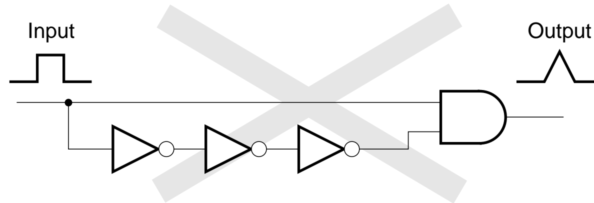


6.2 Prohibition of Differential Circuits

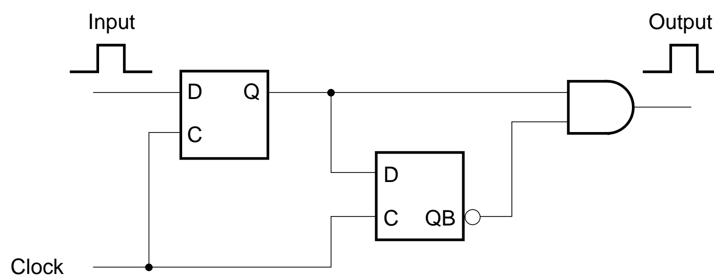
In principle, differential circuits must not be included in the circuit configuration. Since the placement and routing design is performed automatically, it is impossible to guarantee the width of generated internal waveforms, which may prevent the implementation of desired functions. Accordingly, avoid designing circuits such as the one shown in part (a) of Figure 6-3 and instead try to design circuits such as the one shown in part (b) of Figure 6-3.

Figure 6-3. Prohibition of Differential Circuits

(a) Example of incorrect circuit



(b) Example of correct circuit

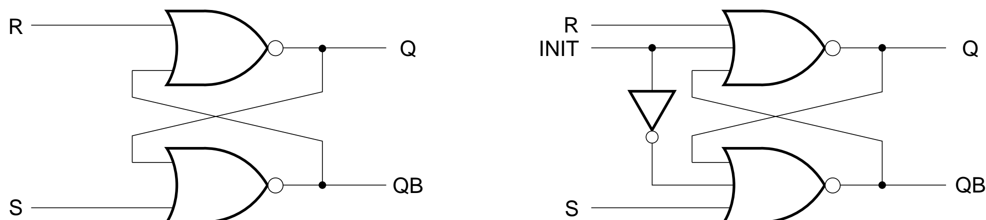


6.3 RS Latches and Loop Circuits

6.3.1 RS latches

Do not use asynchronous RS latches for gate configurations. Not only do such RS latches cause initialization to fail during simulation, they can also result in speed variations on each circuit's path according to the placement and routing results.

Figure 6-4. Asynchronous RS Latch

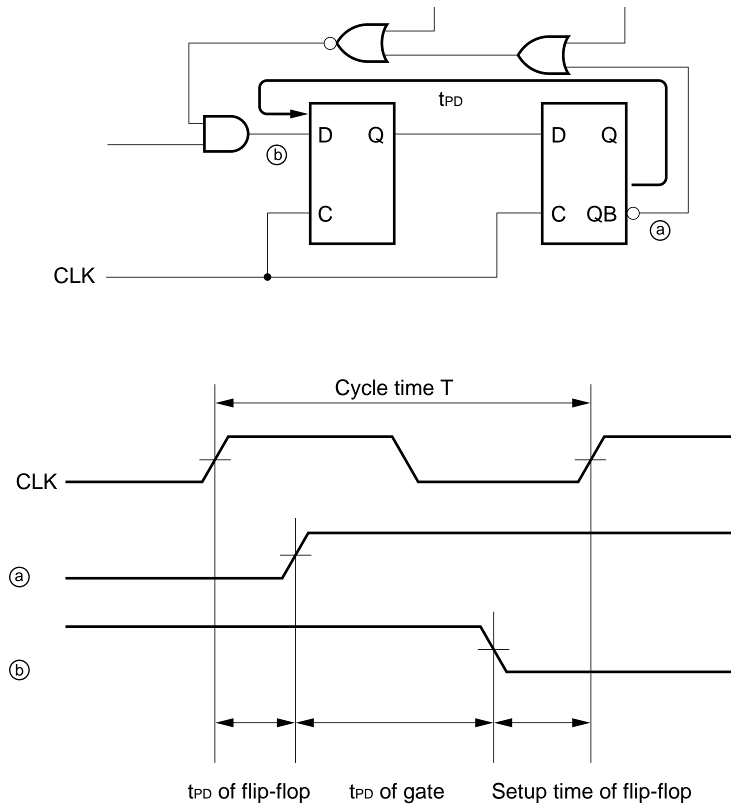


6.3.2 Loop circuits

If your design includes any loop circuits, such as feedback loops, be sure to note the following points.

(1) If gates are inserted in feedback loops for divider circuits, such as is shown in Figure 6-5, the delay time generated by the gates will have an adverse effect on frequency characteristics. Therefore, be sure to determine the loop's delay time in advance to confirm adequate frequency characteristics. For details of how to make this confirmation, see **6.5 Delay Time Margin** below.

Figure 6-5. Loop Circuit



Remark $f_{MAX.} = 1/T$

(2) Loop circuit configurations cannot be used as they are when configuring scan paths.
In such cases, try a countermeasure, such as using gates (or other elements) to isolate the loop circuits.

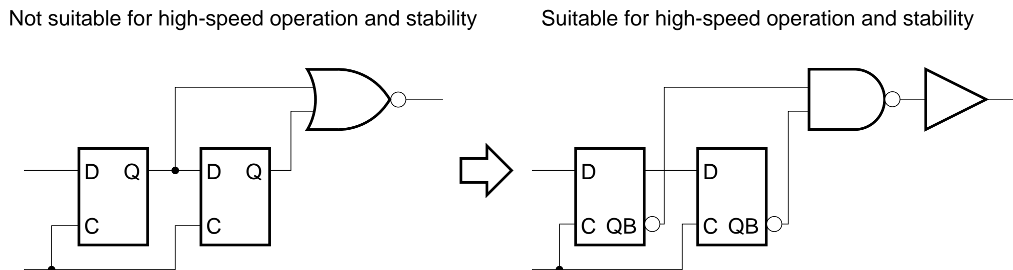
6.4 Cautions Concerning High-Speed Circuit Configurations

Generally, when the characteristics of P-ch transistors and N-ch transistors are compared, we find that the N-ch transistors are able to carry a larger current. Therefore, NOR gates that are directly connected to P-ch transistors have reduced load driving capacity at the rising edge of the output signal. For example, NOR-type blocks are slower than NAND-type blocks and also have inferior fan-out characteristics.

When configuring circuits, note the following points concerning circuit blocks to be operated at high speeds.

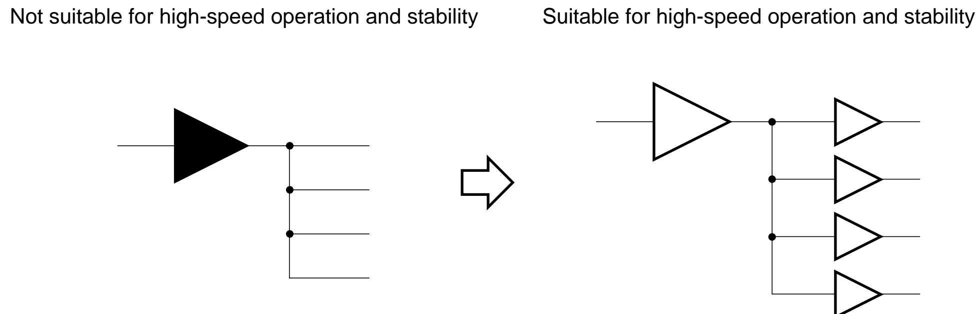
(1) Use methods such as logic conversion to configure standard NAND-type blocks for the circuits to be operated at high speeds.

- This increases the circuit's speed and improves its stability.



(2) Configure circuits to be operated at high speeds using as few fan-outs as possible (to reduce the load).

- As a yardstick, try to keep within one-third to one-half of the fan-out limit value.



(3) Convert from low-power blocks to standard blocks.

6.5 Delay Time Margin

Logic circuits are configured of combination circuits that uniquely determine output according to the input status, and sequential circuits that determine output according to the input status and the previous status. Specifically, sequential circuits include gate circuits and flip-flops and latch circuits that provide feedback.

When factors such as testability and the ease of estimating the delay-time design are considered, it becomes evident that the sizes of the combination circuits and sequential circuits cannot be very large. Also, most sequential circuits are operated using a system clock that includes an adequate margin for the delay time of combination circuits.

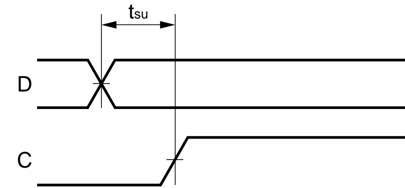
In cases where the clock does not provide an adequate delay time margin, the “entrance” timing (i.e., the input timing for flip-flops and latches) must be secured.

6.5.1 Timing definitions

(1) Setup time (t_{su})

In latches or flip-flops, this is the data setup time that is required to read data at the active edge of the clock.

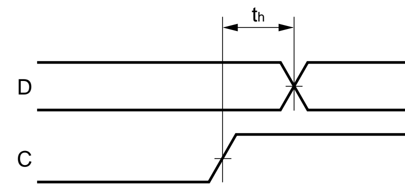
Figure 6-6. Setup Time



(2) Hold time (t_h)

In latches or flip-flops, this is the data hold time that is required to read data at the active edge of the clock.

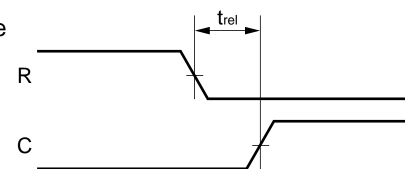
Figure 6-7. Hold Time



(3) Release time (t_{rel})

In latches or flip-flops, this is the time that is required between when a reset (or set) operation is released and when the next clock's active edge becomes valid.

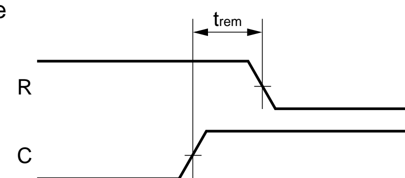
Figure 6-8. Release Time



(4) Removal time (t_{rem})

In latches or flip-flops, this is the time that is required between when a reset (or set) operation is released and when the clock's active edge becomes invalid.

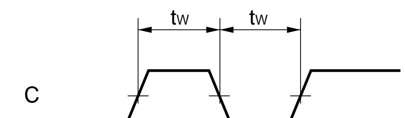
Figure 6-9. Removal Time



(5) Minimum pulse width (t_W)

In latches or flip-flops, this is the minimum time needed for the clock (or reset/set) pulse width in order to correctly read data.

Figure 6-10. Minimum Pulse Width



6.5.2 Delay time margin calculation method (asynchronous circuits)

As an example of how to calculate the delay time margin, let us consider the setup time and hold time in the circuit shown in Figure 6-11. Condition settings for variation and wiring length should be set so as to minimize this margin. Normal operation can be judged as enabled when the rated values (t_{su} and t_h) for each block have been met.

Figure 6-11. Circuit Example for Delay Time Margin Calculation

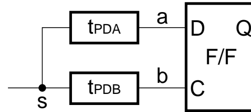
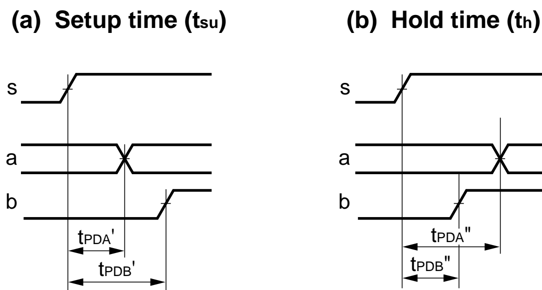


Figure 6-12. Estimated Timing

(a) Setup time (t_{su}) **(b) Hold time (t_h)**



Formula for calculation

$t_{SU} < t_{PDB'} - t_{PDA'}$

$= t_{PDB\ (MIN.)} - t_{PDA}\ [MIN.\ (max.)]$

$= t_{PDB\ (MIN.)} - t_{PDA\ (MIN.)} \times \frac{1 + \alpha}{1 - \alpha}$

$t_h < t_{PDA''} - t_{PDB''}$

$= t_{PDA\ (MIN.)} - t_{PDB}\ [MIN.\ (max.)]$

$= t_{PDA\ (MIN.)} - t_{PDB\ (MIN.)} \times \frac{1 + \alpha}{1 - \alpha}$

α : Variation coefficient (0.1)

6.5.3 Delay time margin calculation method (high-speed circuits)

Since circuits that use a high operating frequency have a short clock cycle time, there is a small operating margin for the delay time of internal function blocks.

Described below are delay time margin calculation methods for in-phase and negative phase circuit configurations.

(1) In-phase clock

Let us consider the operation of a shift register (such as shown in Figure 6-13) that contains delay time “A” between flip-flops F1 and F2. Figure 6-14 shows the verification point for this circuit, which is to check whether or not the data (Q of F1) output via sampling timing <1> is input to F2 after delay time “A” has elapsed and whether or not the data is correctly read via sampling timing <2>.

In other words, the amount of time that results when the maximum delay time at point a is added to the setup time must be no greater than the cycle time (T).

Figure 6-13. In-Phase Clock Circuit Example

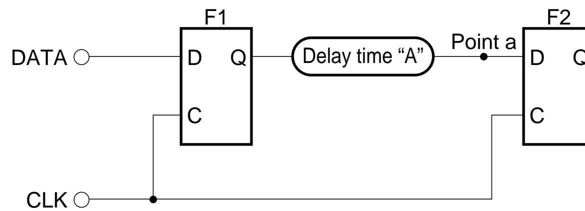
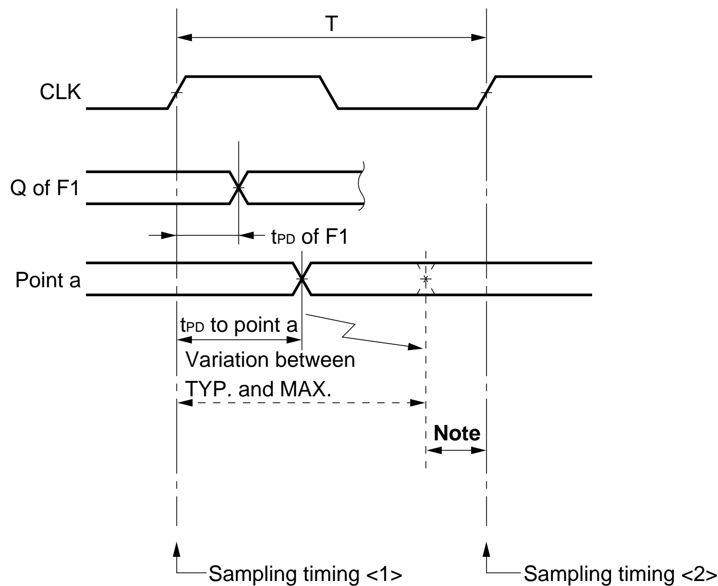


Figure 6-14. Timing for In-Phase Clock



Note Taking F2’s setup time into account, do not overshoot the next sampling timing.

Formula for calculation

$T - (t_{PD\ (F1)\ (MAX.)} + t_{PDA\ (MAX.)}) > t_{SU\ (F2)}$

The following countermeasures are needed if this relational expression is not satisfied.

- Reduce the delay time value of delay A.
- Lower the operating frequency (to lengthen cycle T).

(2) Reverse-phase clock

Figure 6-15 is similar to Figure 6-13 except that the active edge of the F2 clock is changed to the opposite phase. Both the rising edge and falling edge of CLK are used, so the operating margin varies according to CLK's duty. The following are the conditions for this circuit's normal operation.

Figure 6-15. Reverse-Phase Clock Circuit Example

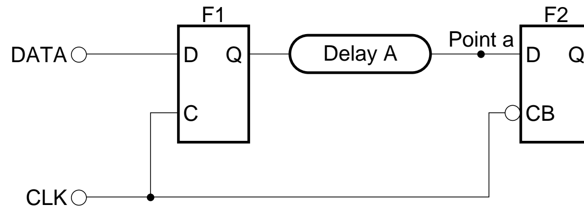
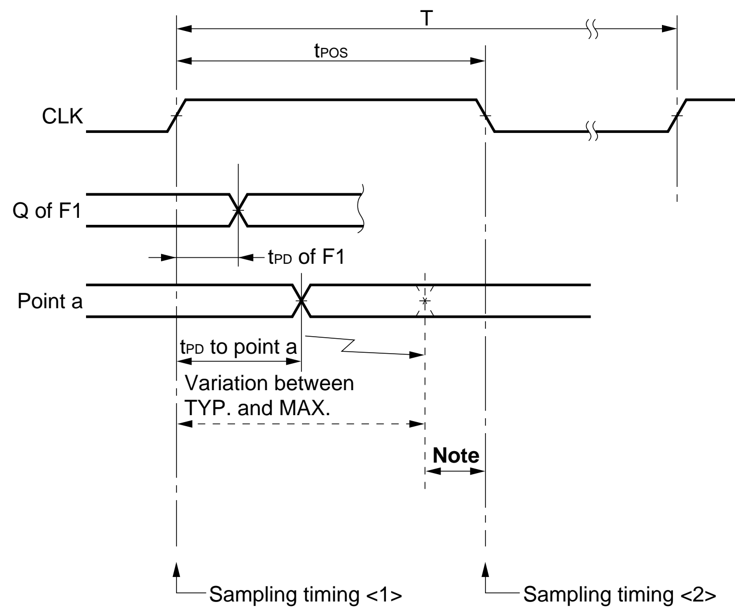


Figure 6-16. Timing for Reverse-Phase Clock



Note Taking F2's setup time into account, do not overshoot the next sampling timing.

Formula for calculation

$t_{POS} - (t_{PD\,(F1)\,(MAX.)} + t_{PDA\,(MAX.)}) > t_{SU\,(F2)}$

The following countermeasures are needed if this relational expression is not satisfied.

- Reduce the delay time value of delay A.
- Lower the operating frequency (to lengthen cycle T).
- Increase CLK's duty.

6.5.4 Minimum pulse width

In high-speed circuits, the delay differential between a signal's rising edge and falling edge and the relative variation on the same path may result in cases that do not meet the condition imposed by the minimum pulse width of a flip-flop's input clock.

Let us consider the circuit example shown in Figure 6-17. The signal that is input to CLK is input to the flip-flop's clock after delay B has elapsed, via the timing shown in Figure 6-18. As for delay B, if delay $t_{PDB\ (LL)}$ that occurs for the falling edge is greater than delay $t_{PDB\ (HH)}$ that occurs for the rising edge, then t_{NEG} is greater than $t_{NEG\ (MIN.)}$, which means that the pulse is too thin. When estimating the $t_{NEG\ (MIN.)}$ value, set the maximum $t_{PDB\ (LL)}$ value and reduce the $t_{PDB\ (HH)}$ value in the direction of minimizing the relative variation.

Figure 6-17. Estimation of Minimum Pulse Width

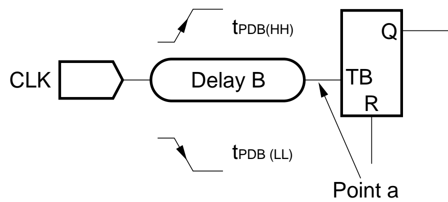
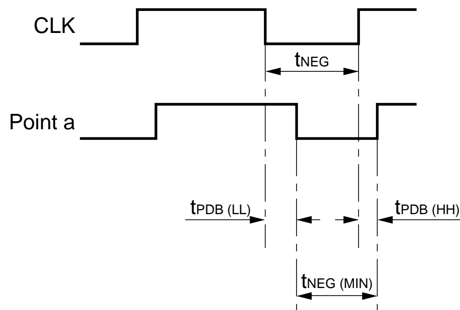


Figure 6-18. Reduction of Pulse Width



Formula for calculation

$t_{NEG\ (MIN.)} = t_{NEG} + (t_{PDB\ (HH)\ (MAX.)} - t_{PDB\ (LL)}\ [_{MAX.\ (min.)}]) > t_W$

$\rightarrow t_{NEG\ (MIN.)} = t_{NEG} + (t_{PDB\ (HH)\ (MAX.)} - t_{PDB\ (LL)\ (MAX.)} \times \dfrac{1-\beta}{1+\beta} > t_W$

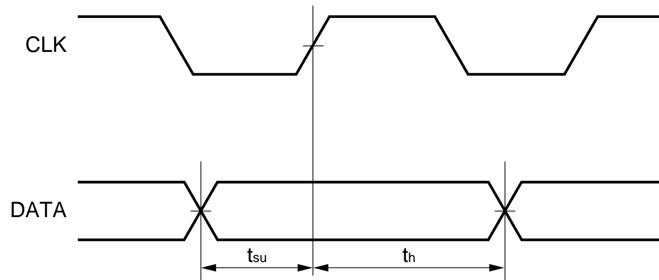
β: Variation coefficient (0.1)

One method for adjusting the minimum pulse width of the signal that is input to the flip-flop's clock is to control $t_{PDB(HH)}/t_{PDB(LL)}$ so as to increase the effective duty. In other words, if the function block included in delay B in the above example is changed so that the falling edge delay $t_{PDB(LL)}$ is the fast type and the rising edge delay $t_{PDB(HH)}$ is the slow type, then the $t_{NEG\ (MIN.)}$ value will increase. When doing this, be careful to ensure that the high-level pulse width meets the minimum pulse width rating.

6.5.5 Metastable

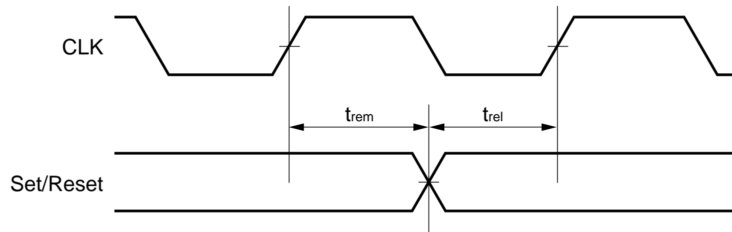
When the ratings stipulated for setup and hold times are not met and transitions between clock and data or between clock and set/reset occur at the same time, the output from flip-flops and latches may oscillate so that they are at an intermediate level that is neither high level or low level. This unstable condition is called a “metastable” condition. A metastable condition is terminated after a certain amount of time has elapsed, and the output returns either to high level or low level. However, since the confirmed level has absolutely no relation to the data input level, an unstable condition persists. Therefore, in cases where it is impossible to meet the rated values for setup time, hold time, release time, and removal time, be sure to implement countermeasures to prevent this type of unstable condition from spreading to the entire circuit.

Setup time (t_{su}) ...... Time during which the data signal must be acknowledged before the clock signal changes
Hold time (t_h) .... Time during which the data signal must be held after the clock signal changes



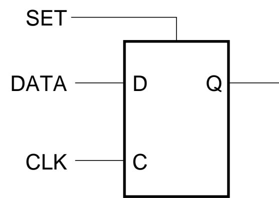
Caution The rated time values must be met (see Block Library).

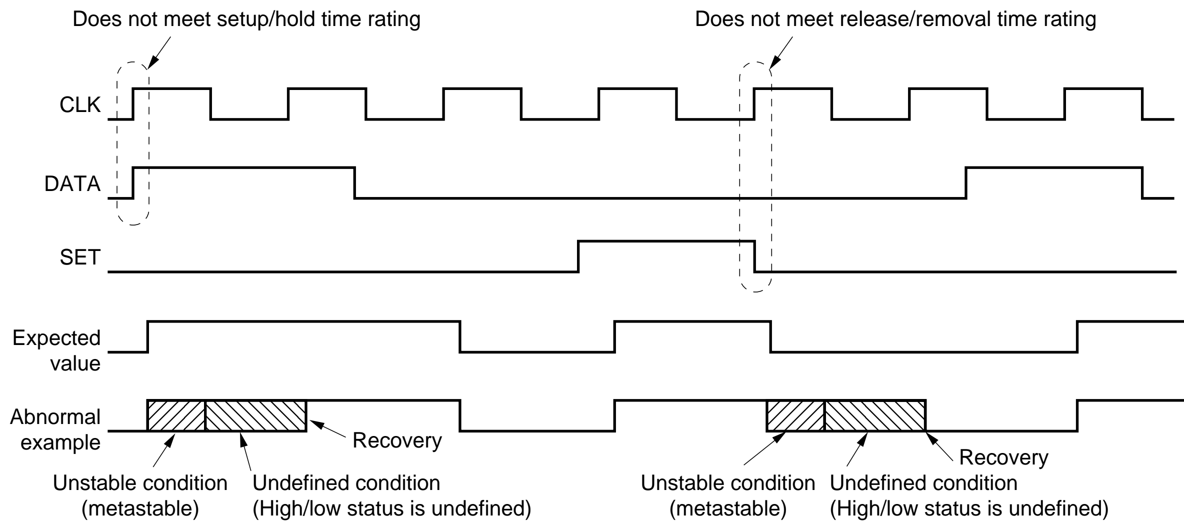
Release time (t_{rel}) .... Time from when set/reset signal changes and until clock becomes valid
Removal time (t_{rem}) ..... Time from when set/reset signal changes and until clock becomes invalid



Caution Do not remove a set or reset signal near the clock’s active edge.

(1) Metastable occurrence and recovery time





In CB-9 Family VX/VM type devices, the duration of the metastable condition is specified as follows. After this metastable time has elapsed, the signal is either high or low but the level cannot be defined (see the "undefined" parts of the above figure).

Metastable time = $t_{PD\ (MAX.)} \times 6$

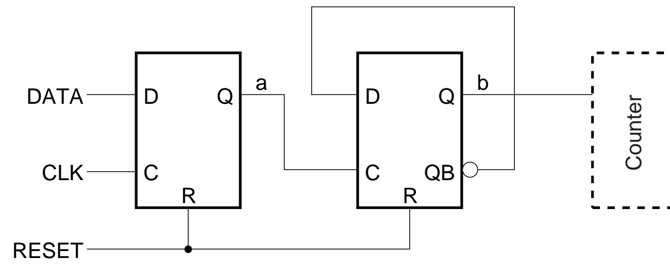
$t_{PD\ (MAX.)}$ .... Maximum value of delay time between clock's active edge and change in output (when the setup/hold time rating is not met) or release/removal time (when the release/removal time rating is not met).

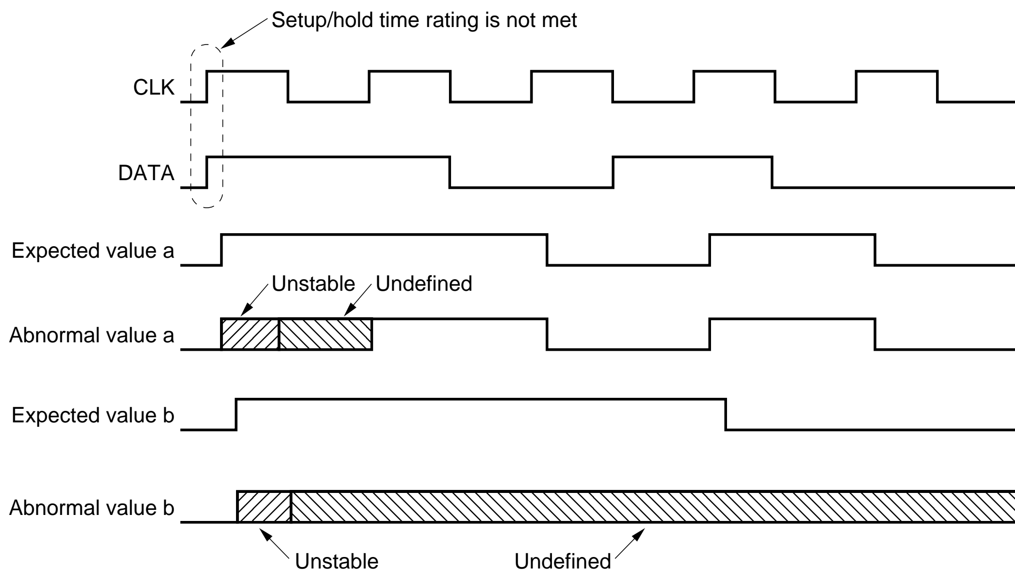
(2) Measures to avoid metastable conditions

If various time ratings (such as for asynchronous input signals) cannot be met, configure the circuit so that any metastable condition that occurs does not affect subsequent circuit components. Examples of abnormal and avoiding abnormality are shown in the following.

Example of abnormal

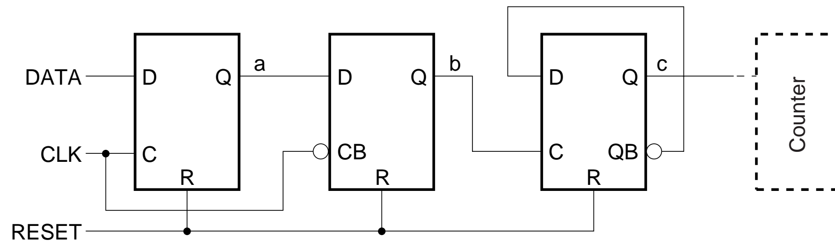
When the output from “b” in the following figure is input to a counter, the operation can last for several extra counts.

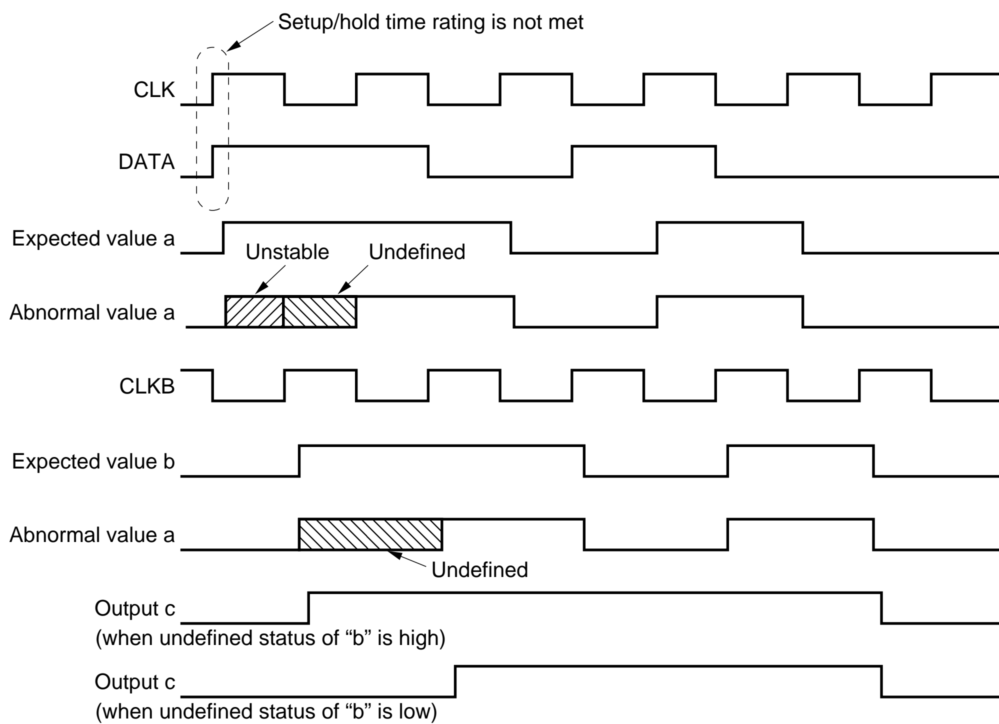




Example of avoiding abnormality

Output c can be stabilized by inserting flip-flops. However, two values are possible during the first clock cycle of c, depending on the next level after the undefined condition at b. In the following example, this does not affect the counter.





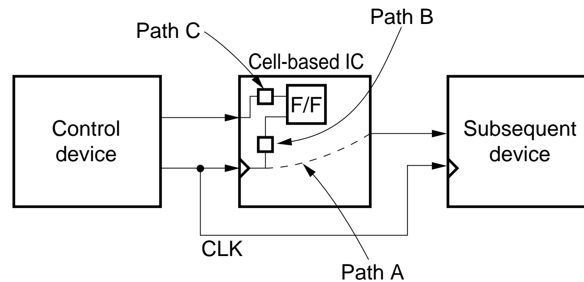
Remark Clock width > $t_{PD\ (MAX.)} \times 6 + t_{setup/hold}$

6.5.6 Critical path

As shown in Figure 6-19, the critical path can be defined as the path that implements the cell-based IC's required delay time in relation to the system timing that includes the cell-based IC. In this example, the following paths should be studied in detail as critical paths.

- Path A .... Since the cell-based IC's output is sampled using CLK, does this meet the input timing of subsequent devices?
- Paths B and C ...... Does the control device's output timing satisfy the sampling timing within the cell-based IC?

Figure 6-19. System that Includes Critical Paths



There are three types of critical paths.

<1> Critical path between input and output
<2> Critical path between input and input
<3> Critical path between output and output

The verification method and specification method for these critical paths are described below.

(1) Critical path calculation and design

The placement and routing is performed after determining the layout scope for each macro layer (first layer only). Consequently, the wire length within a macro may differ greatly from the wiring length between macros.

<1> Critical paths are completed (except for the I/O buffers) within one macro layer (first layer).
<2> Critical paths should be as simple as possible so as to minimize the load connected to the paths (the fan-out value should be about one-third of the limit value).
<3> Except as noted above, a critical path between the input and output pins should be laid out as close as possible to the target input and output pins.
<4> Try not to include circuits other than critical path circuits within the macro layer.

(2) Critical path between input and output

This corresponds to "Path A" in Figure 6-19. Basically, this path is not affected by other inputs. Design it so that the t_{PD} MAX. value is less than the value required by the system.

Also, note that the output buffer's delay time depends greatly on the external load capacitance (C_L).

Formula for calculation

$t_{PD\ (MAX)}$ < Specified value for system

(3) Critical path between input and input

This path is used to study the input sampling timing. Refer to the calculation example in the circuit configuration shown in Figure 6-20. Since a clear specification of the timing between the input pins is needed to verify the timing, assume for the sake of this calculation that the timing of a signal input from an external source is as shown in Figure 6-21.

Figure 6-20. Example of Critical Path between Input and Input

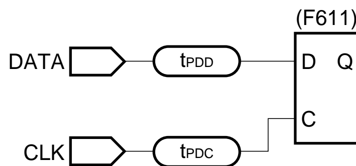
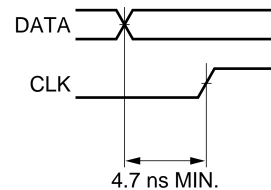


Figure 6-21. Verification of Setup Time



Consider the following points as usage conditions.

- The absolute variation should be in the direction of a smaller margin.
- The relative variation should be in the direction of a greater t_{PDD} value and a smaller t_{PDC} value.

The equation used for this judgment is shown below.

Formula for calculation

It is assumed that DATA has a 4.7 ns (MIN.) time differential in relation to CLK, as is shown in Figure 6-21.

$t_{PDC\ (MIN.)} - t_{PDD}\ [_{MIN.\ (max.)}] + 4.7 > t_{SU}$

$\rightarrow t_{PDC\ (MIN.)} - t_{PDD\ (MIN.)} \times \frac{1+\alpha}{1-\alpha} + 4.7 > t_{SU}$

α: Variation coefficient (0.1)

6.5.7 Conditions for securing operating margin

If the results of the delay margin check and critical path check show that the circuit's operating margin is inadequate, various countermeasures can be performed depending on the circuit configuration.

Generally, these countermeasures are as follows.

<1> Countermeasures based on reevaluation of input and output specifications

- Reduce variation in the input $f_{MAX.}$ value and input $f_{MAX.}$ duty.
- Relax the timing between inputs and between outputs, reduce the output load capacitance, etc.

<2> Reevaluate the pin layout

- Shorten the wiring length (move layout closer to pins) to reduce the delay between the input and output.

<3> Countermeasures based on circuit modifications

- Simplify the circuit to reduce the delay time.
- Reduce the circuit's load to reduce the delay time.
- Insert delay gates to remove the margin.

When implementing countermeasures based on circuit modifications, some delay calculations (recalculations) are necessary, but when inserting delay gates the output wiring length of inserted gates should be estimated as 0 mm.

6.6 Configuration of Internal Buses

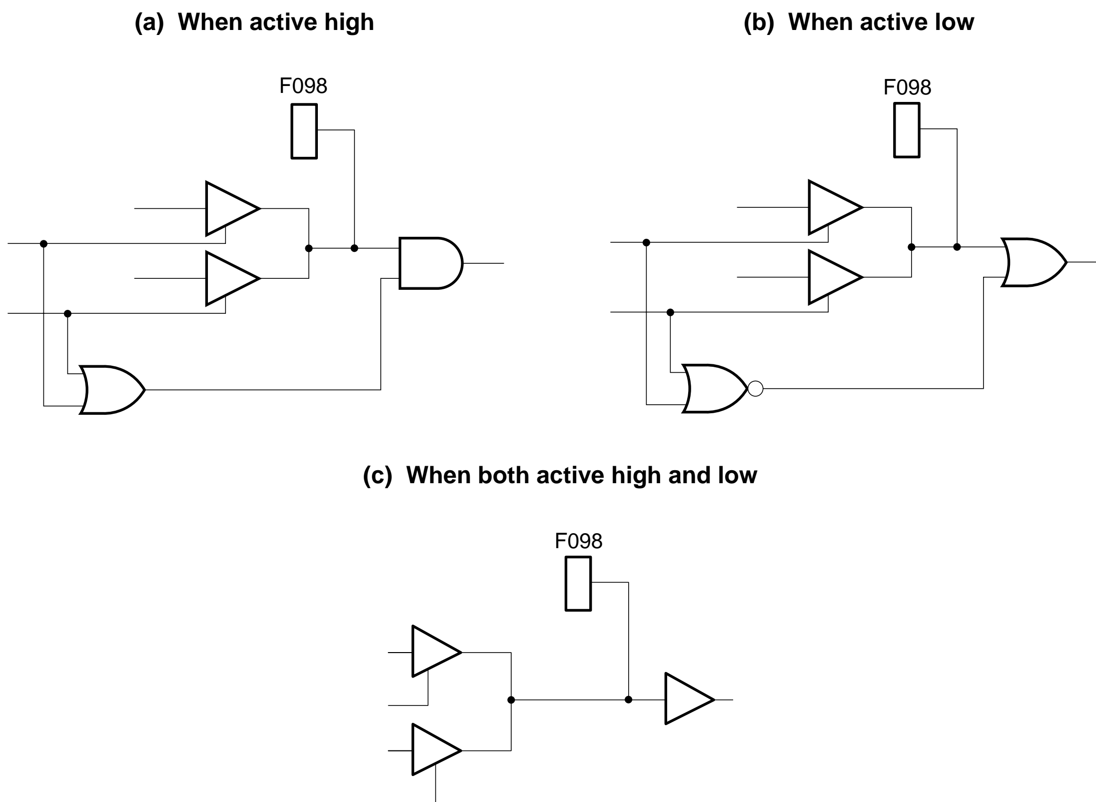
6.6.1 Internal bus configuration method

The data selector type and the bus format type are two typical methods used to select multiple data. If the data selector (multiplexer) is used too much, the circuit configuration becomes rather complicated. Although the bus configuration is simple compared to the circuit configuration and it does not increase cell utilization very much, it may increase the propagation delay time. Select the method that best suits the target circuit configuration.

★ 6.6.2 Prevention of high impedance

When using an internal bus, the basic rule is that only one output enable status can be used for all blocks that are configured along the same bus line. Also ensure that one bus holder (F098) is connected per bus line to prevent input from the next block entering a high-impedance state. Configuration examples are shown in Figure 6-22.

Figure 6-22. Configuration Examples of Circuits for Preventing High Impedance of Internal Bus



(a) When active high **(b) When active low**

(c) When both active high and low

Remark When using F098 (bus holder) in the high-impedance protect circuit in the internal bus, some restrictions apply.
For details, refer to section **6.6.3 Restrictions when using bus holder (F098) with internal bus**.

Also, if two or more outputs are enabled on the same bus line, skewing of the enable signal must be considered to enable these statuses to converge within 12 ns.

6.6.3 Restrictions when using bus holder (F098) with internal bus

Because the driving capacity of the F098 is extremely weak, it is easily affected by noise, and therefore not guaranteed to hold the value. Be sure to use the bus holder only for the purpose of preventing a high-impedance status.

★ 6.6.4 Cautions regarding occurrence of overcurrent at power application

When a bus has been configured inside the LSI, overcurrent may occur between when the power is applied and when the control pin is secured due to bus fighting or floating. Although bus floating can be prevented by connecting a bus holder, there are no countermeasures for bus fighting.

A selector configuration using a 2-state signal must therefore be used for systems that are vulnerable to overcurrent at power application.

Note also that before being used, the core's 3-state output pins must be converted to 2-state signals using the control pin as shown in **Figure 5-4. Example of Countermeasure against High-Impedance Output**.

6.7 Testability Considerations

Important elements in user logic design include not only logic design but also design that considers test methods and test circuits. Consequently, be sure to consider the following points before designing circuits or creating test patterns.

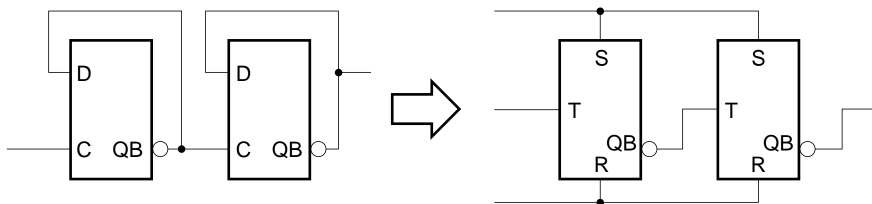
- Initialization of flip-flops
- Division of counter
- Addition of test pins
- Division (modularization) of internal circuits according to test pins

6.7.1 Initialization of flip-flops

When voltage is applied to a block such as a flip-flop or counter, it is impossible to know whether the immediate output status will be low-level or high-level output. Accordingly, for a simulation the first few test patterns must be used to set the initial status.

In the design, be sure to include blocks that have reset inputs so that the initialized patterns will not be too long and internal circuit's initial status can always be set.

Figure 6-23. Initialization of Flip-Flop

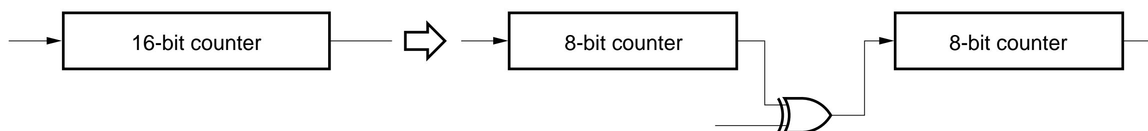


6.7.2 Division of counter

Counters that handle large numbers of bits can be divided into several smaller bit counters to reduce the number of test patterns.

For example, while 2^{16} pulses are needed to reach the final stage during operation of a 16-bit counter, if (as shown in Figure 6-24) this 16-bit counter is divided into two 8-bit counters, the same operation can be performed with only 1/100th to 1/200th the number of pulses needed for the 16-bit counter.

Figure 6-24. Division of Counter



6.7.3 Addition of test pins and division of circuits

As was mentioned in section 6.7.2, LSI testing becomes easier and the number of test patterns is reduced when a TEST pin whose operation mode can be externally set is implemented for testing multi-bit counters or large macros.

(1) One LSI testing method that is especially effective when internal operations are divided into several modes is to establish a separate test mode along with a TEST pin for this test mode.
(2) Often, a large circuit will be configured of several internal macros (modules). In such cases, an effective LSI testing method is to establish a TEST pin for each of these internal modules so that separate LSI tests can be performed for the divided modules.

6.8 Racing and Spike Noise

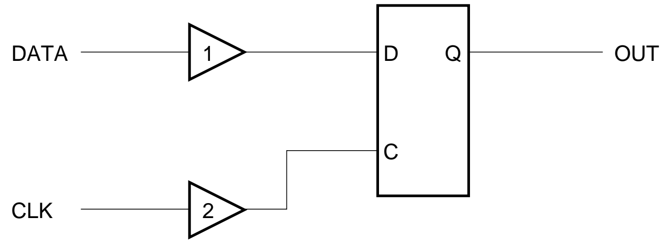
6.8.1 Racing (conflict)

"Racing" refers to status changes that occur when the timing of two or more signals is very close in some logic blocks.

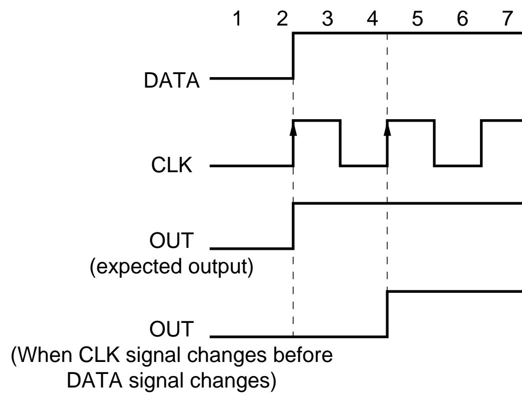
When the test pattern shown in part (b) of Figure 6-25 is applied to the circuit shown in part (a) of Figure 6-25, the delay differential between buffers 1 and 2 and the corresponding wire delay differential may alter the timing of the flip-flop's data and clock signals so that they do not operate as expected. Concerning the circuit shown in part (a) of Figure 6-25, first set the data signal to the flip-flop, then consider where the clock signal will change afterward. The test pattern shown in part (c) of Figure 6-25 is an example of this approach.

Figure 6-25. Racing

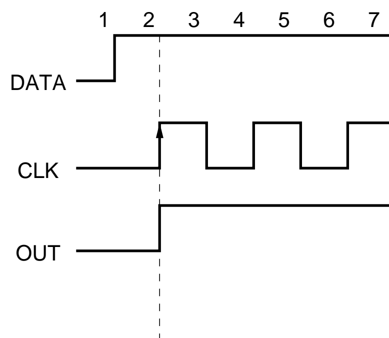
(a) Circuit in which racing can occur



(b) Test pattern in which racing can occur



(c) Test pattern designed to prevent racing



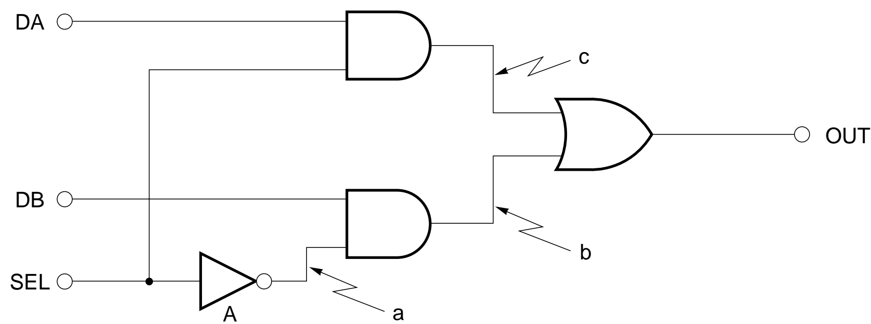
6.8.2 Spike noise

Spike noise is noise that is generated by very small shifts in input timing that occur when two or more input signals change at the same time in a circuit that uses a gate that has two or more inputs. The spike noise's time period varies according to the size of the timing shift. When the spike noise is input to clock or set/reset inputs on a subsequent flip-flop, operation faults may occur in all signal routes related to (affected by) the flip-flop's output signal.

For example, when using a gate that has two or more inputs, it is important to determine whether spike noise that occurs when two or more input signals change at the same time affects subsequent gates or external output signals, and whether an operation fault occurs as a result. If it is determined that spike noise can pose problems in subsequent gates, etc., either the test pattern or the circuit must be modified to prevent such problems.

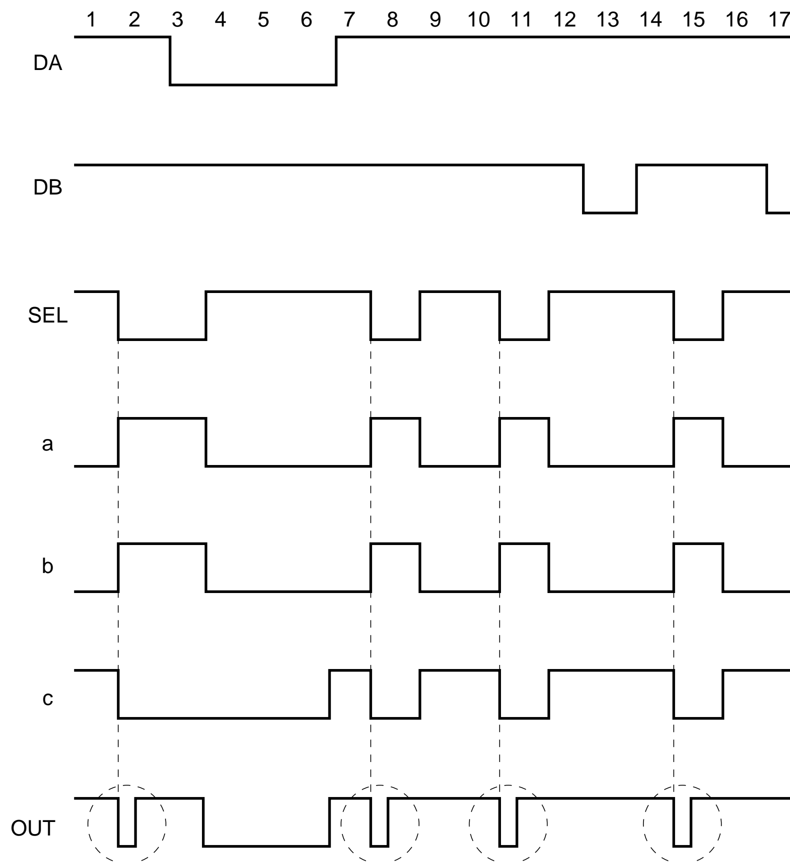
An example of spike noise and a corresponding countermeasure are described below.

Figure 6-26. Data Selector Circuit Example



In this example, the test pattern shown in Figure 6-27 is created for use in the AND-OR data selector circuit shown in Figure 6-26.

Figure 6-27. Test Pattern Example (Before Modification)



In this example, the select signal (SEL) changes from "H" to "L" when two input signals (data signals DA and DB) are held at high level, which causes spike noise to occur in the output signal (OUT). In the test pattern shown in Figure 6-27, spike noise occurs in four places in the pattern indicated by numbers 2, 8, 11, and 15.

As can be seen in the circuit diagram, when DA and DB are at high level, the statuses of signals b and c are determined according to the SEL signal's status. When SEL has changed from "H" to "L", b changes from "L" to "H" and c changes from "H" to "L". Meanwhile, signal a, which has passed via inverter A, is slowed by the delay value of inverter A and therefore lags behind the SEL signal, while signal b consequently is slowed (by inverter A's delay value) behind signal c. Therefore, an "L, L" status is simultaneously generated between signals b and c in 2, 8, 11, and 15 patterns , which results in generation of "H → L → H" spike noise in the OUT pattern.

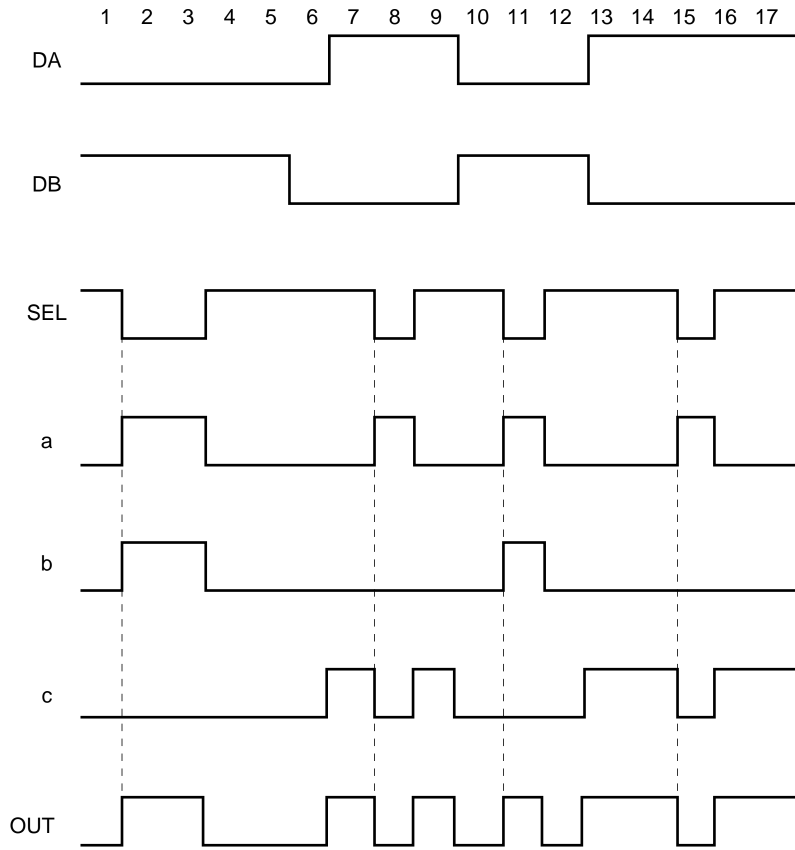
The following two countermeasures can be implemented if the spike noise is input to a flip-flop's clock or set/reset inputs.

<1> Prevent output from a flip-flop from being changed by spike noise, such as by preventing data signal transitions at the same timing whereby spike noise is generated.

<2> Modify the test pattern.

In the case shown in this example, one or both of the DA and DB signals are held low when SEL goes from “H” to “L”. If the timing design from Figure 6-28 is used, spike noise no longer occurs in the OUT pattern.

Figure 6-28. Test Pattern Example (After Modification)



CHAPTER 7 TOTAL CHIP SIMULATION FOR CHIP WITH CPU CORE

7.1 General

Total chip simulation refers to a simulation of the entire chip to check for system-level problems in the circuitry.

This chapter focuses on simulation methods used for chips that include a CPU core.

If the target chip does not include a core (other than memory), perform the total chip simulation using the type of methods that are used for user logic simulations.

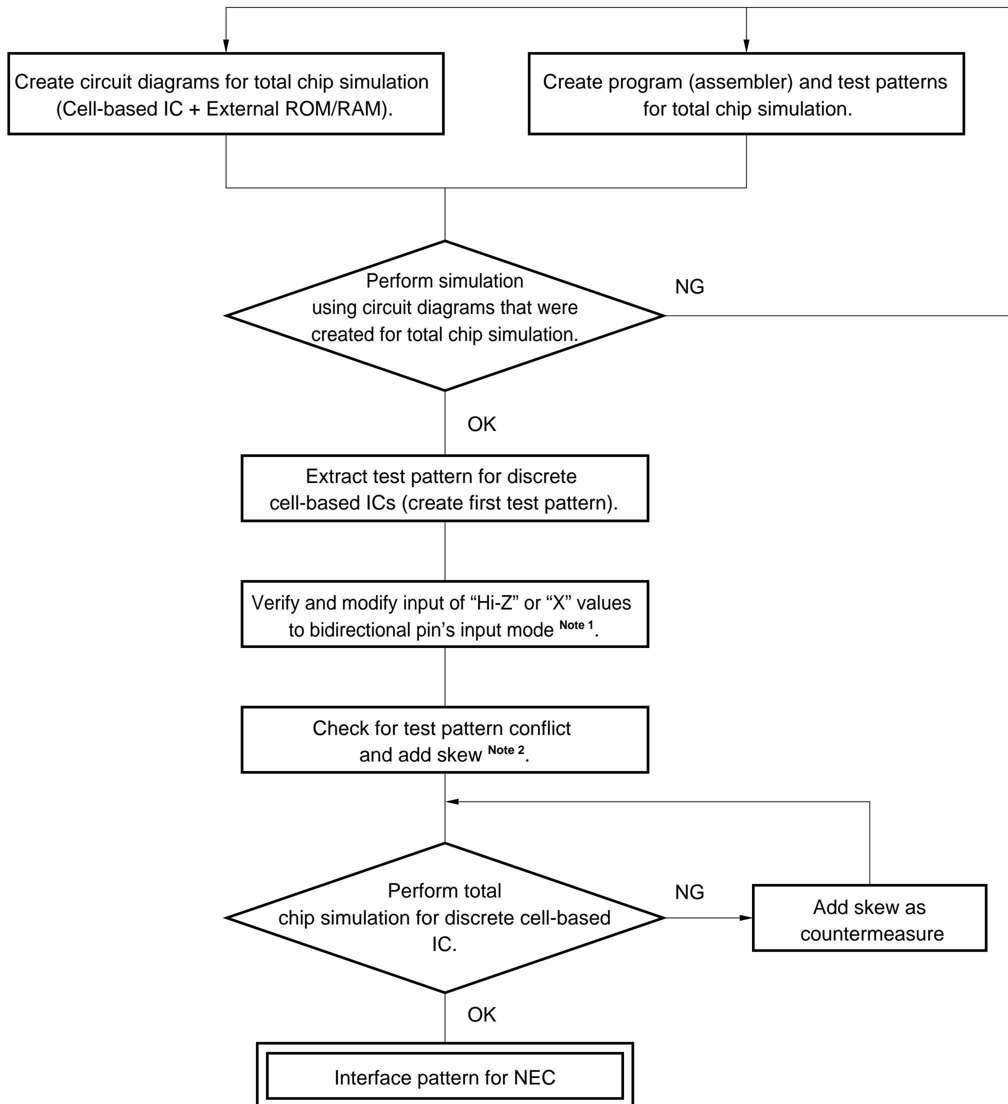
The CPU cores used in this description are the NA70008L, NA71051L, and NA71059L, with circuits whose configurations include a user macro. Note that the circuit in Figure 7-6 was created for description only – its operation has not been verified.

7.2 Total Chip Simulation Flow

Figure 7-1 shows the steps in the total chip simulation flow.

This flow is basically configured of a simple system-level simulation and processes for generating patterns for the tester based on the results of the system-level simulation.

Figure 7-1. Flow of Total Chip Simulation Pattern Generation



Notes 1. Immediately after switching from output mode to input mode, if a "Hi-Z" or "X" status exists, enter the same value ("1" or "0") that appears in the output pattern that is one pattern before the pattern where the output-input mode switch occurred.

2. Note that there are various restrictions related to skew settings.

(1) Create a circuit diagram for total chip simulation

External circuits, such as program ROM and data RAM circuits, are added in order to perform a total chip simulation. For details, see **7.3 Creation of Circuit Diagram for Total Chip Simulation**.

(2) Create a program and test pattern for total chip simulation

A program and test pattern for the CPU core must be created in order to perform a total chip simulation. For details, see **7.4 Creation of Program and Test Pattern for Total Chip Simulation**.

(3) Perform simulation using a total chip simulation circuit

Use an external ROM program to execute the simulation. For details, see **7.5 Execution of Simulation Using Circuit Diagram for Total Chip Simulation**.

(4) Extract a test pattern for a discrete cell-based IC

Dump the initial test pattern for the cell-based IC chip and extract a pattern to be used as the test pattern for a discrete cell-based IC. For details, see **7.6 Extract Test Pattern for Discrete Cell-Based IC**.

(5) Verify and modify input of “Hi-Z” or “X” values to bidirectional pin’s input mode

Check the extracted test pattern to determine whether or not a “Hi-Z” or “X” value has been input when the input pins or bidirectional pins are in input mode, and make any necessary modifications. Depending on the simulator, the extraction of a test pattern may include extraction of pins as output pins, in which case the pin attributes would have to be modified at this point. In such cases, the timing of switching between input mode and output mode on bidirectional pins must be confirmed by checking the results of the total chip simulation of a discrete cell-based IC (described later). For details, see **7.7 Verify and Modify Input of “Hi-Z” or “X” Values to Bidirectional Pin’s Input Mode**.

(6) Check for test pattern conflict and add skew

When a test pattern is extracted for a discrete cell-based IC, the signal input timing is normalized to the basic timing, which means that input conflicts on the test pattern may not operate normally. Therefore, skew is added at this point to avoid test pattern conflict. When selecting the settings and conditions for adding skew, be careful to note how they are reflected in the tester. Also, see **7.8 Check for Test Pattern Conflict and Add Skew**.

(7) Total chip simulation using discrete cell-based IC

Perform a simulation using the test pattern that was modified from the dumped initial test pattern corresponding to the discrete cell-based IC’s circuit diagram to verify the test pattern. For details, see **7.9 Total Chip Simulation Using Discrete Cell-Based IC**.

7.3 Creation of Circuit Diagram for Total Chip Simulation

When performing total chip simulation for a chip that includes a CPU core, software is needed to operate the CPU core.

It is possible to refer to this software while developing a test pattern that is similar to a test pattern used for logic circuits. However, it is very difficult to input the instruction pattern that is needed to align with the read timing from the CPU. Therefore, NEC recommends using the following method instead.

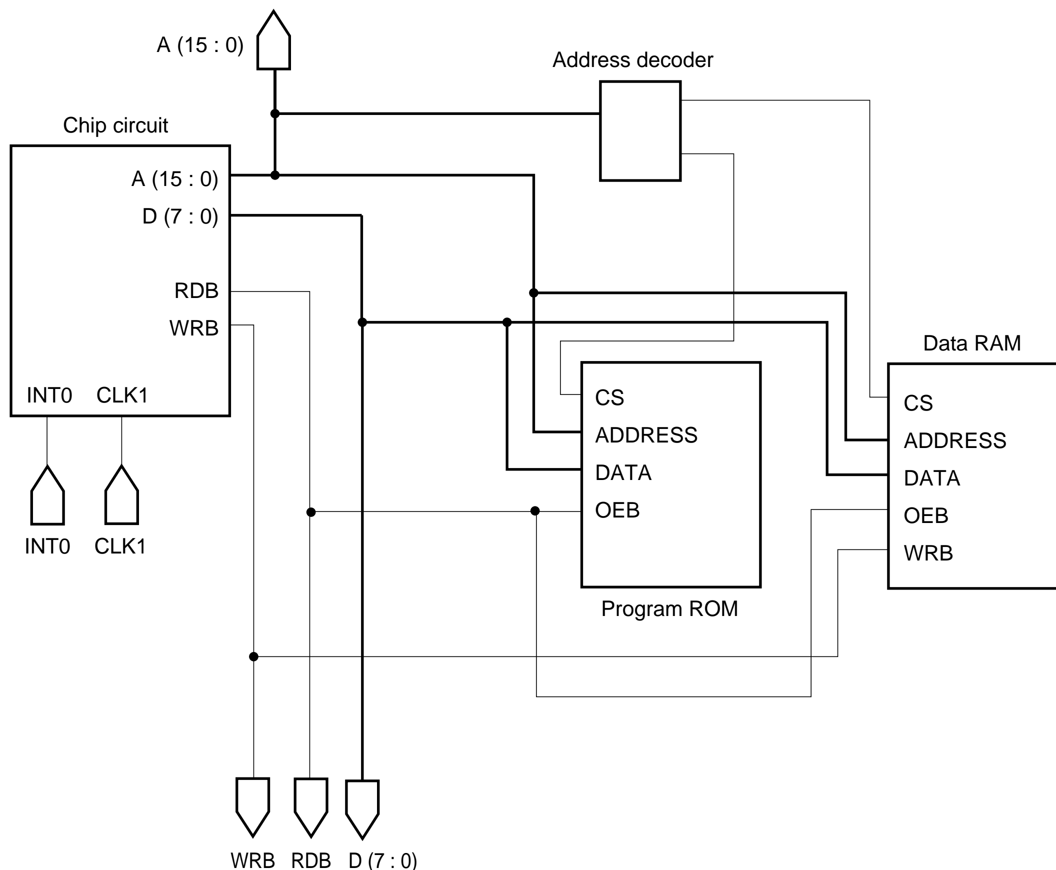
Add a program ROM or data RAM as external to the system circuit, then store the program. Next, execute the simulation and dump the patterns that are at linkage points between the system circuit and external circuits and use the dump results to create a pattern for total chip simulation.

Figure 7-2 shows an abbreviated example of such a circuit configuration. The circuit diagram corresponding to the chip is called the “system circuit diagram”.

Figures 7-3, 7-4, and 7-6 show specific examples of block diagrams for the total chip simulation circuit diagram and the system circuit diagram.

In the example shown in Figure 7-6, NMIs from the CPU control the port and enable input, which reduces the load on the test pattern. Also, READY signals are input when accessing memory.

Figure 7-2. Creation of Circuit Diagram for Total Chip Simulation



Note the following points when creating a circuit diagram for total chip simulation.

(1) Be sure to use macros in the system circuit diagram.
(2) Be sure to place all symbols in the system circuit diagram in the uppermost layer.
(3) Enable the system circuit's CPU core to be accessed by external ROM or RAM.
(4) There is no need to connect external RAM if RAM is not used in the test program for total chip simulation.
(5) All pins corresponding to symbols in the system circuit diagram should be treated as external pins. At this point, all signals that are connected to external ROM/RAM or address lines should be treated as output pins (this may not be necessary for some simulators – contact NEC to check on this).
(6) The only two types of blocks that are currently available for external memory are the SRAM type and the mask ROM type.

7.4 Creation of Program and Test Pattern for Total Chip Simulation

7.4.1 Program and test pattern for total chip simulation

The following test patterns and test programs are required when performing total chip simulation of a system circuit that includes a CPU core.

- **Test pattern (see Figure 7-5)**
  Test pattern data for circuit pins such as the clock input and reset input pins
- **Test program (see the assembler source list example and Figure 7-8 below)**
  The CPU core's assembly language instructions are used to create this software. After the CPU core has been reset by a test pattern, operations begin with reading this program. During the simulation, the assembly language instructions are converted via extended Intel HEX format to a format that the particular simulator can read.

7.4.2 Cautions concerning creation of programs and test patterns for total chip simulation

(1) The test patterns can be confirmed sufficiently merely by confirming the connections between macros. The confirmation of test circuits used for function verification in each macro should be checked using a test circuit simulation of the simple test pattern provided by NEC.
(2) The test program uses interfaces in extended Intel HEX format for various simulators.
(3) Be sure to insert either a program-stopping instruction (such as the HALT instruction for the NA70008L) or an END loop at the end of the test program.
(4) The program size should not exceed 4 Kbytes.
If using a subroutine instruction such as for a CALL statement, this 4-Kbyte limit may be actually exceeded even though the program size is less than 4 Kbytes. Therefore, it is best to basically avoid using subroutine instructions.
(5) The program space to be used for the simulation should be kept within 4 Kbytes.

7.4.3 Test program and test pattern examples

This section presents a test program and test pattern examples used to confirm the connections (interface) between the CPU core (NA70008L) and the various cores and user macros. It is rather difficult to create expected values for output patterns in a total chip simulation performed for verification. Therefore, be sure to enter “X” (Don’t care) for output pins and high impedance for bidirectional pins.

Data containing previously entered expected values is used as the final interface data when the circuit is dumped for dump results to be used in creating test patterns.

Figure 7-3. Block Diagram of Circuit Used for Total Chip Simulation

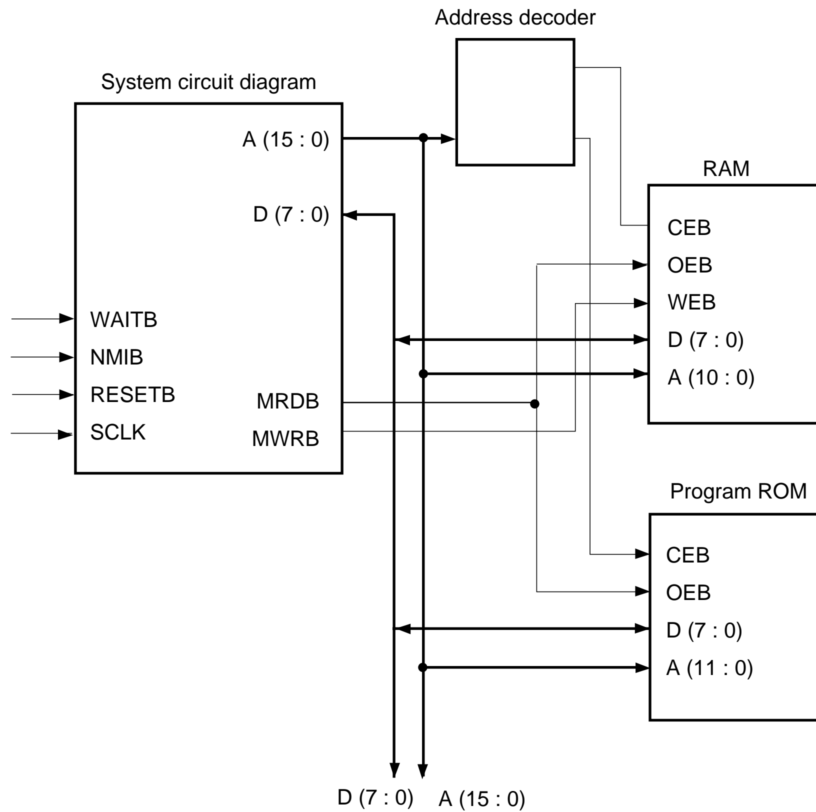


Figure 7-4. Block Diagram of System Circuit

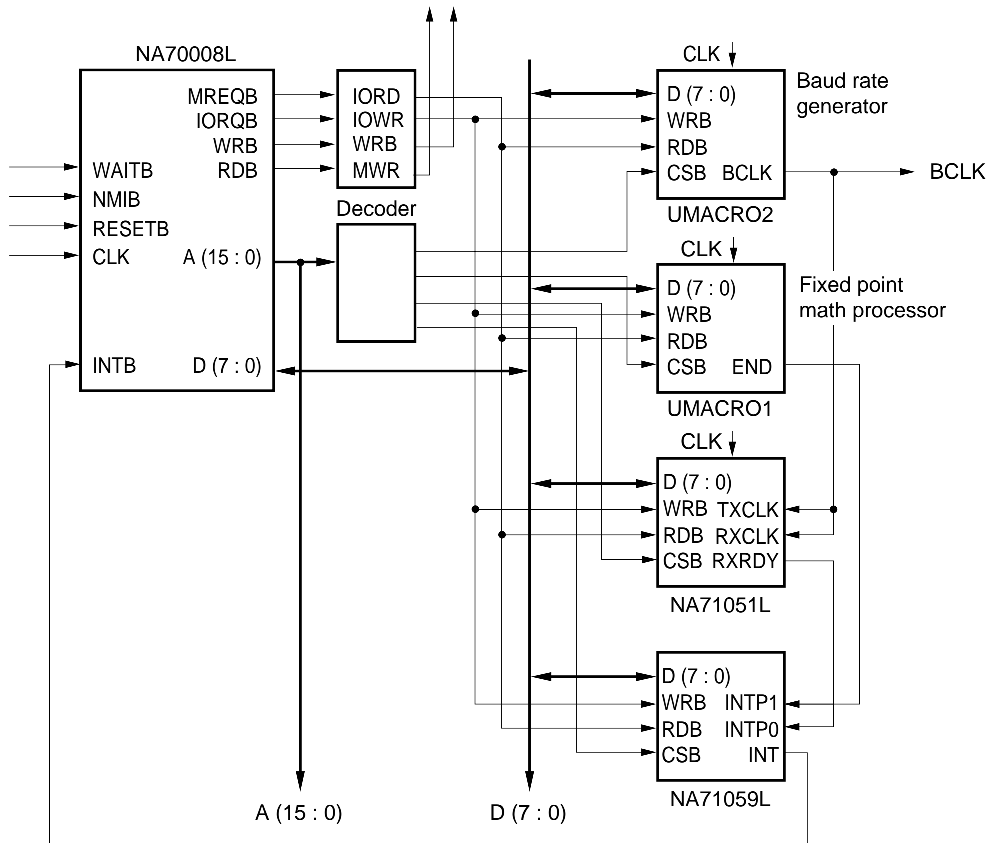
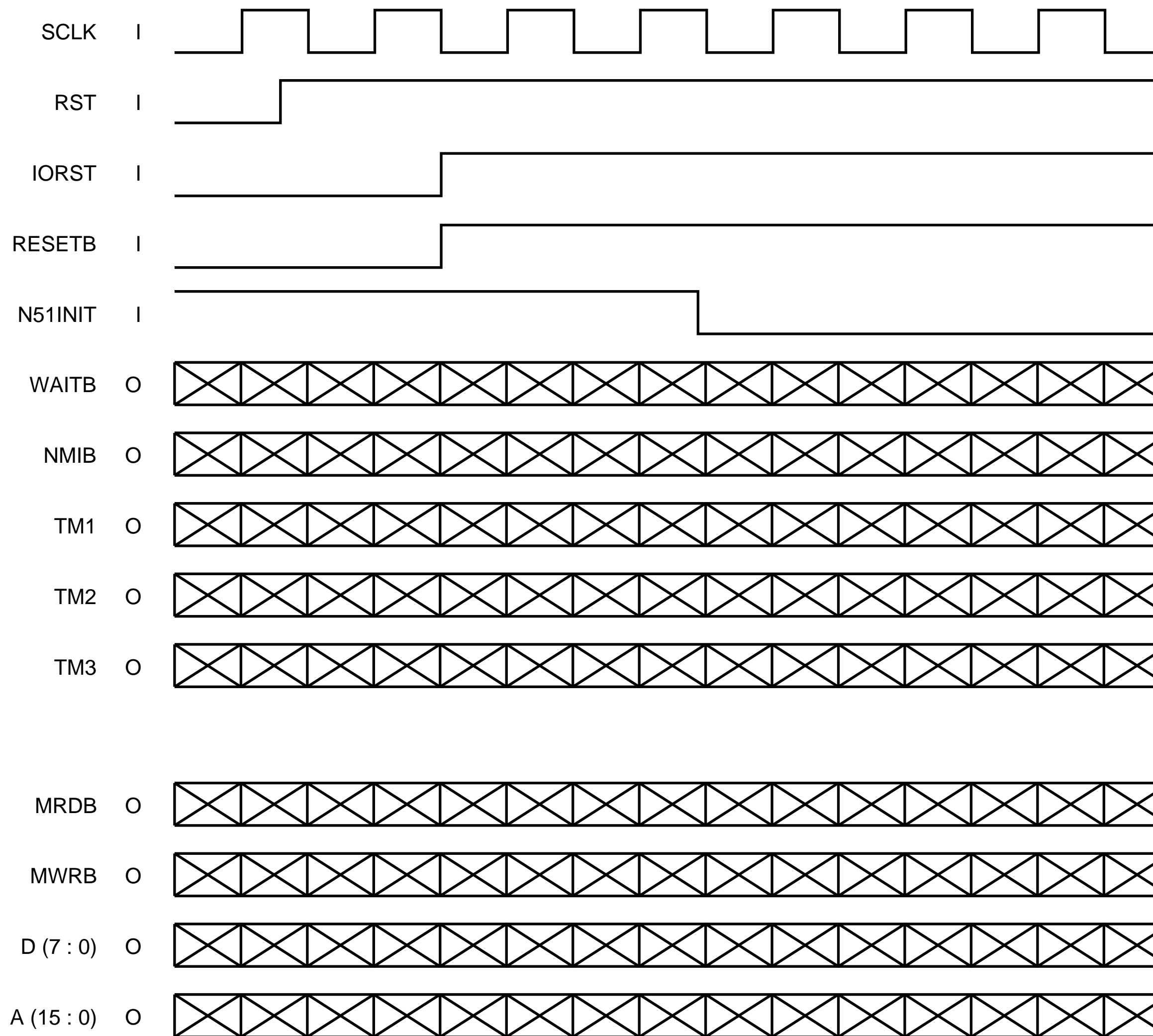


Figure 7-5. Example of Test Pattern for Total Chip Simulation (with External ROM)



The above is an example of a test pattern that corresponds to the total chip simulation circuit diagram shown in Figure 7-6.

In this circuit (shown in Figure 7-6), the test mode selection is made within the circuit and the program enables NMI inputs to be entered via port outputs. The READY signal is entered when accessing memory. Therefore, enter only the required signals in the initial settings, such as for the circuit's system clock (CLK) signal and CPU reset signal (RESETB). Other pins are used as output pins for dumping test patterns.

Be careful to note factors such as the active level and the mode selection conditions when using test patterns to enter signals to the READY, NMI, or mode selection pins.

Figure 7-6. Circuit for Total Chip Simulation (with Added ROM and RAM for Simulation)

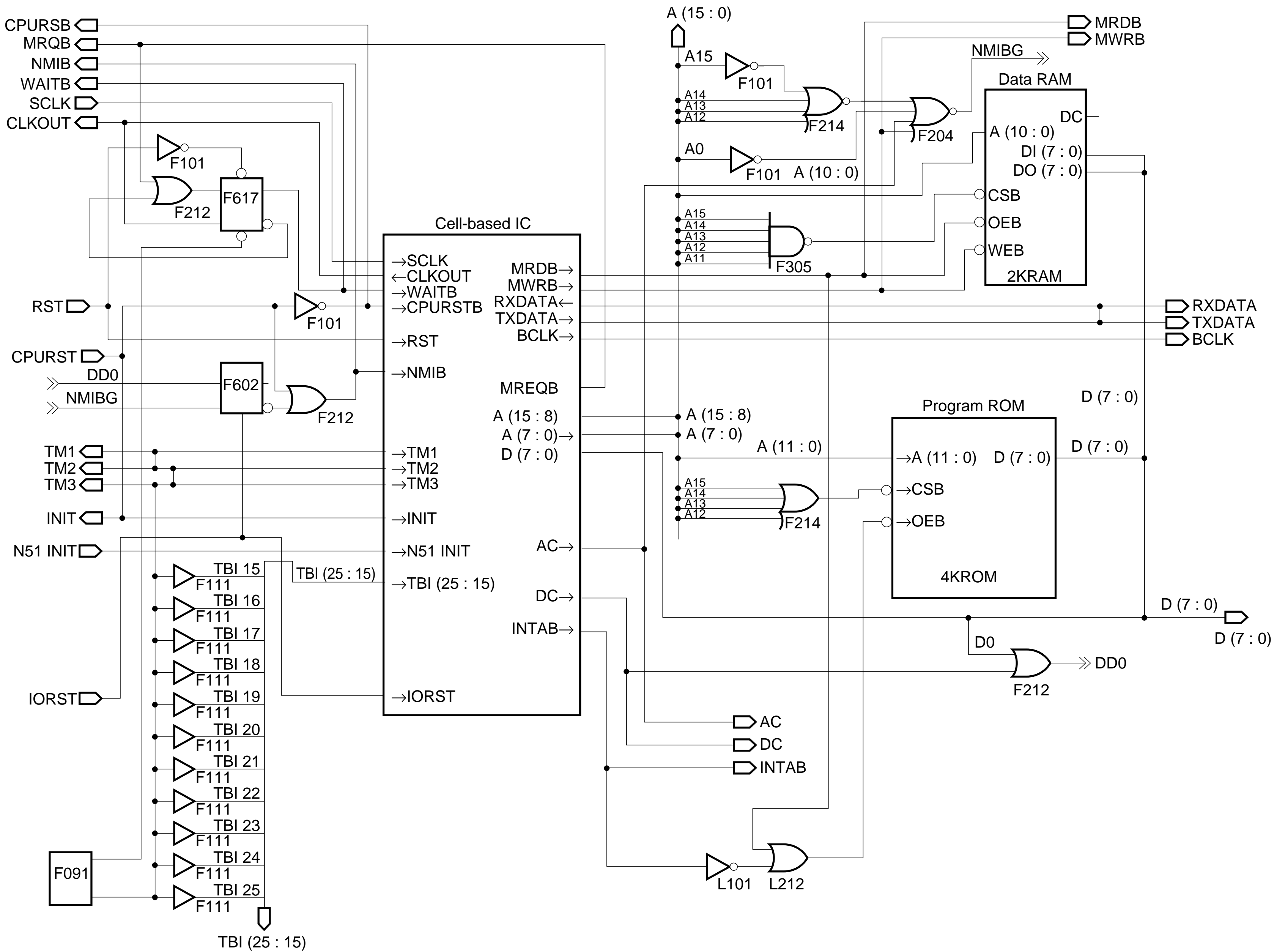
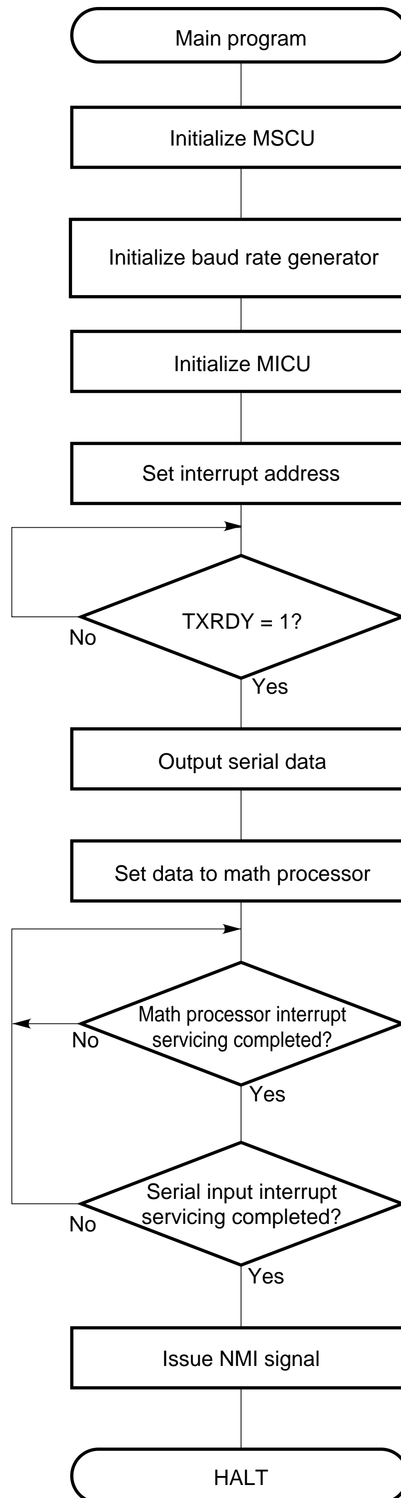


Figure 7-7. Program Flow for Total Chip Simulation



Assembler source list example

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;    System Simulation Demo             ;
;    Create      :1992/12/15            ;
;    update      :1993/03/10*           ;
;          :typing:1993/04/15           ;
;                :1992/06/15**          ;
;                :1992/06/22+           ;
;    CPU         :NA70008L              ;
;    Version     :                      ;
;    Assembler   :AZ80                  ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;    define I/O address                 ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
sCudat      equ   00h                ; MSCU data address**
sCuCom      equ   02h                ; MSCU command address**
;
iCur0 equ   20h                      ; MICU register (A0 = 0)*, **
iCur1 equ   22h                      ; MICU register (A0 = 1)*, **
;
bgCnt equ   60h                      ; Baud rate generator reload  register*, **
bgpre equ   62h                      ; Baud rate generator prescaler*, **
;
CalCmd      equ   40h                ; Fixed point math processor command**
Calap equ   42h                      ; Fixed point math processor  port A**
CalCplequ   42h                      ; Fixed point math processor  port C, low-order byte**
Calbp equ   44h                      ; Fixed point math processor  port B**
CalCPU      equ   44h                ; Fixed point math processor  port C, high-order byte**
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;     Definition of Constant            ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
;;;;;;MSCU initial data;;;;
;
sCudmmy     equ   00000000b          ; MSCU dummy command
sCurstequ   40h                      ; MSCU software reset command
sCumd       equ   01001101b          ; MSCU mode word
sCuCmd      equ   00110111b          ; MSCU command word
;
;;;;;;baud rate generator initial data
;
bpreC equ   000b                     ; Prescaler setting data (1/1)
bCnt  equ   14                       ; Reload register setting data (1/16)
;
```

```
;;;;;;;MICU initial data;;;;;
;
iCuiw1equ   01010010b                   ; MICU IW1 register setting data
iCuiw2equ   00h                         ; MICU IW2 register setting data
iCuimw      equ   11111100b             ; MICU IMW register setting data
iCupfCw     equ   11000111b             ; MICU PPCW register setting data
iCumCw      equ   00001011b             ; MICU MCW register setting data
;
;
;
;;;;;;output data
;
serout equ  0a5h                        ; Serial output data
;
nmion  equ  0ffh                        ; NMI ON setting data
nmioff equ  00h                         ; NMI OFF setting data
;
Cdata  equ  55h                         ; Math processor port A setting data
Cdatb  equ  0aah                        ; Math processor port B setting data
;
;;;;;;;MICU Command
;
fiCmd  equ  00100000b                   ; MICU interrupt end command (FI command)
;
;;;;;;;CalCulator Command
;
addCmd equ  00h                         ; Math processor addition command
;
;;;;;;;CHECK DATA
;
txrdy  equ  00000001b                   ; Data for MSCU TXRDY check
fsCu   equ  00000001b
fCal   equ  00000010b
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;    Program                            ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
       org 0h
start:
       ld     sp,1111111111111111b      ; Stack pointer initialization
       jp inis                          ; Start address setting
;
       org 40h                          ; Address setting for serial input interrupt
       jp intp0
;
       org 48h                          ; Address setting for math processor interrupt
       jp intp1
;
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;      NMI interrupt servicing                  ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
       org 66h
nmi:
       push   af                        ; Save to register
;
       ld     a,nmioff                  ; Release NMI signal
       ld     (8001h),a
;
       halt                             ; Halt
       pop    af
       reti
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;Serial Input Interrupt Servicing               ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
intp0:
       push   af                        ; Save to register
;
       in     a,(sCudat)                ; Serial data input
       ld     (wrtes),a                 ; Store to memory*
       in     a,(sCuCom)                ; MSCU status input
       ld     (wrtes+1),a               ; Store to memory*
       ld     a,(intflag)
       or     fsCu
       ld     (intflag),a
       ld     a,fiCmd
       out    (iCur0),a
       pop    af
       reti
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;Address Setting for Math Processor Interrupts           ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
intp1:
       push   af                        ; Save to register
;
       in     a,(CalCpl)                ; Serial data input
       ld     (wrtes+2),a               ; Store to memory*
       in     a,(CalCPU)                ; MSCU status input
       ld     (wrtes+3),a               ; Store to memory*
       ld     a,(intflag)
       or     fCal
       ld     (intflag),a
       ld     a,fiCmd
       out    (iCur0),a
       pop    af
       reti
```

```
;
inis:
        di                                  ; Interrupt disabled
;
;Baud Rate Generator Initialization+
        ld      a,bCnt                      ; Reload register setting (1/15)
        out     (bgCnt),a                   ; *
        ld      a,bpreC                     ; Prescaler setting (1/1)
        out     (bgpre),a
;
;
;MSCU Initialization
        ld      a,sCudmmy                   ; Dummy command
        out     (sCuCom),a                  ; Initial output of dummy command
        nop
        nop
        nop
        nop
        nop
        out     (sCuCom),a                  ; Second output of dummy command
        nop
        nop
        nop
        nop
        nop
        out     (sCuCom),a                  ; Third output of dummy command
        nop
        nop
        nop
        nop
        nop
        ld      a,sCurst                    ; Software reset command
        out     (sCuCom),a
        nop                                 ; wait >= 3 + 4 + 4
        nop
        ld      a,sCumd                     ;
        out     (sCuCom),a                  ; Mode word setting
        nop
        nop
        ld      a,sCuCmd                    ;
        out     (sCuCom),a                  ; Command word setting
;
```

```
;MICU Initialization
        ld      a,iCuiw1                    ; IW1 initialization data
        out     (iCur0),a                   ; IW1 initialization data output
        ld      a,iCuiw2                    ; IW2 initialization data
        out     (iCur1),a
        ld      a,iCuimw                    ; IMW initialization data
        out     (iCur1),a
        ld      a,iCupfCw                   ; PPCW initialization data
        out     (iCur0),a
        ld      a,iCumCw                    ; MCW initialization data
        out     (iCur0),a
;
        ld      a,0
        ld      (intflag),a                 ; Zero-clear flag area
;
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;       main program                     ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        ei                                  ; Interrupt enabled
;
        im      0                           ;
wittrdy:
        in      a,(sCuCom)                  ; Read MSCU status
        bit     0,a                         ; Does TXRDY = 1?
        jr      z,wittrdy                   ; Wait until TXRDY = 1
;
        ld      a,serout                    ; Serial data setting
        out     (sCudat),a                  ; Serial data output
;
        ld      a,Cdata
        out     (Calap),a                   ; Math processor port A setting
        ld      a,Cdatb
        out     (Calbp),a                   ; Math processor port B setting
        ld      a,addCmd
        out     (CalCmd),a                  ; Addition command output
;
        ei                                  ; Interrupt enabled
wtint:
        ld      a,(intflag)                 ; Read flag area
        bit     1,a                         ; Math processor interrupt completed?
        jr      z,wtint
        bit     0,a                         ; Serial input/output interrupt completed?
        jr      z,wtint
;
        ld      a,nmion                     ; NMI ON*
        ld      (8001h),a                   ;
;
endlp:
         jp     endlp
;
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;       RAM area definition              ;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
       org   1111111000000000b
wrtes  defs  10                        ; Memory read/write test area*
 intflag     defs 1                    ; Flag area
;
       end   start
```

7.5 Execution of Simulation Using Circuit Diagram for Total Chip Simulation

Since it is difficult to create expected values for total chip simulation that includes cores (except for memory), such simulations are performed using an input test pattern and test program.

After completing the creation of the total chip circuit diagram, test pattern, and test program, execute the total chip simulation. Be sure to send the ROM code to the program ROM.

To check operation when the chip includes a CPU, dump the CPU's address output or check the program ROM's addresses and verify them by comparing them to the assembler program list.

7.6 Extract Test Pattern for Discrete Cell-Based IC

The extraction method differs according to the type of simulator to be used.

If using a Verilog™-type simulator, check the cell-based IC's initial interface block and set the simulator to automatically dump a test pattern to extract it. Perform the simulation using the total chip simulation circuit diagram.

If using a V.sim simulator, before starting the total chip simulation make sure that all of the cell-based IC chip's signals (all symbol signals in the system circuit diagram) are set as external output pins, as was mentioned in **7.3 Creation of Circuit Diagram for Total Chip Simulation** above. This means that the test pattern extracted from the dump output will include only output pins, so that the pin attributes can be modified at the next process.

7.7 Verify and Modify Input of "Hi-Z" or "X" Values to Bidirectional Pin's Input Mode

In some cases, the extracted test pattern will include input "Hi-Z" or "X" inputs. While this can be avoided via an external circuit configuration, it is best to check these inputs and replace any "Hi-Z" or "X" input to an input pin or a bidirectional pin in input mode with a "1" or "0" input.

When using a V.sim-type simulator, the attributes of the extracted test pattern should be aligned with the attributes (including names) of the cell-based IC chip's various pins. When doing this, first set bidirectional pin attributes as input pin attributes (to set the test pattern to input mode) before changing them to bidirectional pin attributes.

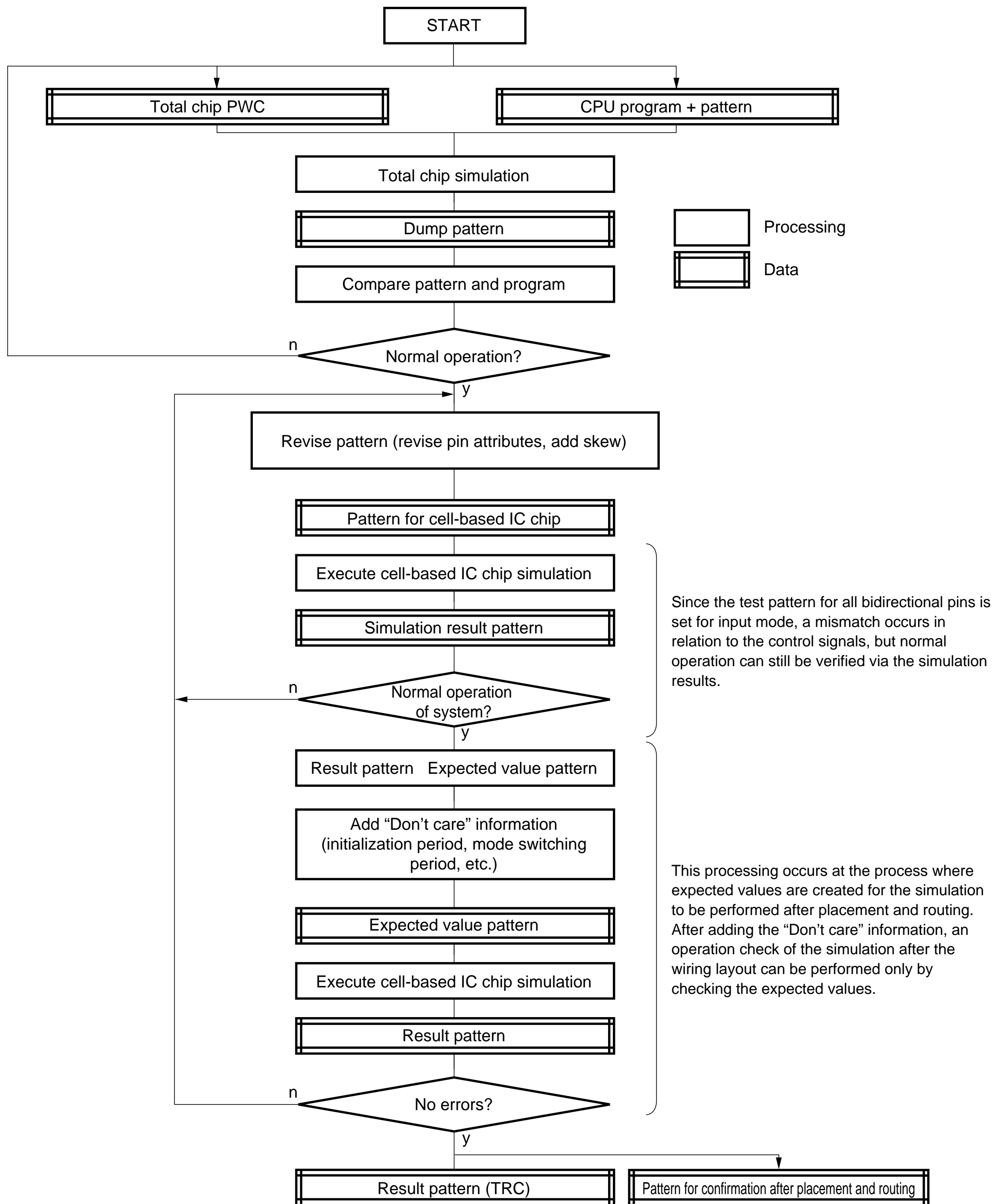
7.8 Check for Test Pattern Conflict and Add Skew

When the test pattern is extracted, the signal input timing is normalized to the basic timing (no delays), which may reduce the previously required skew. At this point, add skew as needed in consideration of the timing of the various input signals. Note that the tester may provide only limited support for added skew. In some cases, addition of skew is required mainly for the data bus.

7.9 Total Chip Simulation Using Discrete Cell-Based IC

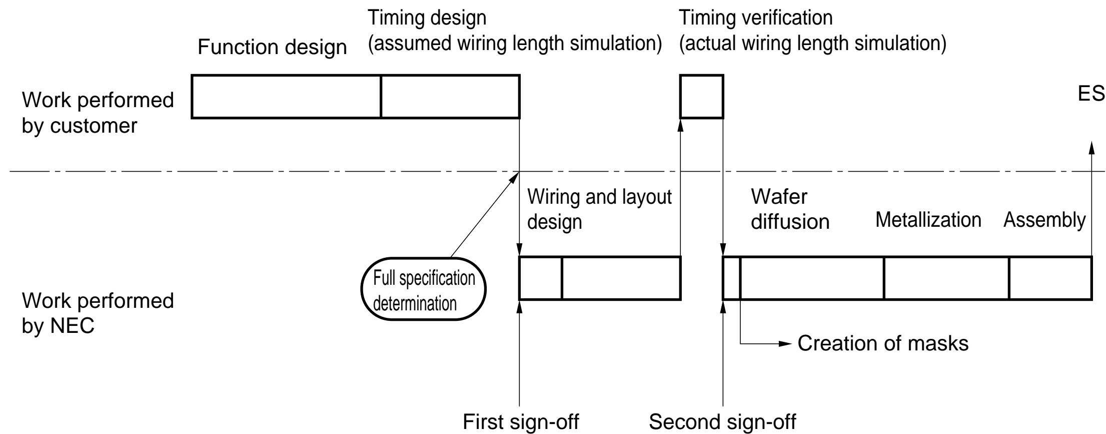
When using a test pattern that has been extracted from a dump and then revised, perform the simulation for the cell-based IC's chip circuit rather than for the circuit diagram used for total chip simulation. Check for normal operation of the simulation.

Figure 7-8. Example of Execution Steps When Using OPENCAD (Using V.sim™)



CHAPTER 8 SIGN-OFF CONDITIONS AND DATA TO BE PASSED

Sign-off conditions are the conditions for accepting design data that is submitted to NEC after verification has been done via simulations. After the assumed wiring length delay simulation is completed, there is a first sign-off that comes immediately before wiring layout. After the actual wiring length simulation is completed, there is a second sign-off that comes immediately before creation of masks. The design data that is submitted for the first sign-off is called the CF1 (clean file 1) data and the design data for the second sign-off is called the CF2 (clean file 2) data.



8.1 Basic Conditions for Sign-offs

The basic conditions for sign-offs are explained below.

[First sign-off]

(1) Make sure there are no critical errors in the design rule check program (except for pseudo errors, such as an all output operation error used when a dummy gate is implemented, which have already been confirmed as OK).

(2) Make sure that a netlist and test patterns have been prepared and checked the next item via a assumed wiring length delay simulation using the sign-off simulator.

<1> Make sure there were no mismatches with expected values or timing errors during simulations using maximum and minimum conditions (except for pseudo errors that have been confirmed as OK via actual operations and tests).

- Test patterns to be submitted to NEC should be prepared using a cycle period (rate) of 200 ns if possible without causing problems. Also, verification should also be done via simulation using actual operation conditions.

[Check items]

- Function check
- Setup/hold time check
- Release/removal time check
- Minimum pulse width check
- Bus conflict/bus float check

(3) If any cores have been implemented, perform a separate simulation for the cores and make sure there are no mismatches. If a RAM macro has been implemented, check access while in separate test mode to make sure there are no problems in the test circuit.

[Second sign-off]

(1) Check for the following items when performing an actual wiring length simulation using the sign-off simulator.

<1> Make sure that there were no mismatches with expected values or timing errors during the simulations using maximum and minimum conditions (except for pseudo errors that have been confirmed as OK via actual operations and tests).

- Also, be sure to perform simulations using actual operation conditions to confirm the test patterns to be submitted to NEC.

<2> When there is a critical path, confirm that the required values are met.

8.2 Data Required for Interface

(1) Data submitted for first sign-off

<1> Netlist that meets the conditions for the first sign-off
[Format]

- PWC [Note] or EDIF

<2> Design rule check confirmation results (LOG file)
<3> Test patterns that meet conditions for sign-off
[Format]
Use the following combination.

Test pattern	Timing data
NELPAT [Note]	Timing ALBATROSS file

Note This is NEC's original format.

[Test pattern types]

The following data from simulation under maximum conditions

- Test patterns for separate test verification of user macro
- Total chip simulation patterns (chip level)
- Test patterns for confirming ROM code (when ROM macro has been implemented)
- Test patterns for separate test verification of cores (when a core has been implemented)
- Access patterns for verification of separate RAM macro (when RAM macro has been implemented) Related register files

Remark Be sure to prepare either one test pattern for separate test verification of user macro or one test pattern for total chip simulation as a test pattern that meets the DC test conditions.

<4> ROM code data and support data for code and macro (when a ROM macro has been implemented)

[Format]

- NINCF [Note] or Verilog format (HEX display)

[Support information]

- ROM block name, instance name (such as CS00 **** for PWC format), ROM code file name, and ROM code header name

Note This is NEC's original format.

<5> Assumed wiring length simulation LOG file

- LOG file contains simulation results for various test patterns under maximum and minimum conditions (logging of execution under maximum conditions only is accepted for separate simulations of core and memory macro blocks, as long as there are no “Delay Over Period” errors).

<6> Other data

- Checklist for CB-9 (contains items up until completion of CF1)
- Cell-based IC product requirement specifications
  Main contents: Pin assignment table, core test mode settings and support data for test mode.
- Critical path instructions (only if required)
- Glitch/noise troubleshooting instructions (only if required)
- Simulation result confirmation instructions (before placement and routing)
- Results of investigation into special requirements (only if required)

(2) Data submitted for second sign-off

<1> LOG files of actual wiring length simulations

[Types]

- LOG file contains simulation results for various test patterns under maximum and minimum conditions (must conform to cycle periods of test patterns submitted to NEC).

<2> Other data

- Simulation result confirmation instructions (after placement and routing)
- Product requirement specifications (only if revisions were made after first sign-off)
- Check list (contains items up until completion of CF2)
- Critical path instructions (only if required)
- Glitch/noise troubleshooting instructions (only if required)
- Results of investigation into special requirements (only if additional investigation was done after first sign-off)

CHAPTER 9 MULTI-FUNCTION BLOCKS

In addition to ordinary function blocks, CB-9 Family VX/VM type devices can use the following types of multi-function blocks. The functions and usage of these multi-function blocks are described below.

- 3.3-V, 5-V interface blocks
- Buffers with on-chip pull-up/pull-down resistors
- GTL (under development)
- Scan path test block

9.1 3.3-V, 5-V Interface Blocks

The following interface blocks are available for CB-9 Family VX/VM type devices.
The features of these blocks are described below. For a list of the blocks' names, see Block Library.

Input blocks
- LVTTL input buffer
- LVTTL input buffer (with fail-safe function)
- 5-V input buffer (VM type only)

Output blocks
- LVTTL output buffer
- TTL 5-V tolerant output buffer
- 5-V output buffer (VM type only)

The block connections are described below.

9.1.1 Input buffers

3.3-V input buffers are used to receive 3.3-V signals and cannot be used to receive 5-V signals. 5-V signals are received by TTL 5-V tolerant input buffers or 5-V input buffers (VM type only). The TTL 5-V tolerant buffers are designed to accommodate the trend toward a 3.3-V power supply on cell-based IC peripheral circuits and therefore are also able to receive 3.3-V signals. Note that this is why the input characteristics V_{IL} and V_{IH} are rated for LVTTL.

In conventional cell-based ICs, it is not possible to apply an input voltage that is higher than the V_{DD} voltage, so it is not possible to apply an input voltage when the cell-based IC's power supply is off. The LVTTL input buffer with the fail-safe function is the exception in that it is able to receive an applied input voltage even when the cell-based IC's power supply is off. In ordinary input buffers, if the cell-based IC's power supply is off, input of a high-level signal causes voltage to be applied to the power supply line via a protective diode (see Figure 9-2). For the LVTTL input buffer with the fail-safe function, input of a high-level signal when the cell-based IC's power supply is off does not apply voltage to the power supply line. Consequently, as long as the device's electrostatic voltage resistance is adequate, it can also be used for hot-line work.

Figure 9-1. Equivalent Circuit Diagrams of 3.3-V and 5-V Input Buffers

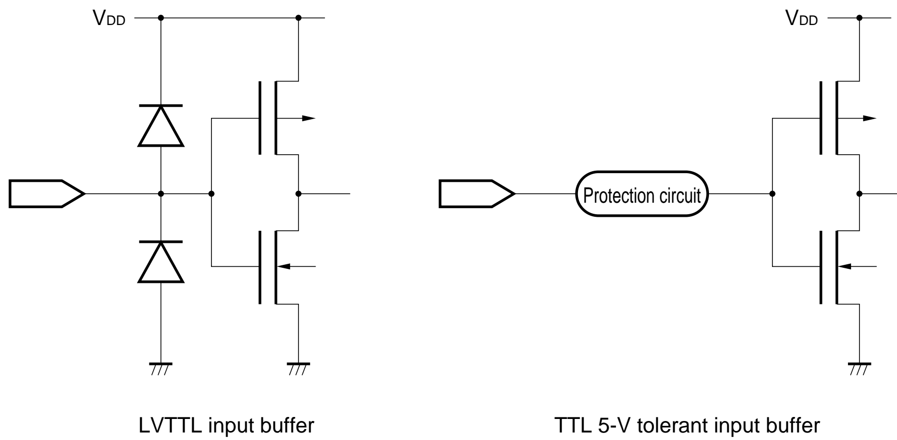
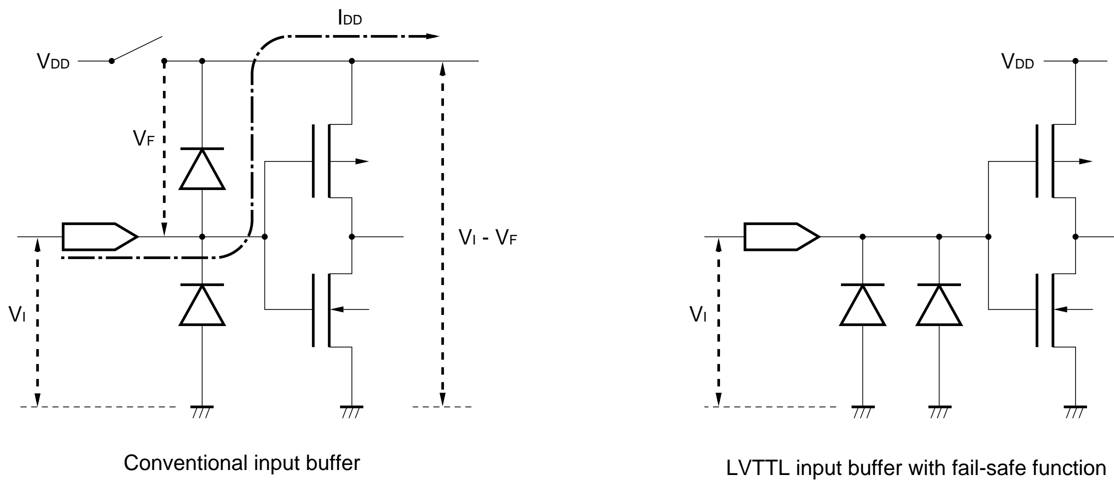
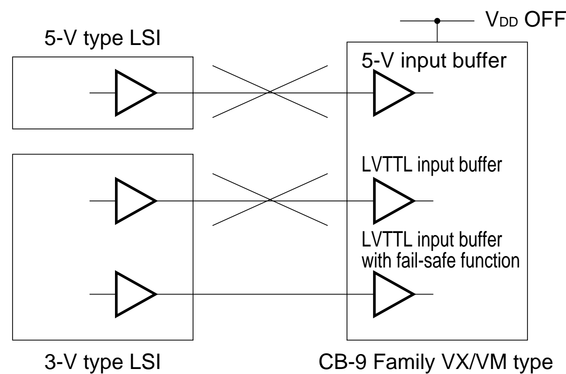


Figure 9-2. Equivalent Circuit Diagrams and Connection Example of 3.3-V Input Buffer with Fail-safe Function

(a) Equivalent circuits



(b) Connection example of 3-V input buffer with fail-safe function



9.1.2 Output buffers

The following two types of 5-V output buffers are provided for CB-9 Family VX/VM type devices. Unlike previous output buffers, the 5-V output blocks enable a high-voltage (5 V) pull-up from a cell-based IC power supply.

<1> TTL 5-V tolerant output buffer

This buffer is used when a subsequent LSI uses 5-V TTL logic. While a 3.3-V output buffer would suffice for the output level, the 5-V output buffer includes a 5-V protection circuit for when connection to a 5-V line is necessary. This buffer can also use a 5-V pull-up. Removing the external pull-up resistor is all that is needed if the LSI with the output load is changed from a LSI with a 5-V power supply to one with a 3-V power supply. This 5-V output buffer will be especially useful in the future, as the power supply voltage used to drive cell-based ICs is changed from 5 V to 3 V. However, with TTL-level 5-V output buffers, a certain amount of current flows to the cell-based IC when a 5-V pull-up is used. Consequently, there may be cases where the pull-up resistance value prevents the output signal from reaching 5 V (see **4.1.2 Output leakage current (I_R)**).

As for three-state buffers and bidirectional buffers, when the three-state circuit is in the off state, there is a slight increase in the off-state current due to the bias voltage of the protection circuit for 5-V voltage.

Note with caution that this buffer cannot be placed next to a 5-V V_{DD} pin or a 5-V full swing buffer.

<2> 5-V output buffer (VM type only)

There are two types: CMOS-level 5-V output buffer and TTL-level output buffer. These two types can be connected to corresponding 5-V TTL-level or 5-V CMOS-level LSIs.

These buffers can only be used with VM type devices. When 5-V power is applied to an LSI, 5-V full swing output is enabled.

Figure 9-3. Equivalent Circuit Diagrams of Output Buffers

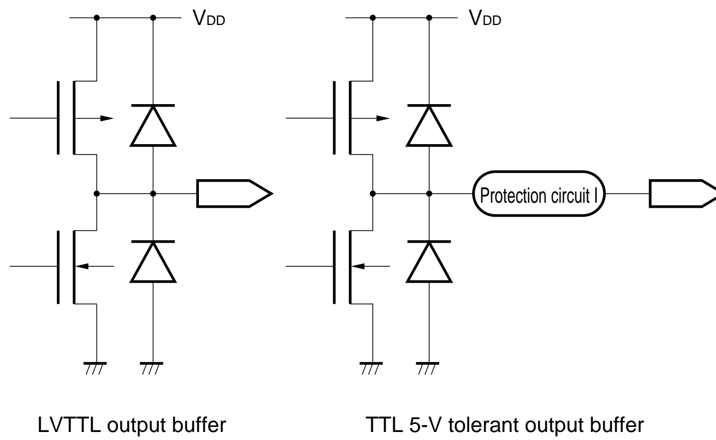
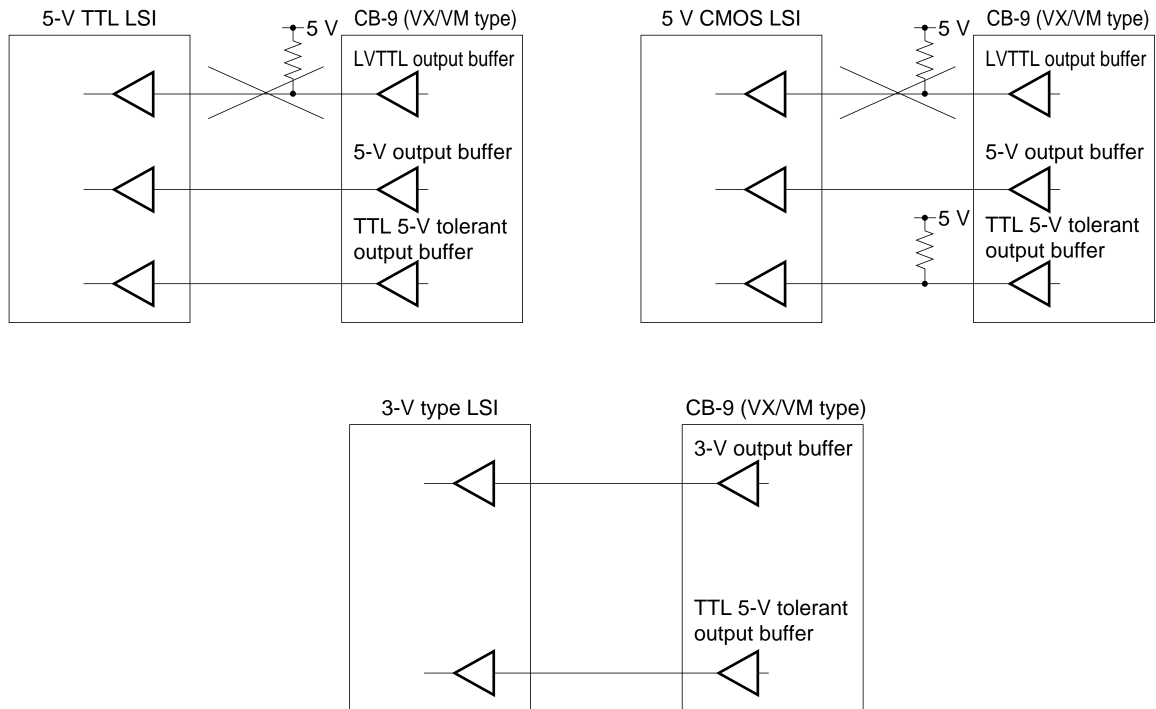


Figure 9-4. Connection Examples of TTL 5-V Tolerant Output Buffer and 5-V Output Buffer

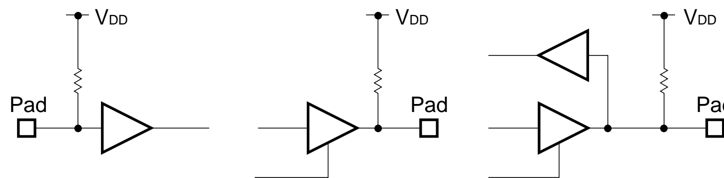


9.2 Input/Output/Bidirectional Buffers with On-Chip Pull-up/Pull-down Resistors

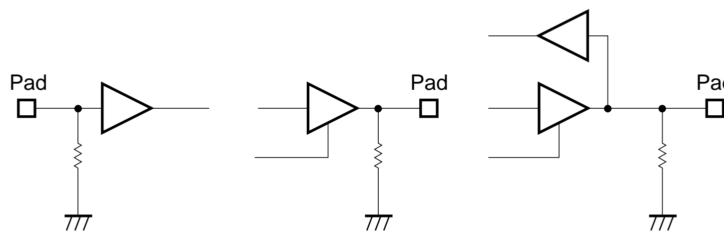
The blocks available for CB-9 Family VX/VM type devices include input buffers, Schmitt input buffers, three-state output buffers, N-ch open drain output buffers, bidirectional buffers, Schmitt input bidirectional buffers, and I/O blocks with on-chip pull-up/pull-down resistors. These blocks can be used to design a more compact system.

The names of these blocks are listed in Block Library.

Pull-up resistors



Pull-down resistors



During simulations, it is not possible to input an undefined (X) or high-impedance (Z) signal to the input pin of an input buffer with on-chip pull-up/pull-down resistors or a bidirectional buffer.

Use high impedance (Z) or Don't care (X) as the expected output value when the output pin of a three-state output buffer with on-chip pull-up/pull-down resistor or a bidirectional buffer is not active.

9.3 Oscillator Block

9.3.1 Overview of oscillator block

The following six blocks are available to be used as the oscillator block. Select the block that best suits the required frequency, based on the recommended oscillation ranges listed in Table 9-1.

Table 9-1. Recommended Oscillation Frequency Ranges for Oscillator Blocks

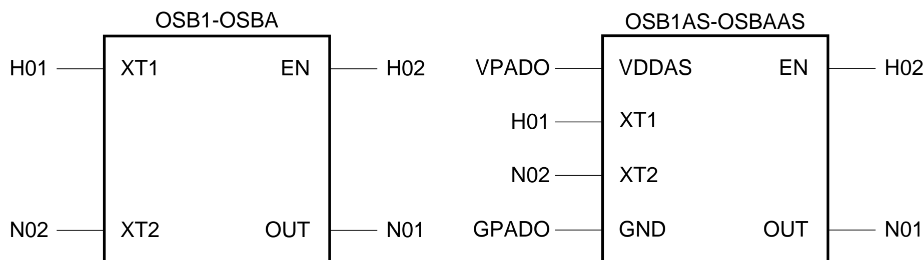
Oscillator Block	Recommended Oscillation Frequency			Unit
	MIN.	TYP.	MAX.	
OSB1, OSB1AS Note		32		kHz
OSB3, OSB3AS Note		4		MHz
OSB4, OSB4AS Note		8		MHz
OSB5, OSB5AS Note		16		MHz
OSB6, OSB6AS Note		32		MHz
OSB7, OSB7AS Note		40		MHz
OSB9, OSB9AS Note		50		MHz
OSBA, OSBAAS Note		64		MHz

Note AS: Indicates that oscillation block includes a 3.3-V/2-V level shifter.

Remark The minimum and maximum values and use conditions are still under evaluation.
A block with external circuits for L and C is required if using a resonator that has tertiary overtones at or above 24 MHz.

Oscillator block symbols and pin functions are shown below.

- **Oscillator block symbols**



- **Operation truth table (for OSB1 to OSB7 and OSB1AS to OSB7AS)**

H01 (XT1)	H02 (EN)	N01 (OUT)	N02 (XT2)
0	1	0	1
1	1	1	0
0	0	0	1
1	0	0	X

Remark X: Prohibited

- **Pin functions**

Pin Name	Function Name	Description of Function
H01	XT1	This is an external input pin. It is connected to an external resonator. When in external clock input mode, an external clock is input via this pin.
N02	XT2	This is an external output pin. It is connected to another external resonator. When in external clock input mode, this pin is left open.
H02	EN	This is the oscillation enable pin. Oscillation is started when this pin is at high level and is stopped when this pin is at low level.
N01	OUT	This is an internal clock signal output pin. It has the same phase as H01 (except for prohibit status).

Remark Contact NEC if external clock input is desired for an oscillator block. In such cases, do not use stop control for oscillator blocks. Also, leave the output pins open.

9.3.2 Cautions on use of oscillator blocks

Note the following points when using oscillator blocks.

(1) If not using stop control, be sure to clamp the stop control signal (EN = 1) to enable actual operation mode.
(2) If using stop control, be sure that stop mode is set in user-generated patterns.
(3) To set stop mode (EN = 0) during a simulation, be sure to apply low-level signals to the external input (XT1) and set a high-level expected value for the external output (XT2).
(4) When performing stop control of the oscillator block via a core, check the corresponding active levels to make sure there are no errors.
(5) Contact NEC if several oscillator blocks are to be implemented.
(6) Designs must take into account the oscillation stabilization period after a stop release.
(7) Place power supply pins on both sides of the oscillator pin (see **2.4 Pin Layout**).
(8) Inserting an in-series limiting resistor on the output (XT2) side is an effective way to reduce unnecessary radiant noise. If using OSB3 to OSBA, be sure to use a low-gain oscillator block as a countermeasure against radiant noise.

9.3.3 Cautions on oscillator configuration

The CB-9 Family's VX/VM types are provided with an on-chip dedicated oscillation block that can be used to configure an oscillator by connecting a resonator and an external constant outside the package. Although this presents the advantage of allowing easy configuration of an oscillator, the oscillator is an analog circuit that operates on a high frequency, so that cautions differing from those for logic circuits apply.

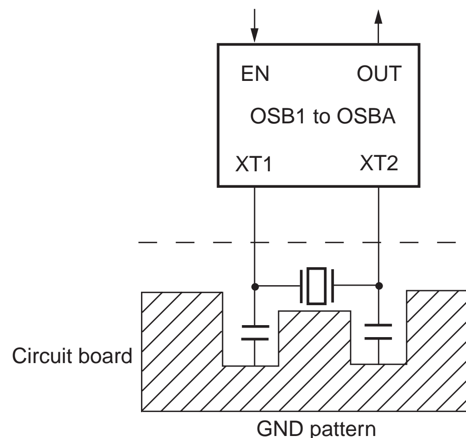
To obtain a stable oscillation, in addition to optimizing the external constant (capacitor on input side, capacitor on output side, and limiting resistor), it is necessary to handle the circuit as an analog circuit, which requires attention to the following three cautions.

<1> Place the oscillator close to the power supply of the cell-based IC.

<2> Place the oscillator as far as possible from high-frequency input pins such as the CLK pin.

<3> Attention to the following cautions regarding the printed circuit board is required.

- Place the input and output pins of the oscillator and the resonator and external constant close to each other, and keep wiring as short as possible.
- Make the wiring between the ground side of the capacitor and the ground pin of the cell-based IC as short and as thick as possible.
- Keep the lead wire of the resonator and capacitor as short as possible, and fix the resonator and capacitor to the printed circuit board to keep the influence of mechanical vibrations to a minimum.
- Lay out the external constant portion so that it is surrounded by GND insofar as possible.



Further, attention to the following cautions regarding evaluation for determining the external constant is required.

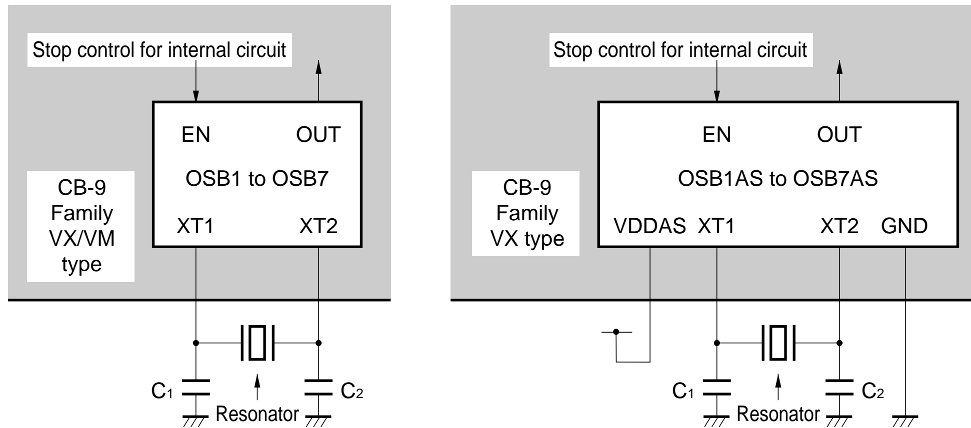
- Use the printed circuit board that will actually be used. (The oscillation operation range may vary depending on the dielectric constant of the circuit board.)
- Perform verification using the developed cell-based IC and the resonator that will actually be used.

9.3.4 Oscillator block configuration examples

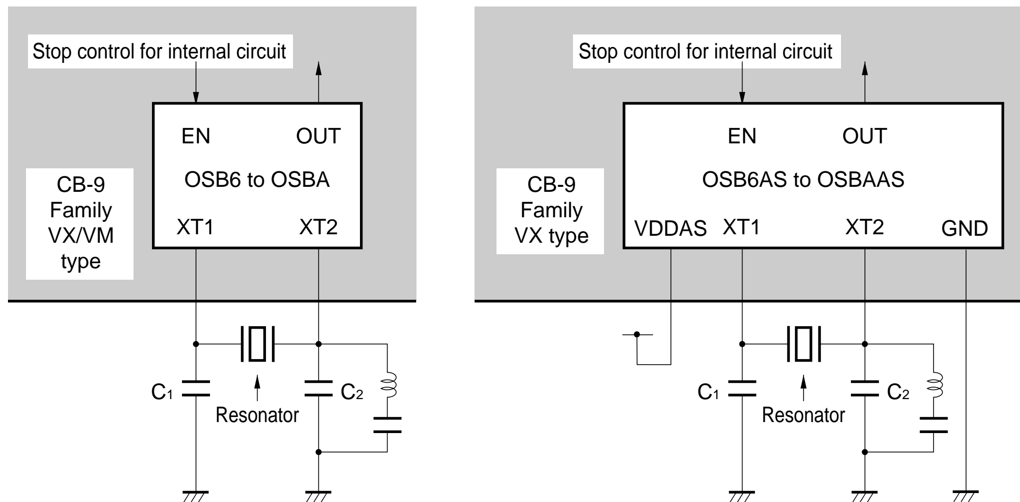
Figure 9-5 shows examples of oscillator block configurations.

Figure 9-5. Oscillator Block Configuration Examples

(a) For 32-kHz to 24-MHz oscillation (fundamental frequency)



(b) Oscillation with overtones at or above 24 MHz



9.3.5 Resonator and circuit configuration

The following table and figure show examples of the resonator and external constant to be connected externally, as well as sample circuit configurations. This data was evaluated with the cooperation of the manufacturer of each resonator.

Table 9-2. Ceramic Resonator Evaluation List

Material	Resonator Manufacturer	Frequency (MHz)	Part Number	Oscillation Block Name	Capacitor	Recommended External Constant				Circuit
						C_{in} (pF)	C_{out} (pF)	R_d (Ω)	R_f (Ω)	
Ceramic	Murata Mfg. Corporation	1	CSB1000J	OSB3	Connected externally	100	100	–	–	<2>
		2	CSA2.00MG			30	30	–	–	
			CST2.00MG		On-chip	(30)	(30)	–	–	<1>
		4	CSA4.00MGU		Connected externally	30	30	–	–	<2>
			CST4.00MGWU		On-chip	(30)	(30)	–	–	<1>
		8	CSA8.00MTZ093		Connected externally	30	30	–	–	<2>
			CST8.00MTW093		On-chip	(30)	(30)	–	–	<1>
		12	CSA12.0MTZ CSA12.0MTZ093	OSB4	Connected externally	30	30	–	–	<2>
			CST12.0MTW CST12.0MTW093		On-chip	(30)	(30)	–	–	<1>
		16	CSA16.00MXZ040	OSB5	Connected externally	5	5	–	–	<2>
			CST16.00MXW0C1		On-chip	(5)	(5)	–	–	<1>
		20	CSA20.00MXZ040	OSB6	Connected externally	3	3	–	–	<2>
		25	CSA25.00MXZ040	OSB7		3	3	–	–	
		32	CSA32.00MXZ040			–	3	–	8.2 k	<4>
		40	CSA40.00MXZ040	OSB9		–	3	–	6.8 k	
		50	CSA50.00MXZ040	OSBA		–	–	–	5.6 k	
	TDK Corp.	28	CCR28.0MSC6	OSB6	Connected externally	–	–	10	–	<2>

Remark Oscillation environment V_{DD} = 3.3 ± 0.3 V, T_A = –40 to +85°C
Since the oscillation status varies depending on the circuit board pattern, also perform evaluation on the actual board using the developed cell-based IC.

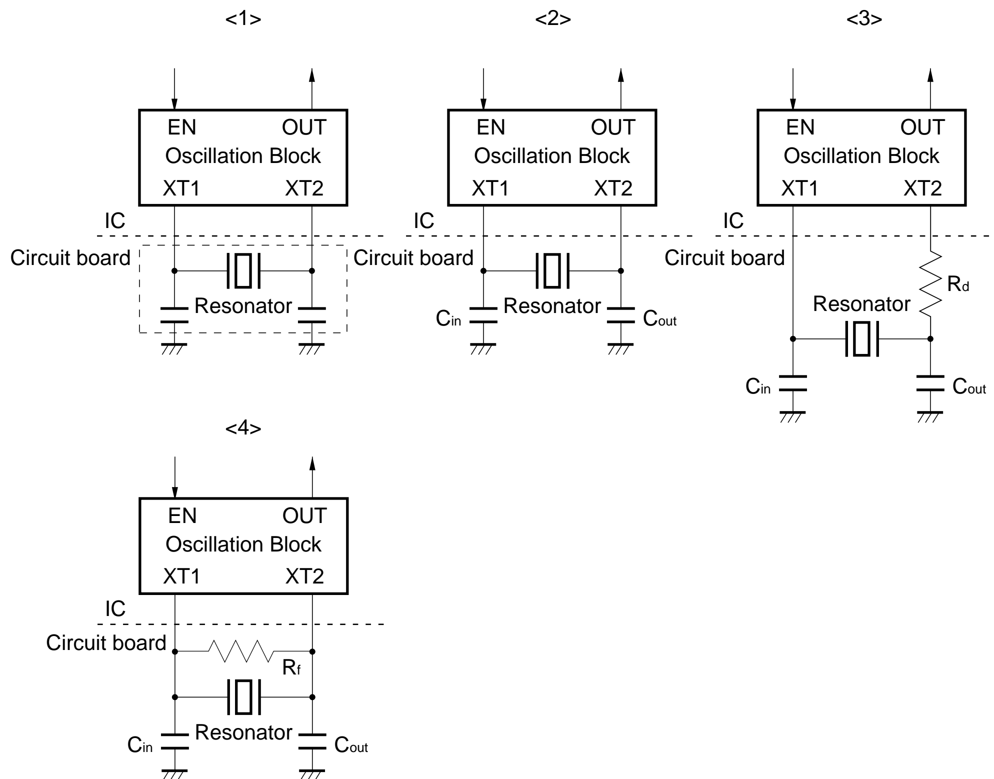
Table 9-3. Crystal Resonator Evaluation List

Material	Resonator Manufacturer	Frequency (kHz)	Part Number	Oscillation Block Name	Capacitor	Recommended External Constant					Circuit
						C_{in} (pF)	C_{out} (pF)	R_d (kΩ)	LT (μH)	CT (μF)	
Crystal	Seiko Instruments, Inc.	32.768	VT-200[Note] SP-T Series SSP-T Series	OSB1	Connected externally	12	15	100	–	–	<3>

Note Oscillation environment V_{DD} = 3.3 ± 0.3 V, T_A = –10 to +60°C

Remark Oscillation environment V_{DD} = 3.3 ± 0.3 V, T_A = –30 to +80°C
Since the oscillation status varies depending on the circuit board pattern, also perform evaluation on the actual board using the developed cell-based IC.

Figure 9-6. Oscillator Configuration Diagrams



9.4 GTL (Under Development)

GTL (Gunning Transceiver Logic) is a new type of interface standard that enables high-speed signal transmission using small signal amplitudes. The input section of a GTL is configured from a differential circuit (similar to those in ECL circuits) within a CMOS circuit. The output section's structure includes an enable pin attached to the N-ch open drain buffer. This enable pin is used to control GTL output in a manner similar to conventional three-state output buffers. A small-amplitude signal of 1.0 V or less can be used to terminate a GTL output pin using a potential that is less than the power supply voltage.

When using this interface, termination suited to the wire impedance may be required to prevent reflection of signals. Be extra cautious about the variation in the GND line due to the very small amplitude.

Caution Be sure to contact NEC before using this interface block.

9.4.1 Electrical characteristics

The GTL's electrical characteristics are listed in Table 9-4.

Table 9-4. Electrical Characteristics of GTL

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Terminating voltage	V_{TT}		1.14	1.2	1.26	V
Reference voltage	V_{REF}		(2/3) V_{TT} – 2%	0.8	(2/3) V_{TT} + 2%	V
High-level input voltage	V_{IH}		V_{REF} + 0.05	0.83		V
Low-level input voltage	V_{IL}			0.77	V_{REF} – 0.05	V
Low-level output current	I_{OL}	V_{OL} = 0.4 V	40			mA
Low-level output voltage	V_{OL}			0.2	0.4	V
Off-state output current	I_{OZ}	V_O = V_{TT} or GND			±10	μA
Input leakage current	I_I	V_I = V_{TT} or GND			±5	μA

9.4.2 Pin layout

Be sure to stay within the pin layout restrictions described below to ensure stable operation of GTLs.

<1> Position the GTL buffer only where there are pins that support it.

<2> Add at least one GND pin for each two GTL buffer pins
(Some package masters support adding one GND for each GTL buffer pin.)

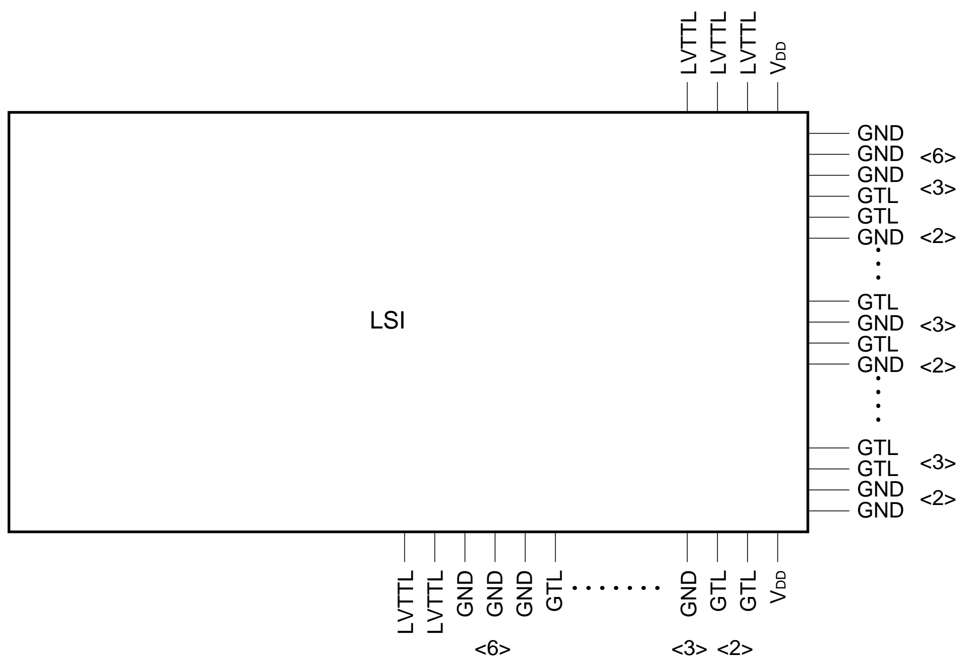
<3> Make sure that the added GND pins are adjacent to GTL buffer pins.

<4> GTL buffer pins can be grouped with GND pins on either side.

<5> Do not layout any non-GTL buffer pins (even for input buffers) between the GND or V_{DD} pins that enclose a group of GTL pins.

<6> Use sets of three GND pins to enclose a group of GTL pins.

Figure 9-7. GTL Pin Layout Example



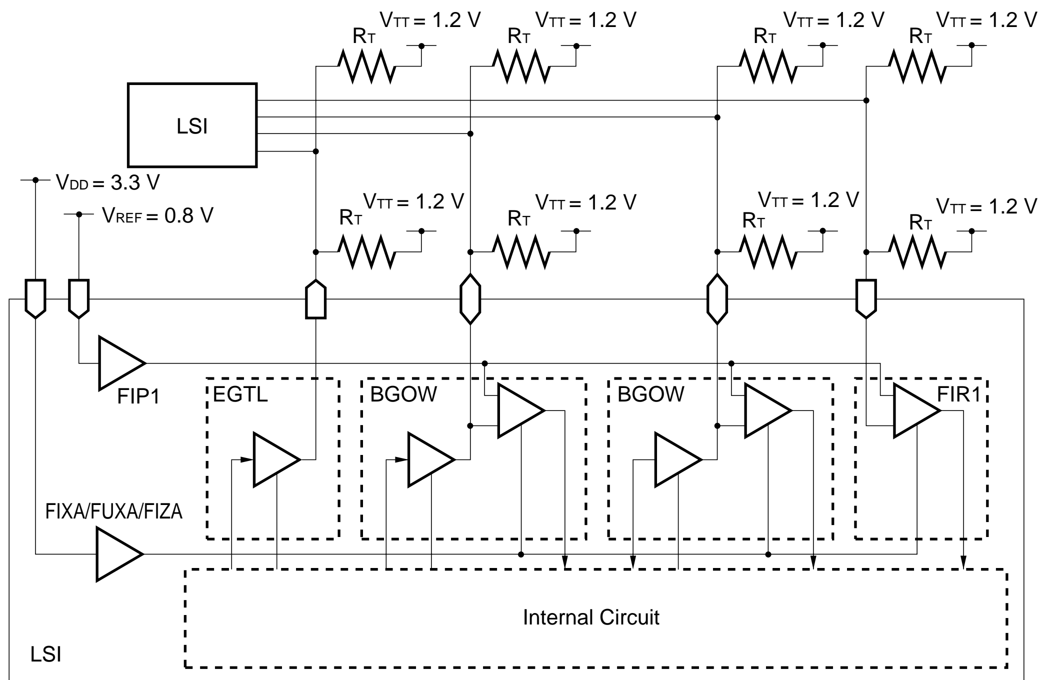
This layout does not affect restrictions on simultaneous operations using a different interface on the same chip.

9.4.3 Connection rules

When using a GTL interface, be sure to set up as external pins the pins for applying a reference voltage and the control pins for stopping the input section's operating current. Also, be sure to attach a suitable terminating resistor to prevent signal reflection.

Make sure that the pin via which the reference voltage is applied is connected via "FIP1" to the RFV pin in the GTL input buffer. Also, make sure that the GTL input buffer's control pin is connected via either "FIXA," "FUXA", or "FIZA" to the GTL input buffer's IEN pin.

Figure 9-8. GTL Use Example



9.4.4 Creation of test patterns

Note the following rules when using a GTL interface to create test patterns.

<1> Always use a high-level test pattern for the reference voltage input pin.

<2> Make sure that at least one of the test patterns for the input control pin is at low level.

<3> If there are any bidirectional pins (including for interface levels other than GTL), check the input/output direction of all bidirectional buffers before inputting low-level signals to the input control pin.

9.5 PCI Local Bus Buffer

The PCI (Peripheral Component Interconnect) local bus is an integrated standard for local bus architecture that improves the speed of bus lines where bottlenecks would otherwise occur as signals are arbitrated between the PC and its peripheral components. Since this bus standard has signal transfers performed mainly by reflected waves, standards must be specified for a wide array of factors, including not only the bus protocol but also the bus driver's electrical characteristics, the types of wire patterns and connectors used on the PC board, and even the shape of the PC board.

This section describes the CB-9 Family VX/VM type bus driver that complies with the PCI LOCAL BUS SPECIFICATION, REVISION 2.1.

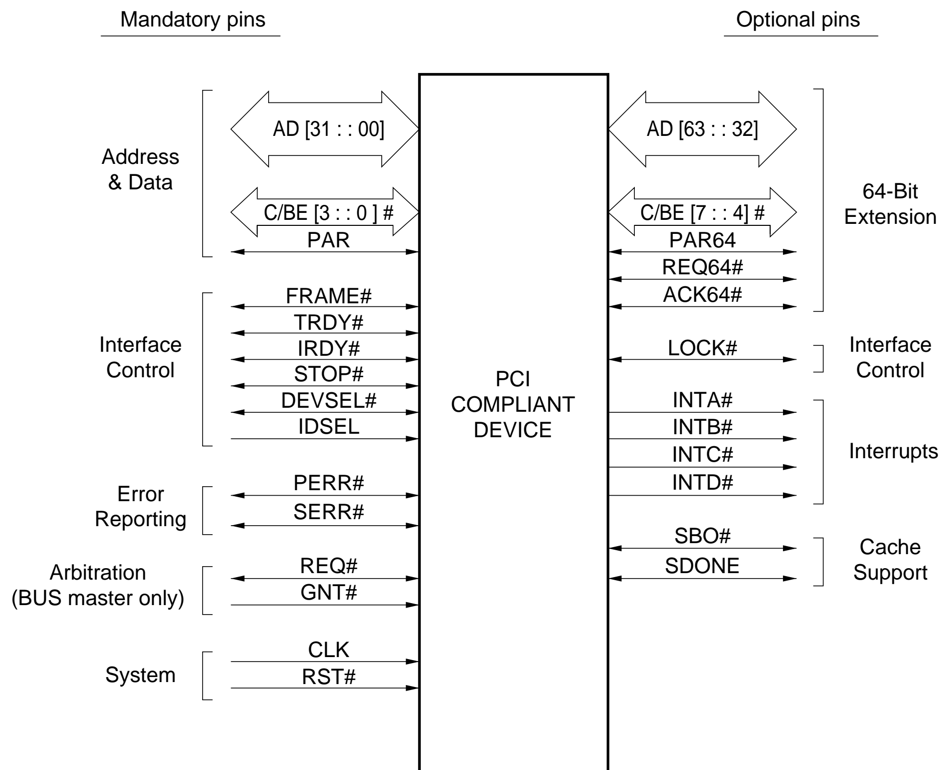
Before creating PCI components for CB-9 Family VX/VM type devices, be sure to join the "PCI Special Interest Group" (PCISIG) since the vendor ID and specific support will be needed.

9.5.1 Signal standard for PCI local bus

The PCI interface requires that the target device have at least 47 pins that can be used as signal pins and that the bus master have at least 49 pins that can be used as signal pins in order to support implementation of an address/data line, interface control line, system signal line, and arbitration control line.

The pin list for the PCI local bus is shown below.

Figure 9-9. PCI Pin List



The PCI blocks which are provided with CB-9 Family VX/VM type devices are listed below.

	Type	Input	Output	Three-state	Bi-directional
3-V PCI bus driver	VX, VM	FI01	FOIO	B00Y	BC0P
5-V PCI bus driver	VX	FPV1	FP14	BV0Y	BP1C
	VM	FI41AL	FVIOAL	BV0YAL	BDJPAL

Remark A clamping diode is included in the 5-V PCI buffer to protect it from reflected waves. When using a VX type 5-V PCI buffer, a separate 5-V (dedicated) power supply must be added.

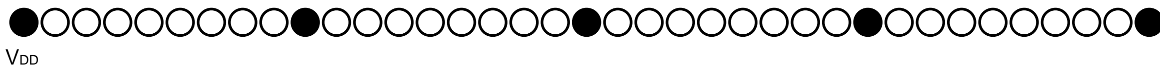
Cautions on use of VX type 5-V PCI buffer

A clamping diode is built into the 5-V PCI buffer to protect it from 11-V reflected waves (see diagram below). When using this buffer, a 5-V power supply pin must be added for the clamping diode.

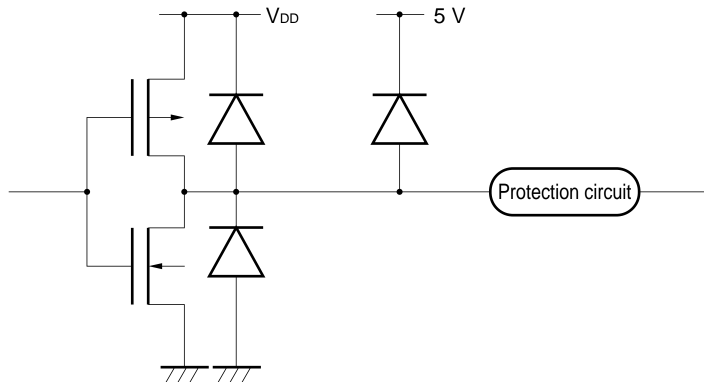
The added 5-V power supply pins should be laid out at both ends of the PCI buffer and spaced evenly with an 8-to-1 interval as shown below.

★ Furthermore, an additional power supply is required for each side.

Caution This added voltage has no relation to boosting power supply as a countermeasure for simultaneous operation.



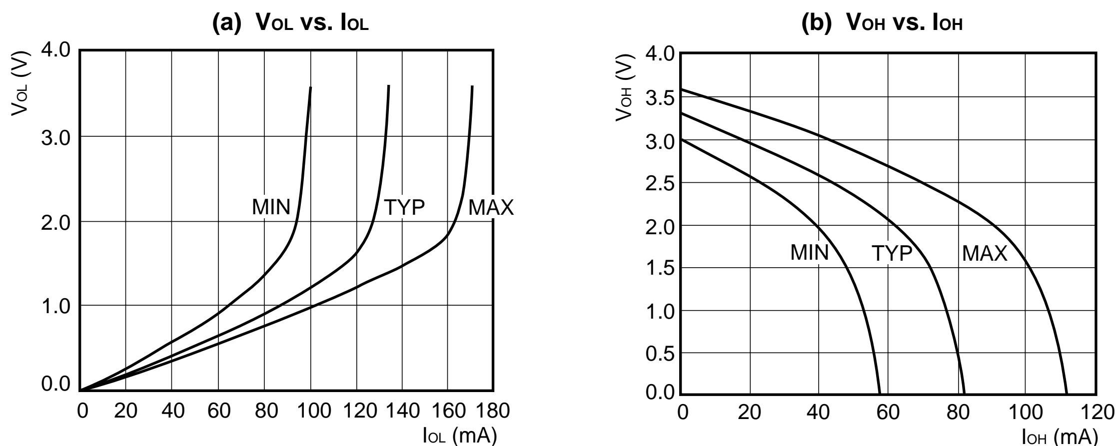
Since the distance to the bus is standardized, we recommend placing these along one edge of the chip. Crosstalk effects may have to be considered.



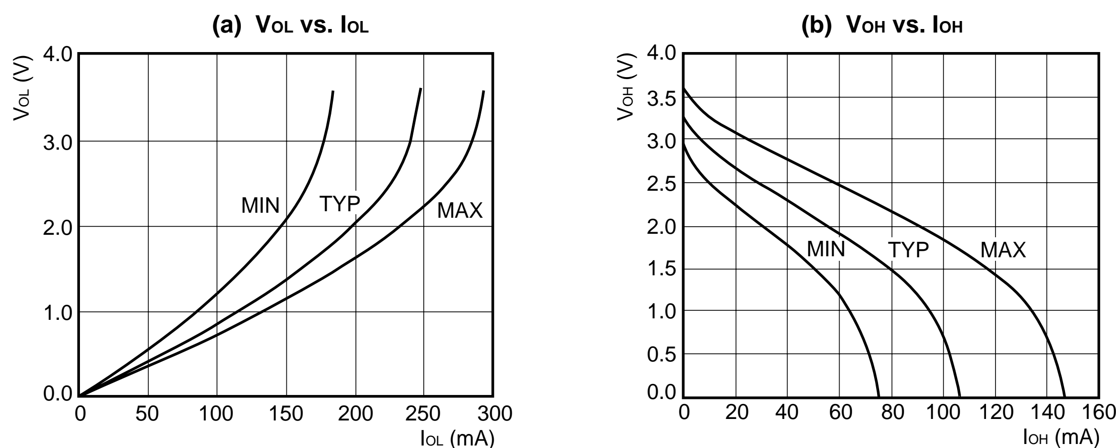
9.5.2 PCI buffer's output current (I_{OL}, I_{OH})

Figure 9-10. V_O vs. I_O

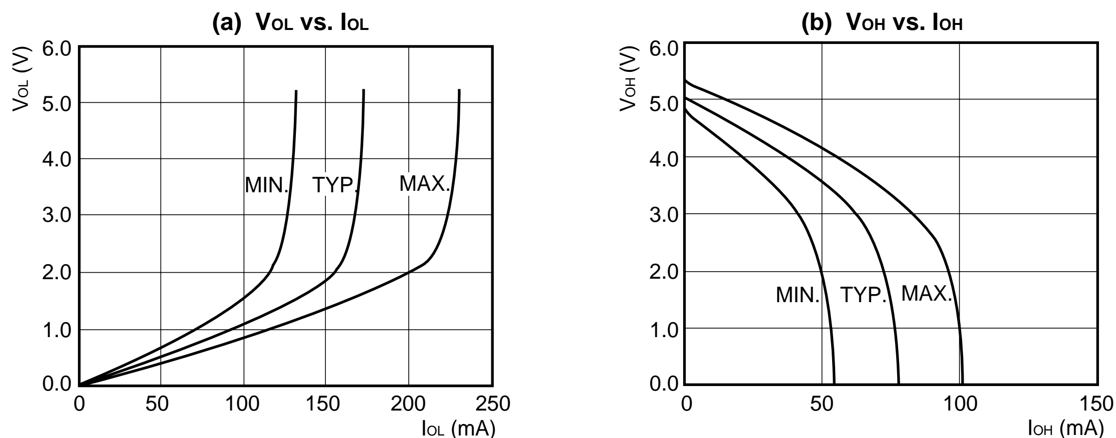
(1) 3-V PCI buffer



(2) 5-V PCI buffer (VX type)



(3) 5-V PCI buffer (VM type)



9.5.3 Electrical characteristics

When using a PCI buffer, the flow of signals on the transmission path must be evaluated in advance. This evaluation requires a certain amount of expertise. Contact NEC for information regarding the output current characteristics that must be considered when designing the propagation of signals on the transmission paths.

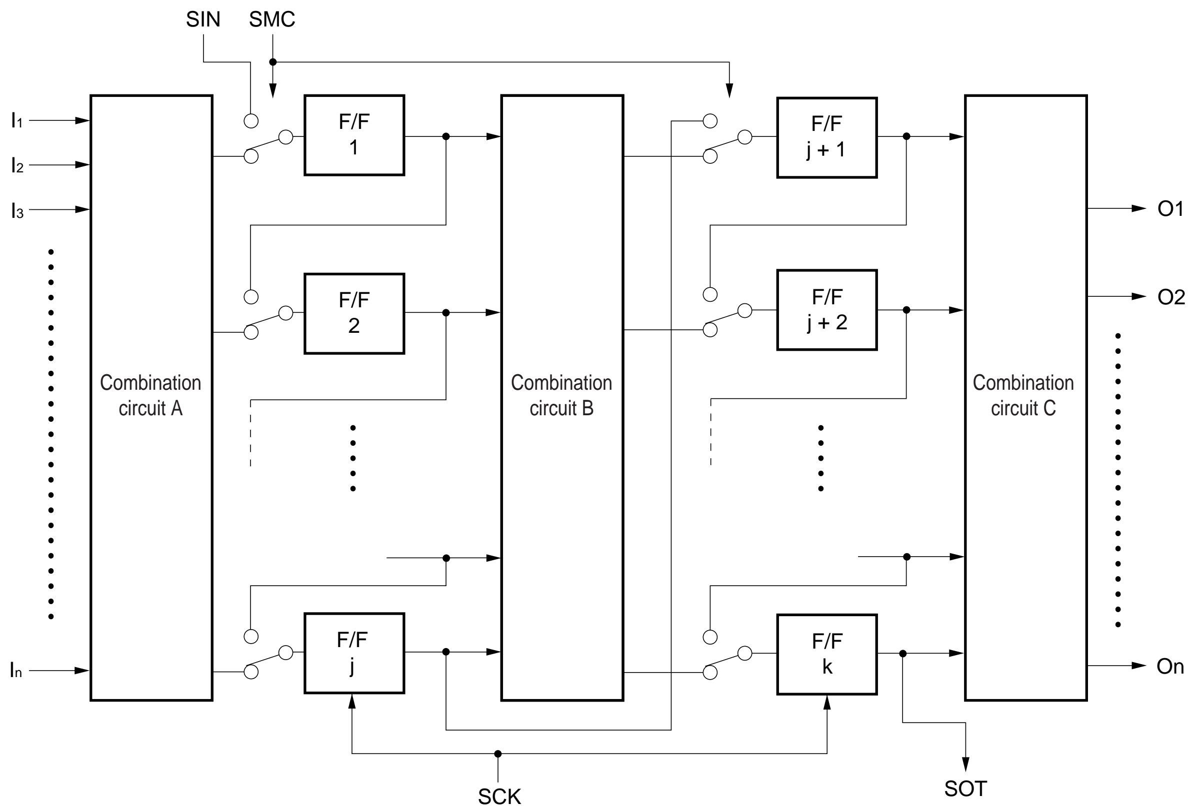
See **CHAPTER 3 PRODUCT SPECIFICATIONS** for details of DC characteristics and pin capacitance ratings.

9.6 Scan Path Test Block

It is very difficult to create an effective test pattern for checking the operation of LSIs whose circuits include many flip-flops and deep logic. The scan path test enables all of the flip-flops to be operated like shift registers. This is an efficient means of testing that makes it easy to initialize all of the flip-flops in a circuit with deep logic, and the status of all flip-flops can be read under various conditions.

For details, see **Design For Test User's Manual (A14357E)**.

Figure 9-11. Principles of Scan Path Test Method



Remark I_n: Input signal for combination circuit test or normal input

On: Diagnostic output during combination circuit test or normal output

SIN: Input signal for sequential circuit test

SMC: Mode switching signal

SCK: Test clock

SOT: Diagnostic output during sequential circuit test

A.1 VX Type

A.1.1 When using 3.3-V single power supply pins

Table A-1. List of Power Supply Pins in Packages (VX Type, 3.3-V Single Power Supply) (1/6)

Package		GND Pin Position	V_{DD} Pin Position	Oscillator Assignable Position	Signal count [Note 2]	NC Pin Position [Note 2]
QFP	44-pin	17	39	Under study	42	–
	52-pin	7, 33	34	Under study	48	14
	64-pin	26, 58	27	Under study	61	–
	100-pin	1, 28, 40, 53, 80	2, 29, 52, 79	Under study	91	
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	Under study	110	
	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	Under study	144	
TQFP	80-pin	1, 20, 41, 60	21, 40, 61, 80	Under study	72	–
QFP (fine pitch)	100-pin	26, 50, 76, 100	1, 25, 51, 75	Under study	92	–
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	Under study	110	
	144-pin	37, 38, 71, 72, 109, 110, 143, 144	1, 36, 73, 108	Under study	132	
	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	Under study	144	
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	Under study	160	

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-1. List of Power Supply Pins in Packages (VX Type, 3.3-V Single Power Supply) (2/6)

Low thermal resistance type

Package		GND Pin Position	V_{DD} Pin Position	Oscillator Assignable Position	Signal count Note 1	NC Pin Position Note 2
QFP	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	Under study	144	–
QPF (fine pitch)	144-pin	37, 38, 71, 72, 109, 110, 143, 144	1, 36, 73, 108	Under study	132	
	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	Under study	144	
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	Under study	160	
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131, 155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	Under study	188	
	240-pin	1, 2, 20, 41, 59, 60, 80, 101, 121, 122, 139, 161, 179, 180, 200, 221	21, 40, 61, 81, 100, 120, 140, 160, 181, 201, 220, 240	Under study	212	
	256-pin	1, 2, 21, 44, 63, 64, 85, 108, 129, 130, 149, 172, 191, 192, 213, 236	22, 43, 65, 86, 107, 128, 150, 171, 193, 214, 235, 256	Under study	228	
	304-pin	1, 2, 20, 39, 40, 58, 75, 76, 95, 96, 115, 116, 133, 134, 153, 154, 172, 191, 192, 210, 227, 228, 247, 248, 267, 268, 285, 286	19, 37, 38, 57, 77, 78, 113, 114, 151, 152, 171, 189, 190, 209, 229, 230, 265, 266, 303, 304	Under study	256	
TQFP	64-pin	9, 41	10	Under study	Under study	
	100-pin	26, 50, 76, 100	1, 25, 51, 75	Under study	92	
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	Under study	110	
LQFP	144-pin	37, 38, 71, 72, 109, 110, 143, 144	1, 36, 73, 108	Under study	132	
	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	Under study	144	
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	Under study	160	
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131, 155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	Under study	188	

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-1. List of Power Supply Pins in Packages (VX Type, 3.3-V Single Power Supply) (3/6)

Low thermal resistance type + HSP Note 1

Package		GND Pin Position	V_{DD} Pin Position	Oscillator Assignable Position	Signal count Note 2	NC Pin Position Note 3
QFP	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	Under study	144	–
QFP (fine pitch)	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	Under study	144	
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	Under study	160	
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131, 155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	Under study	188	
	240-pin	1, 2, 20, 41, 59, 60, 80, 101, 121, 122, 139, 161, 179, 180, 200, 221	21, 40, 61, 81, 100, 120, 140, 160, 181, 201, 220, 240	Under study	212	
	304-pin	1, 2, 20, 39, 40, 58, 75, 76, 95, 96, 115, 116, 133, 134, 153, 154, 172, 191, 192, 210, 227, 228, 247, 248, 267, 268, 285, 286	19, 37, 38, 57, 77, 78, 113, 114, 151, 152, 171, 189, 190, 209, 229, 230, 265, 266, 303, 304	Under study	256	

Notes 1. HSP: Heat spreader

2. This indicates the total number of usable signal pins.

3. NC pin can be generated by combination of the package and step size.

Table A-1. List of Power Supply Pins in Packages (VX Type, 3.3-V Single Power Supply) (4/6)

Package		GND Pin Position	V_{DD} Pin Position	Oscillator Assignable Position	Signal count [Note 1]	NC Pin Position [Note 2]
Plastic BGA	225-pin	203, 207, 211, 215, 217, 218, 219, 220, 221, 222, 223, 224, 225	201, 202, 204, 205, 206, 208, 209, 210, 212, 213, 214, 216	Under study	200	–
	256-pin	1, 205, 209, 214, 218, 222, 227, 231, 235, 240, 244, 248, 253	207, 211, 216, 220, 224, 229, 233, 237, 242, 246, 250, 255		231	–
	313-pin	275, 279, 283, 287, 290, 291, 293, 294, 296, 297, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313	254, 255, 256, 257, 259, 260, 261, 262, 264, 265, 266, 267, 269, 270, 271, 272, 273, 274, 276, 277, 278, 280, 281, 282, 284, 285, 286, 288, 289, 292, 295, 298		256	–
	352-pin	1, 25, 26, 50, 51, 75, 76, 100, 101, 124, 147, 170, 193, 214, 235, 256, 277, 281, 286, 291, 296, 300, 305, 310, 315, 319, 324, 329, 334, 338, 343, 348	279, 284, 289, 294, 298, 303, 308, 313, 317, 322, 327, 332, 336, 341, 346, 351		304	–

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-1. List of Power Supply Pins in Packages (VX Type, 3.3-V Single Power Supply) (5/6)

Package		GND Pin Position	V_{DD} Pin Position	Oscillator Asignable Position	Signal Count [Note 1]	NC Pin Position [Note 2]
Tape BGA	256-pin	205, 208, 212, 215, 218, 221, 225, 228, 231, 234, 238, 241, 244, 247, 251, 254	145, 149, 153, 156, 160, 164, 168, 171, 175, 179, 183, 186, 190, 194, 198, 201	Under study	224	–
	352-pin	277, 280, 283, 287, 290, 293, 296, 299, 302, 306, 309, 312, 315, 318, 321, 325, 328, 331, 334, 337, 340, 344, 347, 350	193, 197, 200, 204, 207, 210, 214, 218, 221, 225, 228, 231, 235, 239, 242, 246, 249, 252, 256, 260, 263, 267, 270, 273	Under study	304	–
	420-pin	353, 356, 358, 360, 363, 365, 367, 370, 373, 375, 377, 380, 382, 384, 387, 390, 392, 394, 397, 399, 401, 404, 407, 409, 411, 414, 416, 418	277, 281, 283, 285, 288, 290, 292, 296, 300, 302, 304, 307, 309, 311, 315, 319, 321, 323, 326, 328, 330, 334, 338, 340, 342, 345, 347, 349	Under study	364	–
	500-pin	417, 420, 422, 424, 426, 429, 431, 433, 435, 438, 441, 443, 445, 447, 450, 452, 454, 456, 459, 462, 464, 466, 468, 471, 473, 475, 477, 480, 483, 485, 487, 489, 492, 494, 496, 498	325, 329, 331, 333, 335, 338, 340, 342, 344, 348, 352, 354, 356, 358, 361, 363, 365, 367, 371, 375, 377, 379, 381, 384, 386, 388, 390, 394, 398, 400, 402, 404, 407, 409, 411, 413	Under study	428	–
	576-pin	501, 503, 505, 507, 509, 510, 512, 514, 516, 518, 520, 522, 524, 526, 528, 529, 531, 533, 535, 537, 539, 541, 543, 545, 547, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 567, 569, 571, 573, 575	417, 420, 422, 424, 426, 427, 429, 431, 433, 435, 438, 441, 443, 445, 447, 448, 450, 452, 454, 456, 459, 462, 464, 466, 468, 469, 471, 473, 475, 477, 480, 483, 485, 487, 489, 490, 492, 494, 496, 498	Under study	496	–

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-1. List of Power Supply Pins in Packages (VX Type, 3.3-V Single Power Supply) (6/6)

Package		GND Pin Position	V_{DD} Pin Position	Oscillator Asignable Position	Signal Count Note 1	NC Pin Position Note 2
Tape BGA	696-pin	6, 12, 18, 24, 34, 40, 46, 52, 62, 68, 74, 80, 90, 96, 102, 108, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 699	488, 490, 491, 493, 494, 496, 497, 499, 500, 502, 503, 505, 506, 508, 509, 511, 517, 519, 520, 522, 523, 525, 526, 529, 531, 532, 534, 535, 537, 538, 540, 546, 548, 549, 551, 552, 554, 555, 557, 558, 560, 561, 563, 564, 566, 567, 569, 575, 577, 578, 580, 581, 583, 584, 587, 589, 590, 592, 593, 595, 596, 598	Under study	506	246, 252, 278, 284, 310, 316, 342, 348, 374, 380, 405, 411, 436, 442, 467, 473

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

A.1.2 When using internal 2.0-V type power supply pins

Note that in the 304-pin QFP (fine pitch) packages, the position of the 3.3-V power supply is slightly different than in VX-type packages (3.3-V single power supply).

Table A-2. List of Power Supply Pins in Packages (VX Type, When Using Internal 2.0-V Power Supply Pin) (1/5)

Package		GND Pin Position	3.3-V V_{DD} Pin Position	2.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count Note 1	NC Pin Position Note 2
QFP	100-pin	1, 28, 40, 53, 80	2, 29, 52, 79	3, 30, 51, 78	Under study	87	–
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	2, 29, 62, 89	Under study	106	–
QFP (fine pitch)	100-pin	26, 50, 76, 100	1, 25, 51, 75	2, 24, 52, 74	Under study	88	–
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	2, 29, 62, 89	Under study	106	–
	144-pin	37, 38, 71, 72, 109, 110, 143, 144	1, 36, 73, 108	2, 35, 74, 107	Under study	128	–
	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	2, 39, 43, 78, 82, 119, 123, 158	Under study	136	–
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	2, 43, 47, 86, 90, 131, 135, 174	Under study	152	–

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-2. List of Power Supply Pins in Packages (VX Type, When Using Internal 2.0-V Power Supply Pin) (2/5)

Low thermal resistance type

Package		GND Pin Position	3.3-V V_{DD} Pin Position	2.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count Note 1	NC Pin Position Note 2
QFP (fine pitch)	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	2, 43, 47, 86, 90, 131, 135, 174	Under study	152	–
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131, 155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	3, 50, 54, 103, 107, 154, 158, 207	Under study	180	–
	240-pin	1, 2, 20, 41, 59, 60, 80, 101, 121, 122, 139, 161, 179, 180, 200, 221	21, 40, 61, 81, 100, 120, 140, 160, 181, 201, 220, 240	3, 58, 62, 119, 123, 178, 182, 239	Under study	204	–
	256-pin	1, 2, 21, 44, 63, 64, 85, 108, 129, 130, 149, 172, 191, 192, 213, 236	22, 43, 65, 86, 107, 128, 150, 171, 193, 214, 235, 256	3, 62, 66, 127, 131, 190, 194, 255	Under study	220	–
	304-pin	1, 2, 20, 39, 40, 58, 75, 76, 95, 96, 115, 116, 133, 134, 153, 154, 172, 191, 192, 210, 227, 228, 247, 248, 267, 268, 285, 286	19, 37, 38, 57, 77, 113, 114, 152, 171, 189, 190, 209, 229, 265, 266, 304	3, 74, 78, 151, 155, 226, 230, 303	Under study	252	–
LQFP	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	2, 43, 47, 86, 90, 131, 135, 174	Under study	152	–

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-2. List of Power Supply Pins in Packages (VX Type, When Using Internal 2.0-V Power Supply Pin) (3/5)

Low thermal resistance type + HSP Note 1

Package		GND Pin Position	3.3-V V_{DD} Pin Position	2.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count Note 2	NC Pin Position Note 3
QFP (fine pitch)	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	2, 39, 43, 78, 82, 119, 123, 158	Under study	136	–
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	2, 43, 47, 86, 90, 131, 135, 174	Under study	152	–
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131,155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	3, 50, 54, 103, 107, 154, 158, 207	Under study	180	–
	240-pin	1, 2, 20, 41, 59, 60, 80, 101, 121, 122, 139, 161, 179, 180, 200, 221	21, 40, 61, 81, 100, 120, 140, 160, 181, 201, 220, 240	3, 58, 62, 119, 123, 178, 182, 239	Under study	204	–
	304-pin	1, 2, 20, 39, 40, 58, 75, 76, 95, 96, 115, 116, 133, 134, 153, 154, 172, 191, 192, 210, 227, 228, 247, 248, 267, 268, 285, 286	19, 37, 38, 57, 77, 113, 114, 152, 171, 189, 190, 209, 229, 265, 266, 304	3, 74, 78, 151, 155, 226, 230, 303	Under study	252	–

Notes 1. HSP: Heat spreader

2. This indicates the total number of usable signal pins.

3. NC pin can be generated by combination of the package and step size.

Table A-2. List of Power Supply Pins in Packages (VX Type, When Using Internal 2.0-V Power Supply Pin) (4/5)

Package		GND Pin Position	3.3-V V_{DD} Pin Position	2.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count Note 1	NC Pin Position Note 2
Tape BGA	256-pin	205, 208, 212, 215, 218, 221, 225, 228, 231, 234, 238, 241, 244, 247, 251, 254	145, 149, 153, 156, 160, 164, 168, 171, 175, 179, 183, 186, 190, 194, 198, 201	209, 214, 222, 227, 235, 240, 248, 253	Under study	216	–
	352-pin	277, 280, 283, 287, 290, 293, 296, 299, 302, 306, 309, 312, 315, 318, 321, 325, 328, 331, 334, 337, 340, 344, 347, 350	193, 197, 200, 204, 207, 210, 214, 218, 221, 225, 228, 231, 235, 239, 242, 246, 249, 252, 256, 260, 263, 267, 270, 273	281, 285, 291, 300, 304, 310, 319, 323, 329, 338, 342, 348	Under study	292	–
	420-pin	353, 356, 358, 360, 363, 365, 367, 370, 373, 375, 377, 380, 382, 384, 387, 390, 392, 394, 397, 399, 401, 404, 407, 409, 411, 414, 416, 418	277, 281, 283, 285, 288, 290, 292, 296, 300, 302, 304, 307, 309, 311, 315, 319, 321, 323, 326, 328, 330, 334, 338, 340, 342, 345, 347, 349	354, 359, 364, 369, 371, 381, 386, 388, 393, 398, 403, 405, 415, 420	Under study	350	–
	500-pin	417, 420, 422, 424, 426, 429, 431, 433, 435, 438, 441, 443, 445, 447, 450, 452, 454, 456, 459, 462, 464, 466, 468, 471, 473, 475, 477, 480, 483, 485, 487, 489, 492, 494, 496, 498	325, 329, 331, 333, 335, 338, 340, 342, 344, 348, 352, 354, 356, 358, 361, 363, 365, 367, 371, 375, 377, 379, 381, 384, 386, 388, 390, 394, 398, 400, 402, 404, 407, 409, 411, 413	418, 421, 428, 434, 437, 439, 442, 455, 458, 460, 463, 470, 476, 479, 481, 484, 497, 500	Under study	410	–

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-2. List of Power Supply Pins in Packages (VX Type, When Using Internal 2.0-V Power Supply Pin) (5/5)

Package		GND Pin Position	3.3-V V_{DD} Pin Position	2.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count Note 1	NC Pin Position Note 2
Tape BGA	576-pin	501, 503, 505, 507, 509, 510, 512, 514, 516, 518, 520, 522, 524, 526, 528, 529, 531, 533, 535, 537, 539, 541, 543, 545, 547, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 567, 569, 571, 573, 575	417, 420, 422, 424, 426, 427, 429, 431, 433, 435, 438, 441, 443, 445, 447, 448, 450, 452, 454, 456, 459, 462, 464, 466, 468, 469, 471, 473, 475, 477, 480, 483, 485, 487, 489, 490, 492, 494, 496, 498	502, 506, 511, 515, 519, 521, 525, 530, 534, 538, 540, 544, 549, 553, 557, 559, 563, 568, 572, 576	Under study	476	–
	696-pin	6, 12, 18, 24, 34, 40, 46, 52, 62, 68, 74, 80, 90, 96, 102, 108, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696	488, 490, 491, 493, 494, 496, 497, 499, 500, 502, 503, 505, 506, 508, 509, 511, 517, 519, 520, 522, 523, 525, 526, 529, 531, 532, 534, 535, 537, 538, 540, 546, 548, 549, 551, 552, 554, 555, 557, 558, 560, 561, 563, 564, 566, 567, 569, 575, 577, 578, 580, 581, 583, 584, 587, 589, 590, 592, 593, 595, 596, 598	489, 492, 495, 498, 501, 504, 507, 510, 518, 521, 524, 528, 533, 536, 539, 547, 550, 553, 556, 559, 562, 565, 568, 576, 579, 582, 586, 591, 594, 597	Under study	476	246, 252, 278, 284, 310, 316, 342, 348, 374, 380, 405, 411, 436, 442, 467, 473

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

A.2 VM Type

Note that in the 304-pin QFP (fine pitch) package, the position of the 3.3-V power supply is slightly different than in VX-type packages (3.3-V single power supply).

Table A-3. List of Power Supply Pins in Packages (VM Type) (1/5)

42 material

Package		GND Pin Position	3.3-V V_{DD} Pin Position	5.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count Note 1	NC Pin Position Note 2
QFP	100-pin	1, 28, 40, 53, 80	2, 29, 52, 79	3, 30, 51, 78	Under study	87	–
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	2, 29, 62, 89	Under study	106	–
QFP (fine pitch)	100-pin	26, 50, 76, 100	1, 25, 51, 75	2, 24, 52, 74	Under study	88	–
	120-pin	15, 31, 60, 75, 91, 120	1, 30, 61, 90	2, 29, 62, 89	Under study	106	–
	144-pin	37, 38, 71, 72, 109, 110, 143, 144	1, 36, 73, 108	2, 35, 74, 107	Under study	128	–
	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	2, 39, 43, 78, 82, 119, 123, 158	Under study	136	–
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	2, 43, 47, 86, 90, 131, 135, 174	Under study	152	–

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-3. List of Power Supply Pins in Packages (VM Type) (2/5)

Copper material Note 1

Package		GND Pin Position	3.3-V V_{DD} Pin Position	5.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count Note 2	NC Pin Position Note 3
QFP (fine pitch)	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	2, 43, 47, 86, 90, 131, 135, 174	Under study	152	–
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131,155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	3, 50, 54, 103, 107, 154, 158, 207	Under study	180	–
	240-pin	1, 2, 20, 41, 59, 60, 80, 101, 121, 122, 139, 161, 179, 180, 200, 221	21, 40, 61, 81, 100, 120, 140, 160, 181, 201, 220, 240	3, 58, 62, 119, 123, 178, 182, 239	Under study	204	–
	256-pin	1, 2, 21, 44, 63, 64, 85, 108, 129, 130, 149, 172, 191, 192, 213, 236	22, 43, 65, 86, 107, 128, 150, 171, 193, 214, 235, 256	3, 62, 66, 127, 131, 190, 194, 255	Under study	220	–
	304-pin	1, 2, 20, 39, 40, 58, 75, 76, 95, 96, 115, 116, 133, 134, 153, 154, 172, 191, 192, 210, 227, 228, 247, 248, 267, 268, 285, 286	19, 37, 38, 57, 77, 113, 114, 152, 171, 189, 190, 209, 229, 265, 266, 304	3, 74, 78, 151, 155, 226, 230, 303	Under study	252	–
LQFP	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	2, 43, 47, 86, 90, 131, 135, 174	Under study	152	–

Notes 1. Low thermal resistance type

2. This indicates the total number of usable signal pins.

3. NC pin can be generated by combination of the package and step size.

Table A-3. List of Power Supply Pins in Packages (VM Type) (3/5)

Copper [Note 1] + HSP [Note 2]

Package		GND Pin Position	3.3-V V_{DD} Pin Position	5.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count [Note 3]	NC Pin Position [Note 4]
QFP (fine pitch)	160-pin	21, 41, 42, 79, 80, 101, 121, 122, 159, 160	1, 20, 40, 81, 100, 120	2, 39, 43, 78, 82, 119, 123, 158	Under study	136	–
	176-pin	23, 45, 46, 87, 88, 111, 133, 134, 175, 176	1, 22, 44, 89, 110, 132	2, 43, 47, 86, 90, 131, 135, 174	Under study	152	–
	208-pin	1, 2, 26, 51, 52, 79, 105, 106, 131,155, 156, 182	27, 53, 78, 104, 130, 157, 183, 208	3, 50, 54, 103, 107, 154, 158, 207	Under study	180	–
	240-pin	1, 2, 20, 41, 59, 60, 80, 101, 121, 122, 139, 161, 179, 180, 200, 221	21, 40, 61, 81, 100, 120, 140, 160, 181, 201, 220, 240	3, 58, 62, 119, 123, 178, 182, 239	Under study	204	–
	304-pin	1, 2, 20, 39, 40, 58, 75, 76, 95, 96, 115, 116, 133, 134, 153, 154, 172, 191, 192, 210, 227, 228, 247, 248, 267, 268, 285, 286	19, 37, 38, 57, 77, 113, 114, 152, 171, 189, 190, 209, 229, 265, 266, 304	3, 74, 78, 151, 155, 226, 230, 303	Under study	252	–

Notes 1. Low thermal resistance type

2. HSP: Heat spreader

3. This indicates the total number of usable signal pins.

4. NC pin can be generated by combination of the package and step size.

Table A-3. List of Power Supply Pins in Packages (VM Type) (4/5)

Package		GND Pin Position	3.3-V V_{DD} Pin Position	5.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count Note 1	NC Pin Position Note 2
Tape BGA	256-pin	205, 208, 212, 215, 218, 221, 225, 228, 231, 234, 238, 241, 244, 247, 251, 254	145, 149, 153, 156, 160, 164, 168, 171, 175, 179, 183, 186, 190, 194, 198, 201	209, 214, 222, 227, 235, 240, 248, 253	Under study	216	–
	352-pin	277, 280, 283, 287, 290, 293, 296, 299, 302, 306, 309, 312, 315, 318, 321, 325, 328, 331, 334, 337, 340, 344, 347, 350	193, 197, 200, 204, 207, 210, 214, 218, 221, 225, 228, 231, 235, 239, 242, 246, 249, 252, 256, 260, 263, 267, 270, 273	281, 285, 291, 300, 304, 310, 319, 323, 329, 338, 342, 348	Under study	292	–
	420-pin	353, 356, 358, 360, 363, 365, 367, 370, 373, 375, 377, 380, 382, 384, 387, 390, 392, 394, 397, 399, 401, 404, 407, 409, 411, 414, 416, 418	277, 281, 283, 285, 288, 290, 292, 296, 300, 302, 304, 307, 309, 311, 315, 319, 321, 323, 326, 328, 330, 334, 338, 340, 342, 345, 347, 349	354, 359, 364, 369, 371, 381, 386, 388, 393, 398, 403, 405, 415, 420	Under study	350	–
	500-pin	417, 420, 422, 424, 426, 429, 431, 433, 435, 438, 441, 443, 445, 447, 450, 452, 454, 456, 459, 462, 464, 466, 468, 471, 473, 475, 477, 480, 483, 485, 487, 489, 492, 494, 496, 498	325, 329, 331, 333, 335, 338, 340, 342, 344, 348, 352, 354, 356, 358, 361, 363, 365, 367, 371, 375, 377, 379, 381, 384, 386, 388, 390, 394, 398, 400, 402, 404, 407, 409, 411, 413	418, 421, 428, 434, 437, 439, 442, 455, 458, 460, 463, 470, 476, 479, 481, 484, 497, 500	Under study	410	–

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

Table A-3. List of Power Supply Pins in Packages (VM Type) (5/5)

Package		GND Pin Position	3.3-V V_{DD} Pin Position	5.0-V V_{DD} Pin Position	Oscillator Assignable Position	Signal Count [Note 1]	NC Pin Position [Note 2]
Tape BGA	576-pin	501, 503, 505, 507, 509, 510, 512, 514, 516, 518, 520, 522, 524, 526, 528, 529, 531, 533, 535, 537, 539, 541, 543, 545, 547, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 567, 569, 571, 573, 575	417, 420, 422, 424, 426, 427, 429, 431, 433, 435, 438, 441, 443, 445, 447, 448, 450, 452, 454, 456, 459, 462, 464, 466, 468, 469, 471, 473, 475, 477, 480, 483, 485, 487, 489, 490, 492, 494, 496, 498	502, 506, 511, 515, 519, 521, 525, 530, 534, 538, 540, 544, 549, 553, 557, 559, 563, 568, 572, 576	Under study	476	–
	696-pin	6, 12, 18, 24, 34, 40, 46, 52, 62, 68, 74, 80, 90, 96, 102, 108, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696	488, 490, 491, 493, 494, 496, 497, 499, 500, 502, 503, 505, 506, 508, 509, 511, 517, 519, 520, 522, 523, 525, 526, 529, 531, 532, 534, 535, 537, 538, 540, 546, 548, 549, 551, 552, 554, 555, 557, 558, 560, 561, 563, 564, 566, 567, 569, 575, 577, 578, 580, 581, 583, 584, 587, 589, 590, 592, 593, 595, 596, 598	489, 492, 495, 498, 501, 504, 507, 510, 518, 521, 524, 528, 533, 536, 539, 547, 550, 553, 556, 559, 562, 565, 568, 576, 579, 582, 586, 591, 594, 597	Under study	476	246, 252, 278, 284, 310, 316, 342, 348, 374, 380, 405, 411, 436, 442, 467, 473

Notes 1. This indicates the total number of usable signal pins.

2. NC pin can be generated by combination of the package and step size.

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