

March 1993

High Frequency N-P-N Transistor Array

Features

- Gain Bandwidth Product (f_T) >1GHz
- Power Gain 30dB (Typ) at 100MHz
- Noise Figure 3.5dB (Typ) at 100MHz
- Five Independent Transistors on a Common Substrate

Applications

- VHF Amplifiers
- Multifunction Combinations - RF/Mixer/Oscillator
- Sense Amplifiers
- Synchronous Detectors
- VHF Mixers
- IF Converter
- IF Amplifiers
- Synthesizers
- Cascade Amplifiers

Description

The CA3127* consists of five general purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low $1/f$ noise and a value of f_T in excess of 1GHz, making the CA3127 useful from DC to 500MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

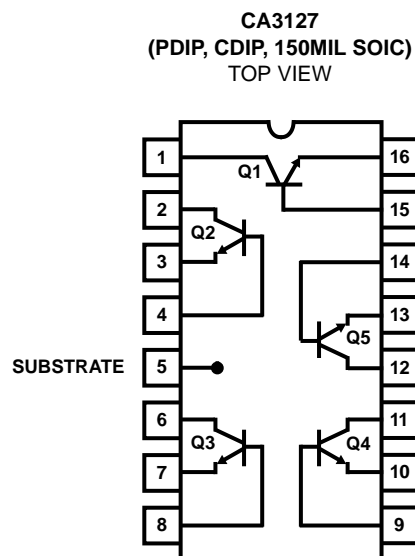
* Formerly Development Number TA6206.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3127E	-55°C to +125°C	16 Lead Plastic DIP
CA3127F	-55°C to +125°C	16 Lead Ceramic DIP
CA3127M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3127M96	-55°C to +125°C	16 Lead Narrow Body SOIC*

* Denotes Tape and Reel.

Pinout



Specifications CA3127

Absolute Maximum Ratings

Power Dissipation, P_D
 Any One Transistor 85mW
 Total Package
 For T_A Up to $+75^\circ\text{C}$ 425mW
 For $T_A > +75^\circ\text{C}$ Derate Linearly at 6.67mW/ $^\circ\text{C}$

The following ratings apply for each transistor in the device

Collector-to-Emitter Voltage, V_{CEO} 15V
 Collector-to-Base Voltage, V_{CBO} 20V
 Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
 Collector Current, I_C 20mA
 Junction Temperature $+175^\circ\text{C}$
 Junction Temperature (Plastic Packages) $+150^\circ\text{C}$
 Lead Temperature (Soldering 10 Sec.) $+300^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range -55°C to $+125^\circ\text{C}$
 Storage Temperature Range -65°C to $+150^\circ\text{C}$

Electrical Specifications $T_A = +25^\circ\text{C}$

PARAMETERS	TEST CONDITIONS	LIMITS			UNITS	
		MIN	TYP	MAX		
DC SPECIFICATIONS (For Each Transistor)						
Collector-to-Base Breakdown Voltage	$I_C = 10\mu\text{A}, I_E = 0$	20	32	-	V	
Collector-to-Emitter Breakdown Voltage	$I_C = 1\text{mA}, I_B = 0$	15	24	-	V	
Collector-to-Substrate Breakdown-Voltage	$I_{C1} = 10\mu\text{A}, I_B = 0, I_E = 0$	20	60	-	V	
Emitter-to-Base Breakdown Voltage (Note 2)	$I_E = 10\mu\text{A}, I_C = 0$	4	5.7	-	V	
Collector-Cutoff-Current	$V_{CE} = 10\text{V}, I_B = 0$	-	-	0.5	μA	
Collector-Cutoff-Current	$V_{CB} = 10\text{V}, I_E = 0$	-	-	40	nA	
DC Forward-Current Transfer Ratio	$V_{CE} = 6\text{V}$	$I_C = 5\text{mA}$	35	88	-	
		$I_C = 1\text{mA}$	40	90	-	
		$I_C = 0.1\text{mA}$	35	85	-	
Base-to-Emitter Voltage	$V_{CE} = 6\text{V}$	$I_C = 5\text{mA}$	0.71	0.81	0.91	V
		$I_C = 1\text{mA}$	0.66	0.76	0.86	V
		$I_C = 0.1\text{mA}$	0.60	0.70	0.80	V
Collector-to-Emitter Saturation Voltage	$I_C = 10\text{mA}, I_B = 1\text{mA}$	-	0.26	0.50	V	
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched	-	0.5	5	mV	
Magnitude of Difference in I_B	$V_{CE} = 6\text{V}, I_C = 1\text{mA}$	-	0.2	3	μA	
SWITCHING SPECIFICATIONS						
Noise Figure	$f = 100\text{kHz}, R_S = 500\Omega, I_C = 1\text{mA}$	-	2.2	-	dB	
Gain-Bandwidth Product	$V_{CE} = 6\text{V}, I_C = 5\text{mA}$	-	1.15	-	GHz	
Collector-to-Base Capacitance	$V_{CB} = 6\text{V}, f = 1\text{MHz}$	-	See Fig. 5	-	pF	
Collector-to-Substrate Capacitance	$V_{CI} = 6\text{V}, f = 1\text{MHz}$	-		-	pF	
Emitter-to-Base Capacitance	$V_{BE} = 4\text{V}, f = 1\text{MHz}$	-		-	pF	
Voltage Gain	$V_{CE} = 6\text{V}, f = 10\text{MHz}, R_L = 1\text{k}\Omega, I_C = 1\text{mA}$	-	28	-	dB	
Power Gain	Cascode Configuration	27	30	-	dB	
Noise Figure	$f = 100\text{MHz}, V_+ = 12\text{V}, I_C = 1\text{mA}$	-	3.5	-	dB	
Input Resistance	Common-Emitter Configuration $V_{CE} = 6\text{V}, I_C = 1\text{mA}, f = 200\text{MHz}$	-	400	-	Ω	
Output Resistance		-	4.6	-	k Ω	
Input Capacitance		-	3.7	-	pF	
Output Capacitance		-	2	-	pF	
Magnitude of Forward Transadmittance		-	24	-	mmho	

NOTE:

1. The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. When used as a zener for reference voltage, the device must not be subjected to more than 0.1mJ of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10mA.

Typical Performance Curves

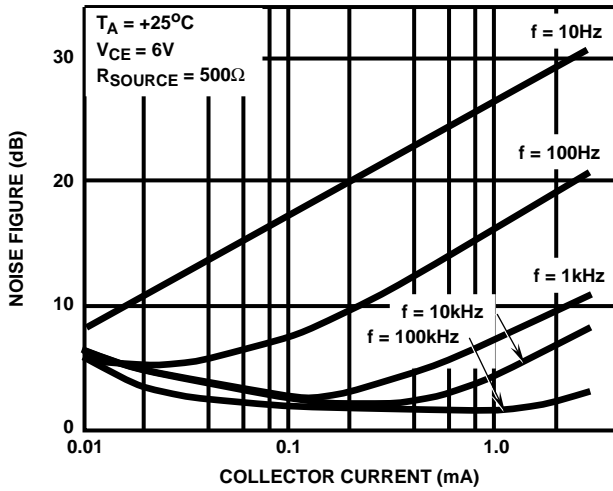


FIGURE 1. NOISE FIGURE vs COLLECTOR CURRENT AT $R_{SOURCE} = 500\Omega$

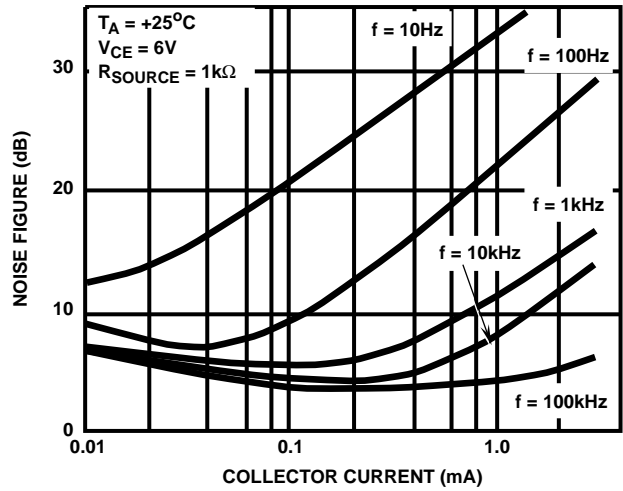


FIGURE 2. NOISE FIGURE vs COLLECTOR CURRENT AT $R_{SOURCE} = 1k\Omega$

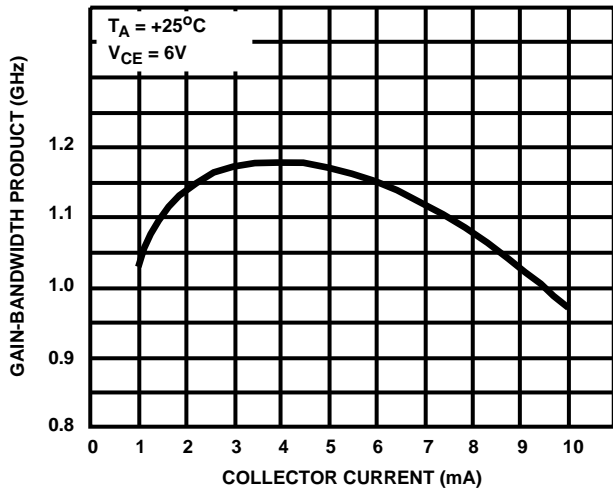


FIGURE 3. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT

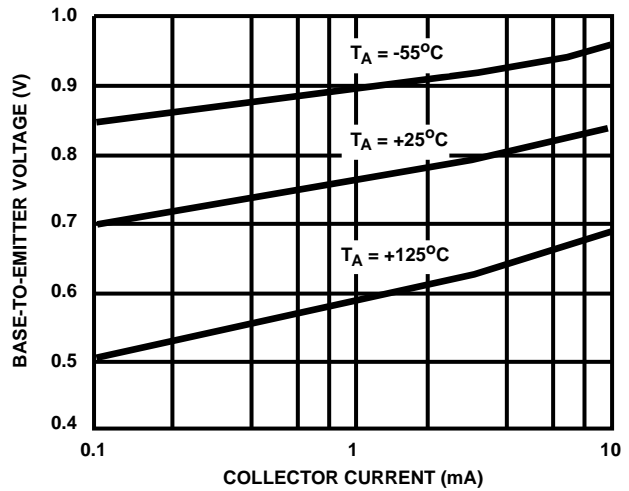


FIGURE 4. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

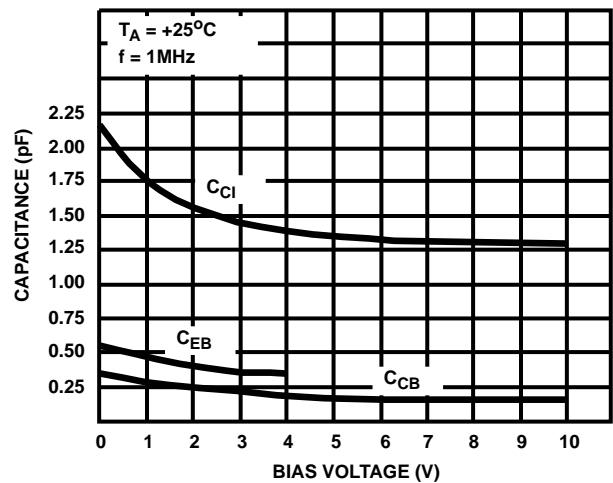


FIGURE 5A. CAPACITANCE vs BIAS VOLTAGE FOR Q2

TRAN- SISTOR	CAPACITANCE (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	PKG	TOTAL	PKG	TOTAL	PKG	TOTAL	PKG	TOTAL
BIAS (V)	-	6V	-	6V	-	4V	-	6V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

FIGURE 5B. TYPICAL CAPACITANCE VALUES AT $f = 1MHz$. THREE TERMINAL MEASUREMENT. GUARD ALL TERMINALS EXCEPT THOSE UNDER TEST.

Typical Performance Curves (Continued)

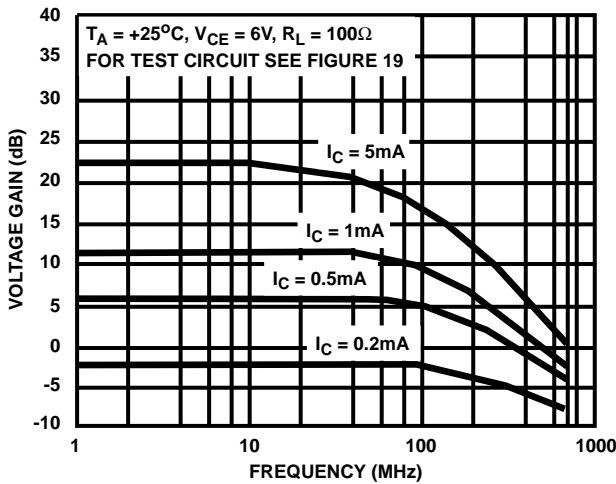


FIGURE 6. VOLTAGE GAIN vs FREQUENCY AT $R_L = 100\Omega$

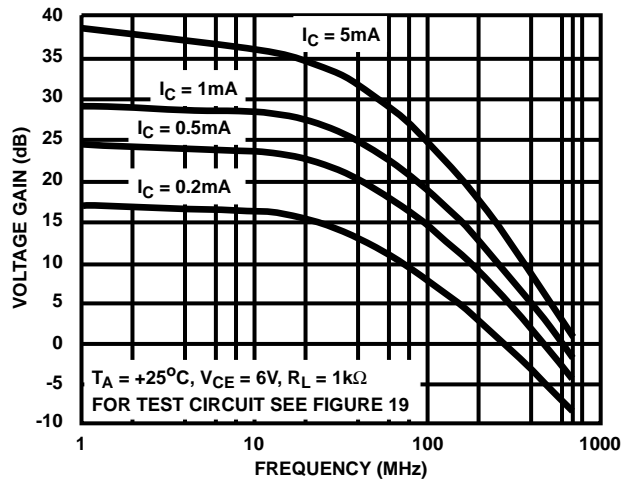


FIGURE 7. VOLTAGE GAIN vs FREQUENCY AT $R_L = 1k\Omega$

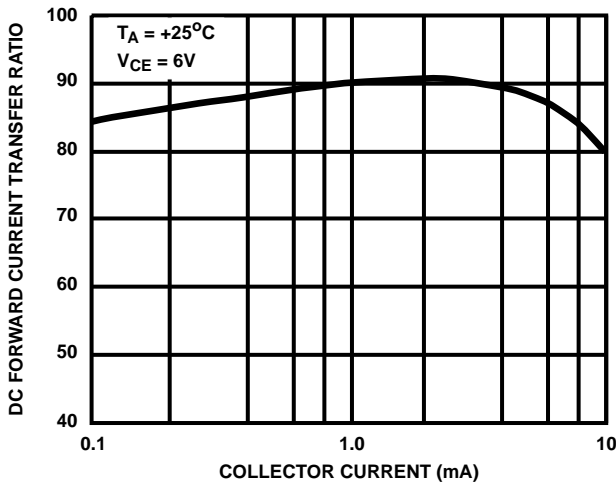


FIGURE 8. DC FORWARD-CURRENT TRANSFER RATIO (h_{FE}) vs COLLECTOR CURRENT

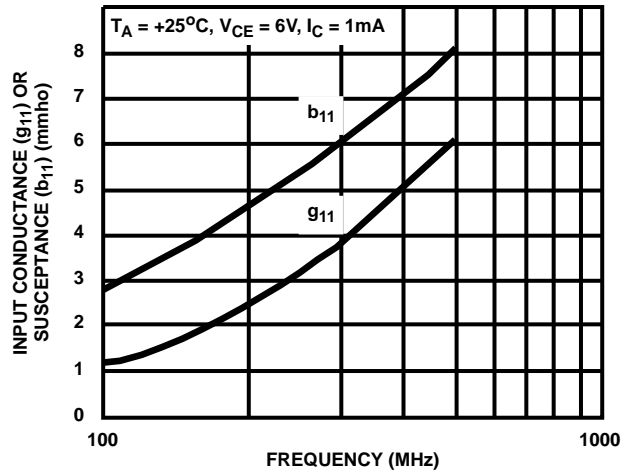


FIGURE 9. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

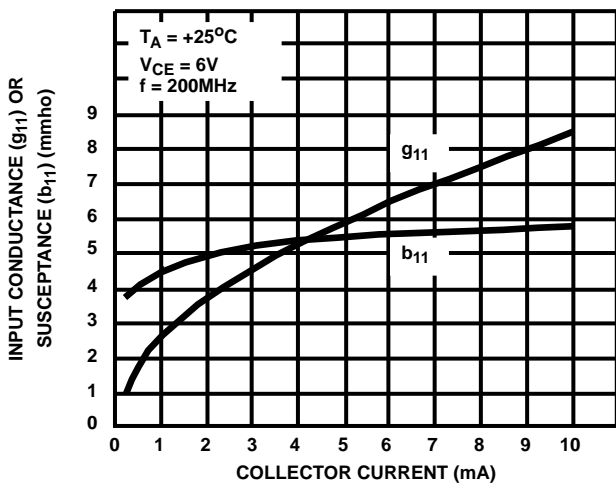


FIGURE 10. INPUT ADMITTANCE (Y_{11}) vs COLLECTOR CURRENT

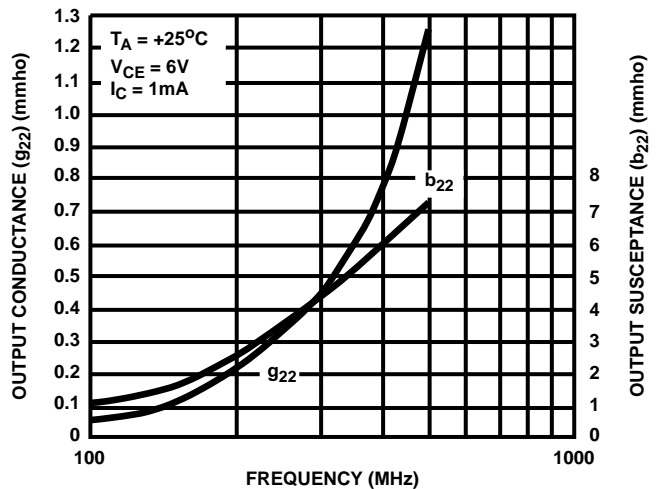


FIGURE 11. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

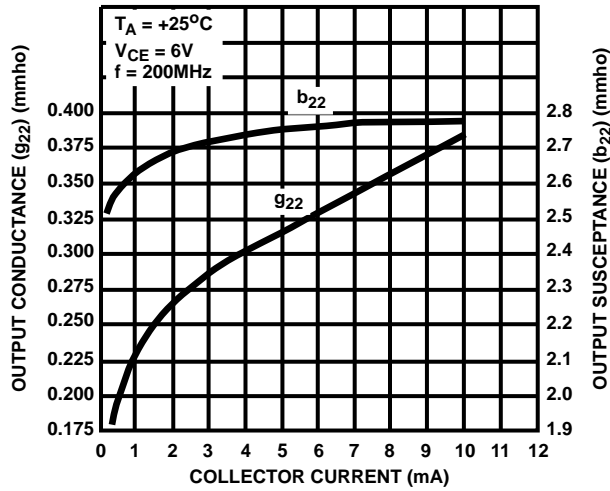


FIGURE 12. OUTPUT ADMITTANCE (Y_{22}) vs COLLECTOR CURRENT

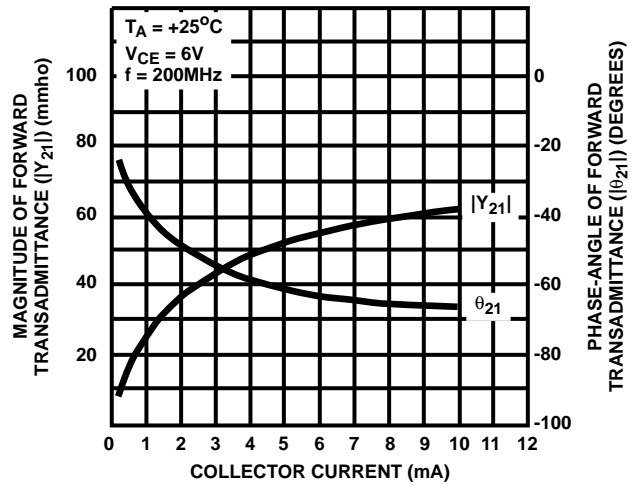


FIGURE 13. FORWARD TRANSADMITTANCE (Y_{21}) vs COLLECTOR CURRENT

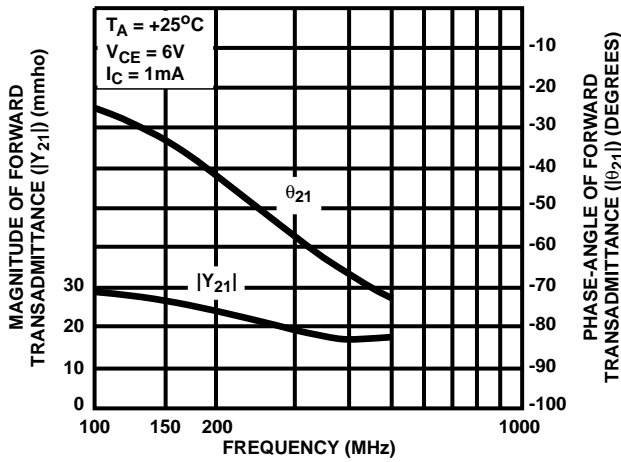


FIGURE 14. FORWARD TRANSADMITTANCE (Y_{21}) vs FREQUENCY

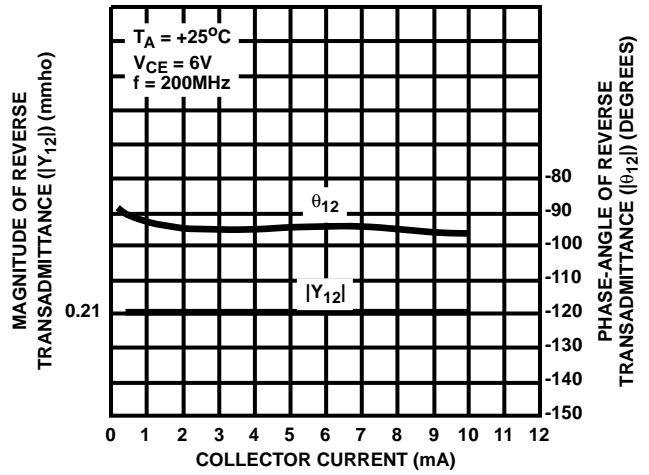


FIGURE 15. REVERSE TRANSADMITTANCE (Y_{12}) vs COLLECTOR CURRENT

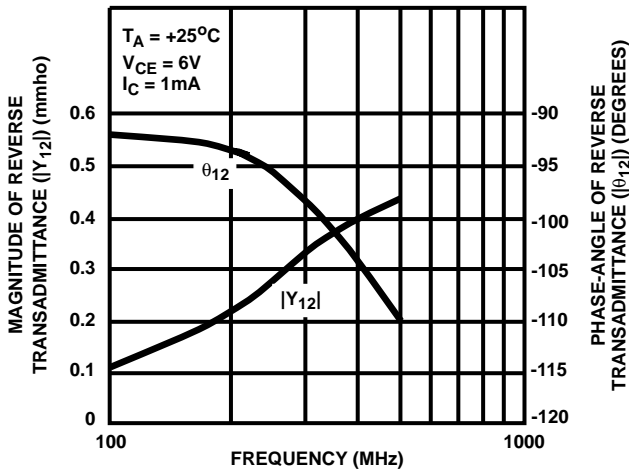


FIGURE 16. REVERSE TRANSADMITTANCE (Y_{12}) vs FREQUENCY

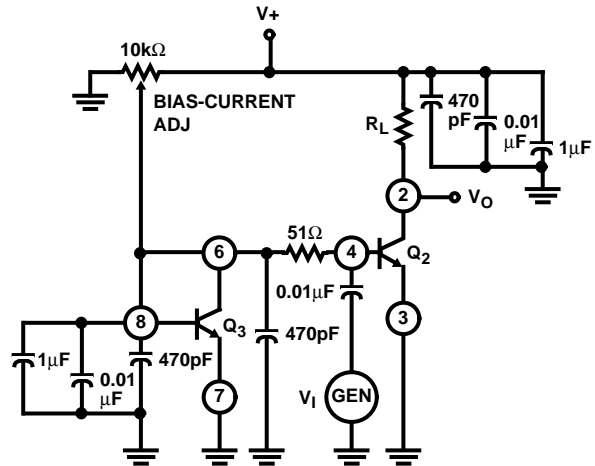
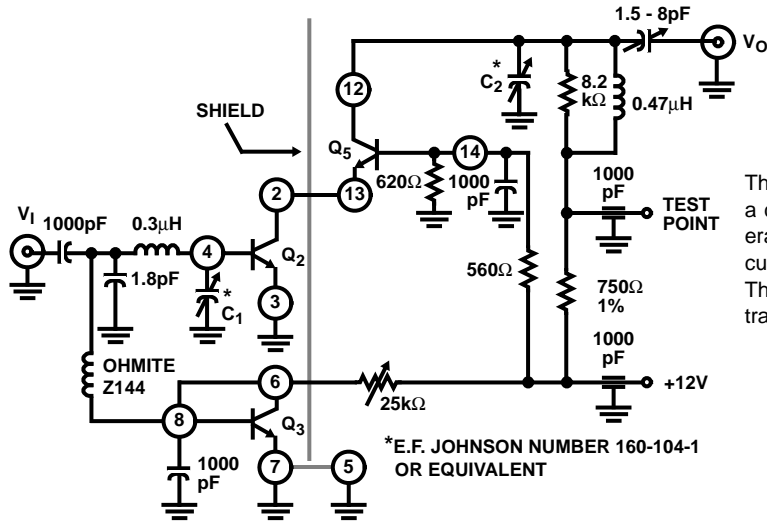


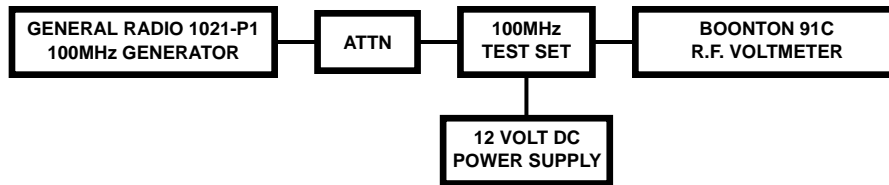
FIGURE 17. VOLTAGE-GAIN TEST CIRCUIT USING CURRENT-MIRROR BIASING FOR Q_2

Typical Performance Curves (Continued)

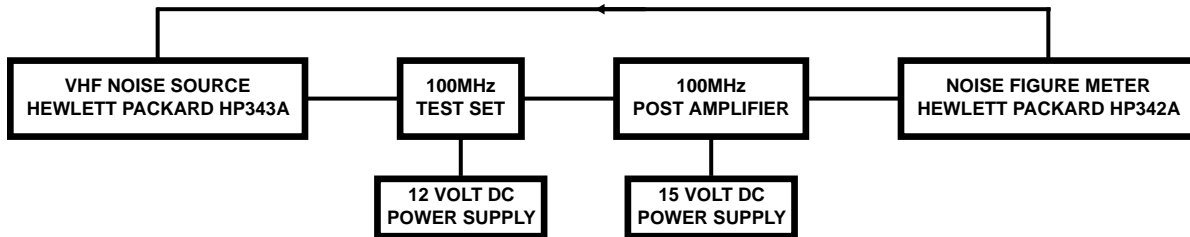


This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

FIGURE 18. 100MHz POWER-GAIN AND NOISE-FIGURE TEST CIRCUIT



(a) POWER GAIN SET-UP



(b) NOISE FIGURE SET-UP

FIGURE 19. BLOCK DIAGRAMS OF POWER-GAIN AND NOISE-FIGURE TEST SET-UPS