Audio sound controller
BH3864F

The BH3864F has been developed for use in mini-component stereo systems. Switching is done using a resistor ladder to suppress DC offset at switching. Two-line serial control is available, and external three-line serial control is also possible. The package is a compact 24-pin SOP.

●Applications

Mini- and micro-component stereo systems, CD radio cassette players and TVs.

●Features

1) Volume, tone, and dynamic bass boost control possible by a serial link to a microprocessor.
2) Left and right channel volume can be controlled independently.
3) Resistor-ladder type volume control uses BiCMOS process for low distortion and noise.
4) Dynamic bass and linked ALC are provided on chip.

●Absolute maximum ratings (Ta = 25℃)

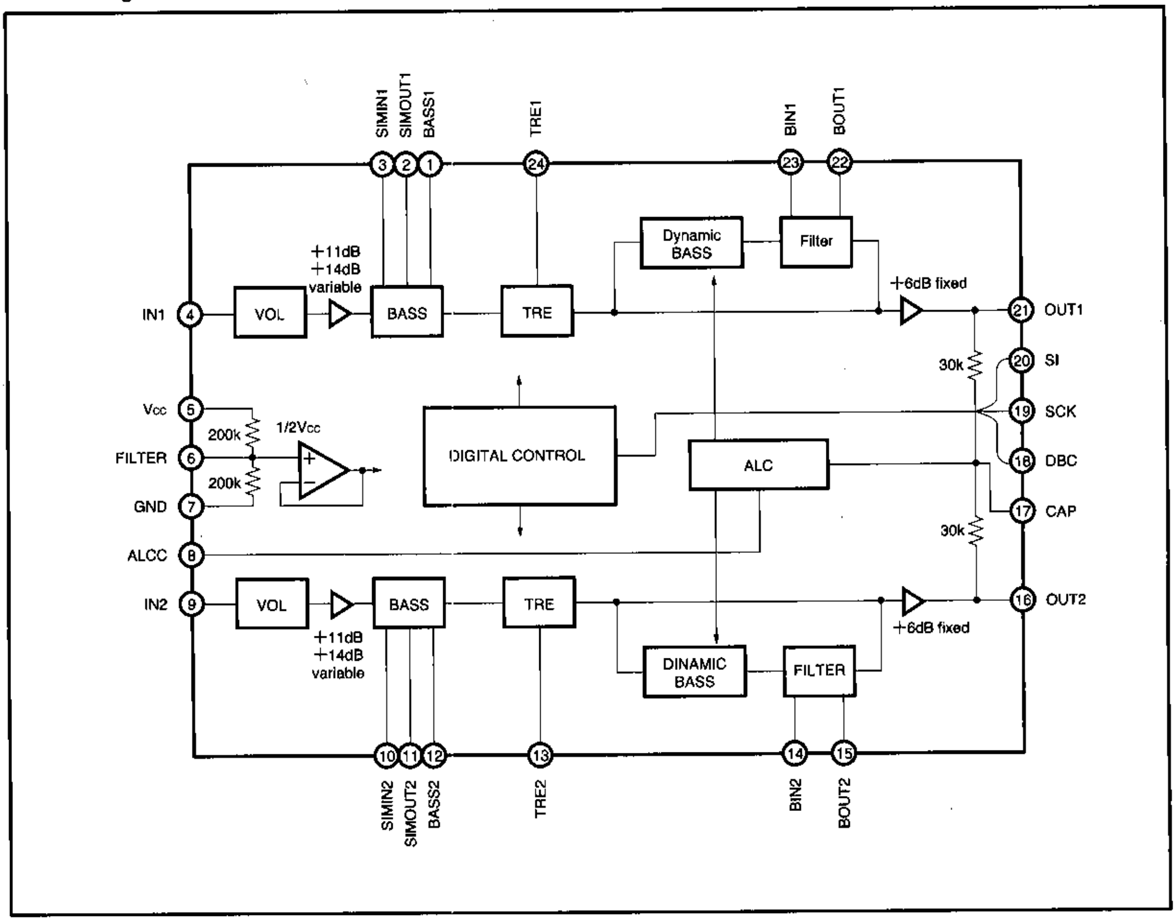
Parameter	Symbol	Limits	Unit
Applied voltage	Vcc	−0.3~10.0	V
Power dissipation	Pd	550 *	mW
Operating temperature	Topr	−40~+85	℃
Storage temperature	Tstg	−55~+125	℃

* Reduced by 5.5mW for each increase in Ta of 1°C over 25°C when mounted on a 50mm x 50mm x 1.6mm board.

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	7.0	9.0	9.5	V

●Block diagram



●Pin descriptions

Pin No.	Symbol	Function
1	BASS1	Channel 1 bass filter setting terminal
2	SIMOUT1	Channel 1 bass filter setting terminal
3	SIMIN1	Channel 1 bass filter setting terminal
4	IN1	Channel 1 signal input terminal
5	Vcc	Power supply terminal
6	FILTER	Filter terminal
7	GND	Ground terminal
8	ALCC	ALC attack and release time setting terminal
9	IN2	Channel 2 signal input terminal
10	SIMIN2	Channel 2 bass filter setting terminal
11	SIMOUT2	Channel 2 bass filter setting terminal
12	BASS2	Channel 2 bass filter setting terminal
13	TRE2	Channel 2 treble filter setting terminal
14	BIN2	Channel 2 dynamic bass filter setting terminal
15	BOUT2	Channel 2 dynamic bass filter setting terminal
16	OUT2	Channel 2 signal output terminal
17	CAP	ALC trap frequency setting terminal
18	DBC	Dynamic bass switch retiming setting terminal
19	SCK	Serial clock input terminal
20	SI	Serial data input terminal
21	OUT1	Channel 1 signal output terminal
22	BOUT1	Channel 1 dynamic bass filter setting terminal
23	BIN1	Channel 1 dynamic bass filter setting terminal
24	TRE1	Channel 1 treble filter setting terminal

●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 9V, f = 1kHz, Rg = 600Ω, R_L = 10kΩ, BW = 20Hz to 20kHz, VIN = 200mVrms, volume = 0dB, tone = 0dB, dynamic bass = 0dB, and gain select = 14dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	—	11	22	mA	V_{IN}=0Vrms
Maximum input voltage	V_{IM}	2.2	2.5	—	Vrms	ATT = −30dB, output THD = 1%
Maximum output voltage	V_{OM}	2.2	2.5	—	Vrms	Output THD = 1%, BW = 400Hz to 30kHz
Voltage gain	G_V	18	20	22	dB	
Total harmonic distortion	THD	—	0.01	0.05	%	V_O=1Vrms
Output noise conversion voltage	V_{NO}	—	25	40	μVrms	Rg=0Ω *
Residual noise voltage	V_{MNO}	—	25	40	μVrms	Volume = −infinity *
Crosstalk	CT	—	94	60	dB	
Channel balance	CB	−1.5	0	1.5	dB	CH1 standard measuring
Input impedance	R_{IN1}	7.5	9.4	11.3	kΩ	
Input impedance	R_{IN2}	10.6	13.3	16.0	kΩ	ATT=−3dB (−45dB)
Ripple rejection	RR	—	−40	−35	dB	f_{RR}=100Hz, V_{RRIN}=100mVrms
Volume step resolution	AT_{STEP}	—	1	—	dB	
Maximum volume attenuation	AT_{MIN}	−80	−94	—	dB	
Volume step error	AT_{ERR}	—	0	—	dB	
Bass control range	VB	±8.5	±10.5	±12.5	dB	
Treble control range	VT	±8	±10	±12	dB	
Tone step resolution	V_{STEP}	—	2	—	dB	
Dynamic bass control range	VDB	18	20	22	dB	f=60Hz, V_{IN}=10mVrms
Dynamic bass step resolution	VD_{STEP}	—	5	—	dB	
Current from logic terminals when "L"	I_D	—	1	10	μA	

* Measured using a Matsushita Comminucation Industry VP-9690A (average value detector, effective value display) IHF-A filter.
Operating specifications: same phase for the input and output signals.
◎Circuit not designed for radiation resistance.

●Measurement circuit

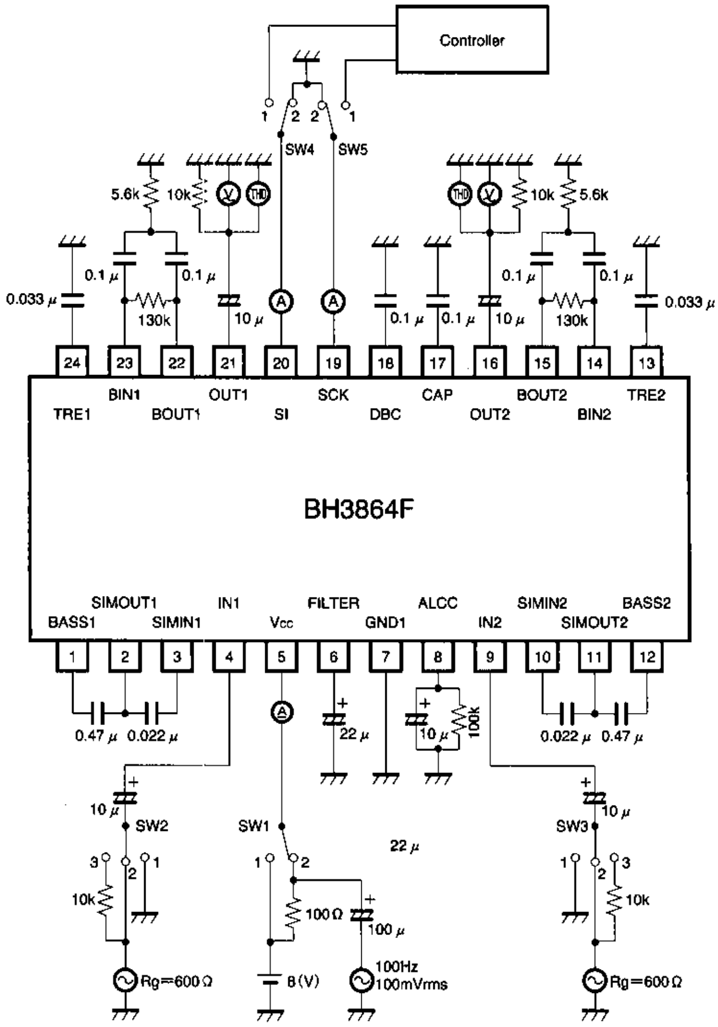


Fig. 1

●Circuit operation

(1) About the data format

As shown in Fig. 2, there are 28 bits of data. There are two chip select bits, but multiple units cannot be controlled by a single controller.

MSB D0 — 28bit total — D27 LSB

Gain	Dynamic bass	Treble	Bass	CH2 volume A	CH2 volume B	CH1 volume A	CH1 volume B	Chip select
1bit	3bit	4bit	4bit	5bit	2bit	5bit	2bit	2bit

(2) SCK and SI signal timing

The SCK and SI signal timing are shown in Fig. 3. The SI signal potential level decision is made internally. A Schmitt trigger circuit on the chip is used to provide noise margin. The internal circuits are bipolar, so take care with regard to source current.

The data is read in on the rising edge of the clock.

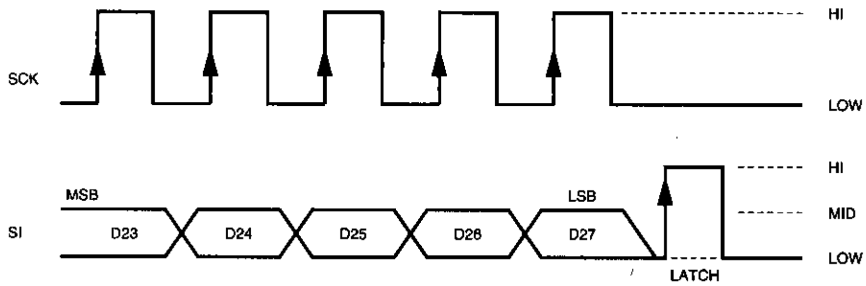
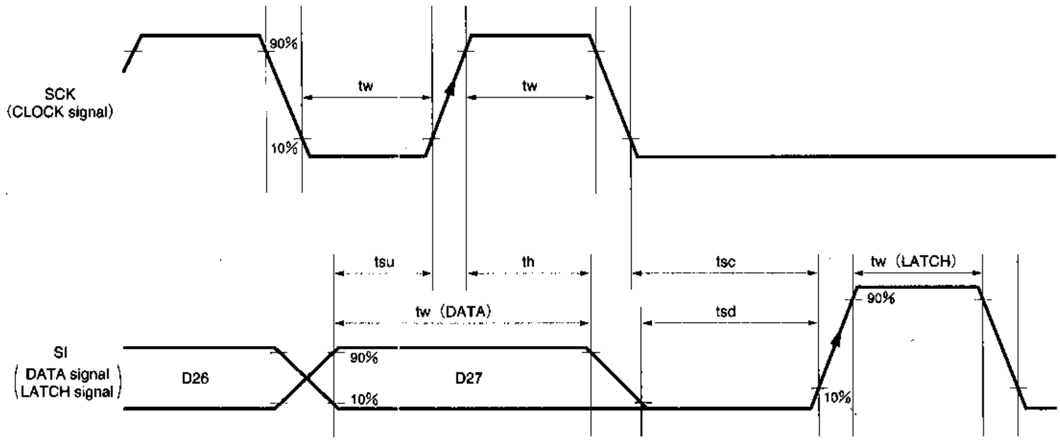


Fig. 3

(3) Timing chart
The timing chart is shown in Fig. 4.

Serial data timing



* When SI is "H", the DATA signal is forced "L" internally, and data is not accepted.

Fig. 4

Timing chart constants (Ta = 25℃, V_{CC} = 9V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
H input voltage	V_{IH}	4.0	5.0	6.0	V
M input voltage	V_{IM}	2.0	2.5	3.0	V
L input voltage	V_{IL}	−0.3	0	1.0	V
Minimum clock width	tw	2.0	—	—	μS
Minimum data width	tw (DATA)	4.0	—	—	μS
Minimum latch width	tw (LATCH)	2.0	—	—	μS
Setup time (DATA to CLK)	tsu	1.0	—	—	μS
Hold time (CLK to DATA)	th	1.0	—	—	μS
Setup time (CLK to LATCH)	tsc	1.0	—	—	μS
Setup time (DATA to LATCH)	tsd	1.0	—	—	μS

(4) Data table
The transmission data is given in the table below.

VOLUME ATTENUATION
Volume A

GAIN	CH1	D19	D20	D21	D22	D23
	CH2	D12	D13	D14	D15	D16
0dB		0	0	0	0	0
−2dB		0	0	0	0	1
−4dB		0	0	0	1	0
−6dB		0	0	0	1	1
−8dB		0	0	1	0	0
−10dB		0	0	1	0	1
−12dB		0	0	1	1	0
−14dB		0	0	1	1	1
−16dB		0	1	0	0	0
−18dB		0	1	0	0	1
−20dB		0	1	0	1	0
−22dB		0	1	0	1	1
−24dB		0	1	1	0	0
−26dB		0	1	1	0	1
−28dB		0	1	1	1	0
−30dB		0	1	1	1	1
−32dB		1	0	0	0	0
−34dB		1	0	0	0	1
−36dB		1	0	0	1	0
−38dB		1	0	0	1	1
−40dB		1	0	1	0	0
−42dB		1	0	1	0	1
−46dB		1	0	1	1	0
−50dB		1	0	1	1	1
−54dB		1	1	0	0	0
−58dB		1	1	0	0	1
−62dB		1	1	0	1	0
−66dB		1	1	0	1	1
−70dB		1	1	1	0	0
−74dB		1	1	1	0	1
−78dB		1	1	1	1	0
−∞		1	1	1	1	1

Volume B

GAIN	CH1	D24	D25
	CH2	D17	D18
0dB		0	0
−1dB		0	1
−2dB		1	0
−3dB		1	1

(The −2dB and −3dB settings operate when the setting is −42dB or lower.)

By combining volume A and B, it is possible to provide control from 0dB to −81dB in 1dB steps.

BASS AND TREBLE (TONE CONTROL)

GAIN	BASS			
	D4	D5	D6	D7
+10.5dB	1	1	0	1
+8dB	1	1	0	0
+6dB	1	0	1	1
+4dB	1	0	1	0
+2dB	1	0	0	1
0dB	1	0	0	0
0dB	0	0	0	0
−2dB	0	0	0	1
−4dB	0	0	1	0
−6dB	0	0	1	1
−8dB	0	1	0	0
−10.5dB	0	1	0	1

GAIN	TREBLE			
	D8	D9	D10	D11
+10dB	1	1	0	1
+8dB	1	1	0	0
+6dB	1	0	1	1
+4dB	1	0	1	0
+2dB	1	0	0	1
0dB	1	0	0	0
0dB	0	0	0	0
−2dB	0	0	0	1
−4dB	0	0	1	0
−6dB	0	0	1	1
−8dB	0	1	0	0
−10dB	0	1	0	1

Note: Gain is the name given to the transfer data. Depending on the values of the external components, the specified gain may not be output.

DYNAMIC BASS BOOST

GAIN	D1	D2	D3
0dB	0	0	0
5dB	0	0	1
10dB	0	1	0
15dB	0	1	1
20dB	1	0	0

Note: Gain is the name given to the transfer data. Depending on the values of the external components, the specified gain may not be output.

CHIP SELECT

D26	D27
1	1

Note: For all other data, the previous data are maintained.

GAIN SELECT

INPUT AMP GAIN	D0
11dB	1
14dB	0

●Application example

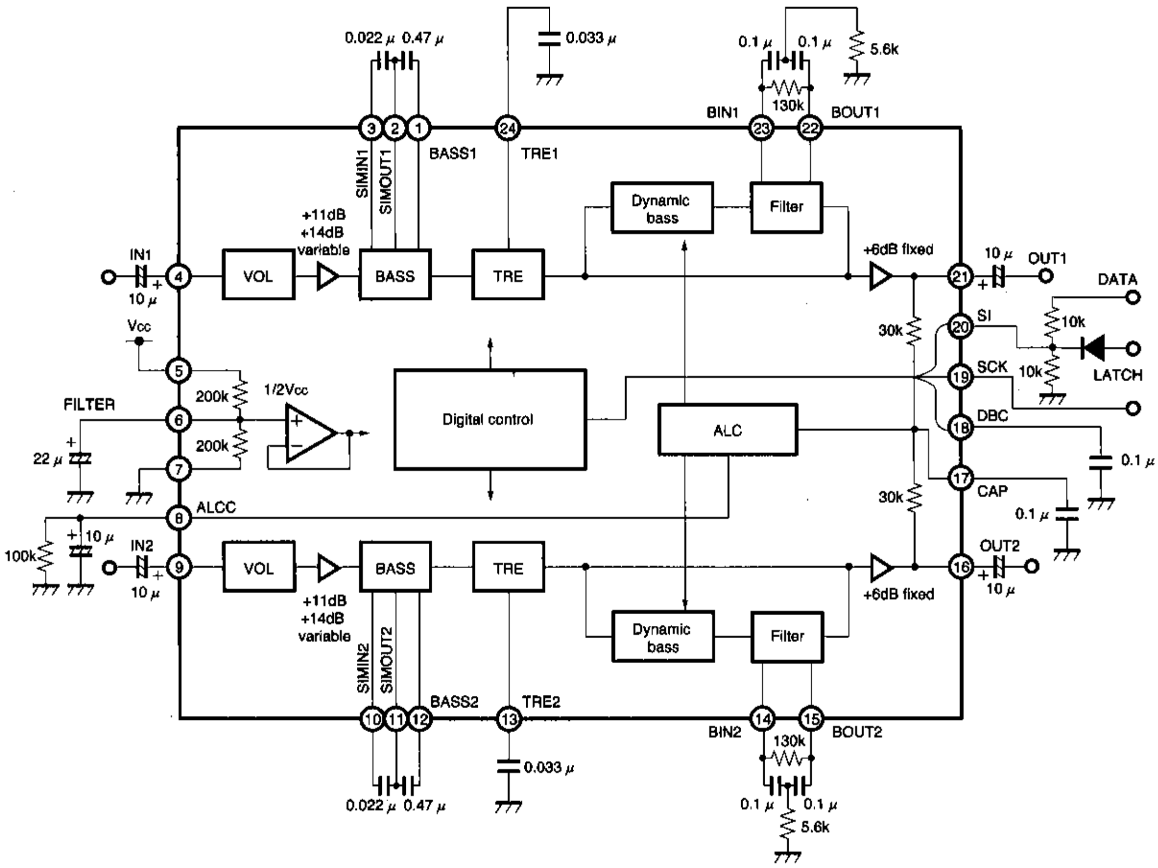


Fig. 5

●External components

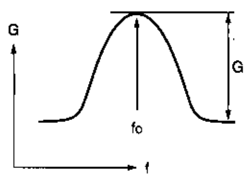
(1) Tone control filter constants

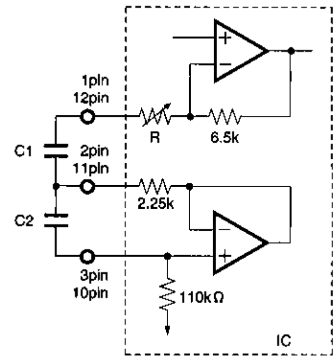
Bass region

$$f_o = \frac{1}{2\pi\sqrt{110k \times 2.25k \times C_1 \times C_2}} \quad \text{(Hz)}$$

$$Q = \sqrt{\frac{110k \times C_2}{2.25k \times C_1}}$$

$$G = 20 \log \left(\frac{2.25k + R + 6.5k}{2.25k + R} \right) \quad \text{(dB)}$$





Equivalent circuit diagram

Note: The variables C_1, C_2 and R in the formulas are the components in the equivalent circuit.

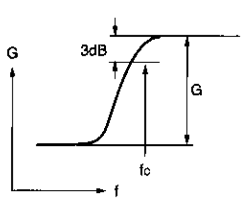
Bass control data	R(kΩ)
±10.5dB	0
±8dB	1.95
±6dB	4.5
±4dB	9.0
±2dB	23.0
±0dB	∞

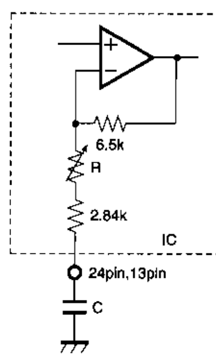
The actual gain may vary somewhat.

Treble

$$f_c = \frac{1}{2\pi \times 2.84k \times C} \quad \text{(Hz)}$$

$$G = 20 \log \left(\frac{2.84k + R + 6.5k}{2.84k + R} \right) \quad \text{(dB)}$$





Equivalent circuit diagram

Note: The variables C and R in the formulas are the components in the equivalent circuit. The internally-fixed settings for R are as follows.

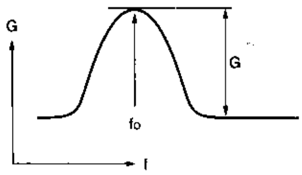
Treble control data	R(kΩ)
±10dB	0
±8dB	1.34
±6dB	3.6
±4dB	8.22
±2dB	22
±0dB	∞

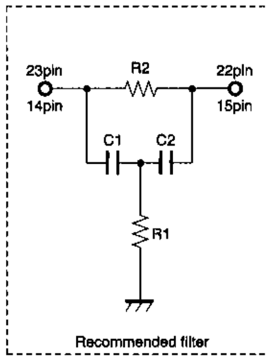
The actual gain may vary somewhat.

(2) Dynamic bass filter constants

$$fo = \frac{1}{2\pi\sqrt{R_1 \times R_2 \times C_1 \times C_2}} \quad (Hz)$$

$$G = 20\log\left(1 + \frac{55g}{1+54t}\right) \quad (dB)$$





Note: R_1, R_2, C_1 and C_2 are the recommended values for the filter. g is fixed internally (see the table below).

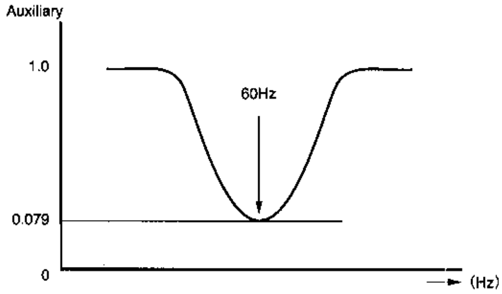
Dynamic bass control data	g
20dB	1
15dB	0.5
10dB	0.25
5dB	0.085
0dB	0

Constants in formulas

The variable "t" in the formula depends on the filter. For the recommended filter, the relationship is as follows.

$$t = 1 - \frac{1}{1+\frac{R_1}{R_2}\left(1+\frac{C_1}{C_2}\right)}$$

For the application circuit example, t = 0.079.



Recommended filter characteristics

The actual gain may vary slightly.

(3) ALC (automatic level control)

1) Trap frequency T_f

The trap frequency T_f is obtained from the following formula.

$$T_f = \frac{1}{2\pi \times 10k \times C} \quad (Hz)$$

Note: C is the value of the capacitance between pin 17 and GND.

2) Trap level

The signal level at which the ALC begins to operate depends on V_{CC}. The relationship is given below (T_L = trap level).

$$T_L = \frac{V_{CC}}{9} \quad (Vrms) \quad \text{(same phase input)}$$

Note: It is possible to switch ALC off permanently by connecting pin 8 to GND.

●Operation notes

We guarantee the application circuit design, but recommend that you thoroughly check its characteristics and pay attention to the points of caution given below. If you change any of the external component values, check both the static and transient characteristics of the circuit, and allow sufficient margin in your selections to take into account variations in the components and ICs.

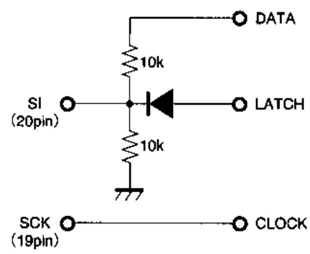
(1) Supply voltage range

The basic circuit functions are guaranteed to operate if the circuit is operated within the recommended temperature and supply voltage ranges. Please confirm the values of the circuit constants, voltage setting, and temperature in actual use.

(2) Serial control

High-frequency digital signals are input to the SI and SCK pins. Ensure that the wiring is done in such a way as to prevent interference with the analog signal lines. If noise is measured during step switching, connect resistors of about 2k Ω in series with and close to the microprocessor outputs.

If you plan to use the conventional three-line serial method, we recommend that you used the following circuit (as shown in the application example circuit).



The diode should have as low a V_F as possible.
Adjust the value of the resistors depending on the drive capacity of the microprocessor.

(3) Dynamic bass step switching noise
A capacitor is shown connected to DBC (pin 18) in the application circuit example. The value of this component varies with the signal level setting and PCB pattern. Investigate carefully before deciding on the values of the various circuit constants.

●Electrical characteristic curves

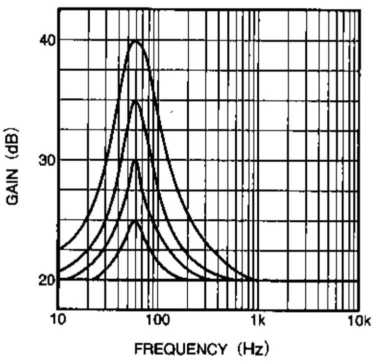


Fig. 6 Dynamic bass frequency characteristics

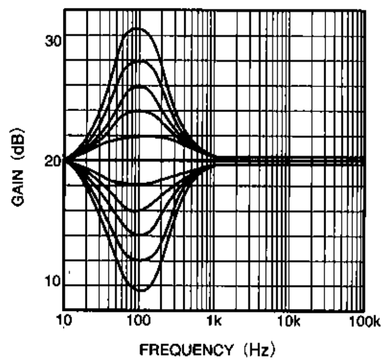


Fig. 7 Bass frequency characteristics

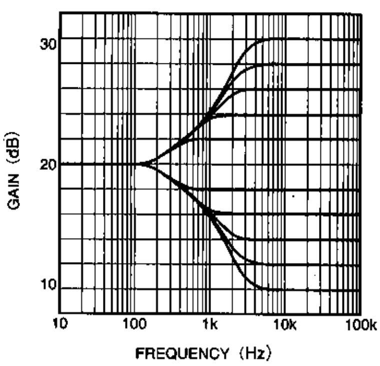
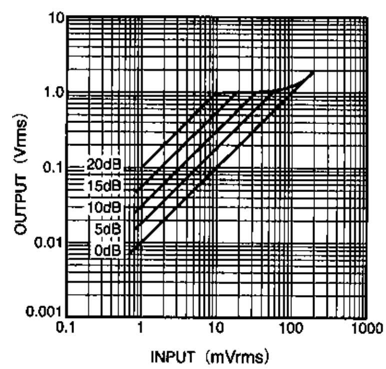


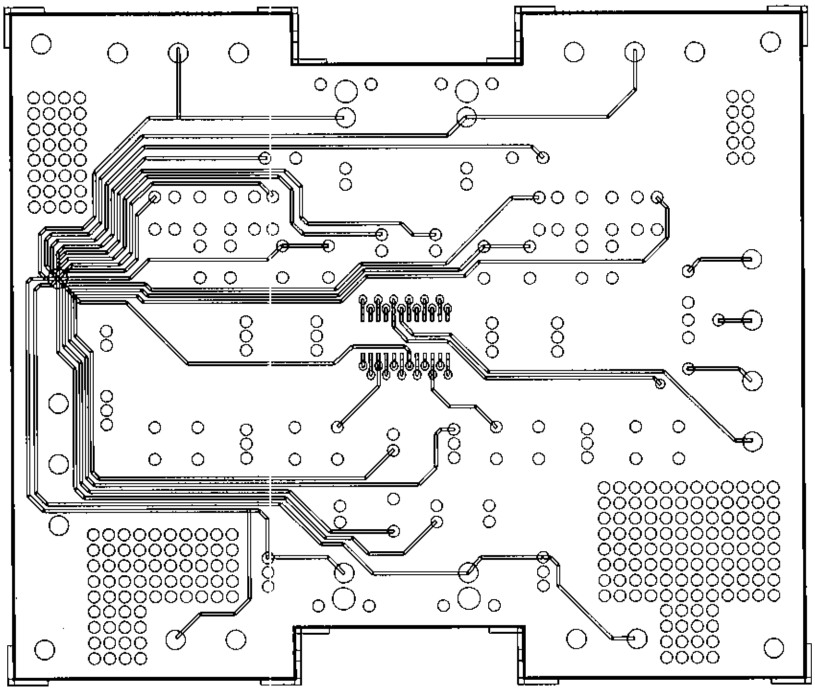
Fig. 8 Treble frequency characteristics

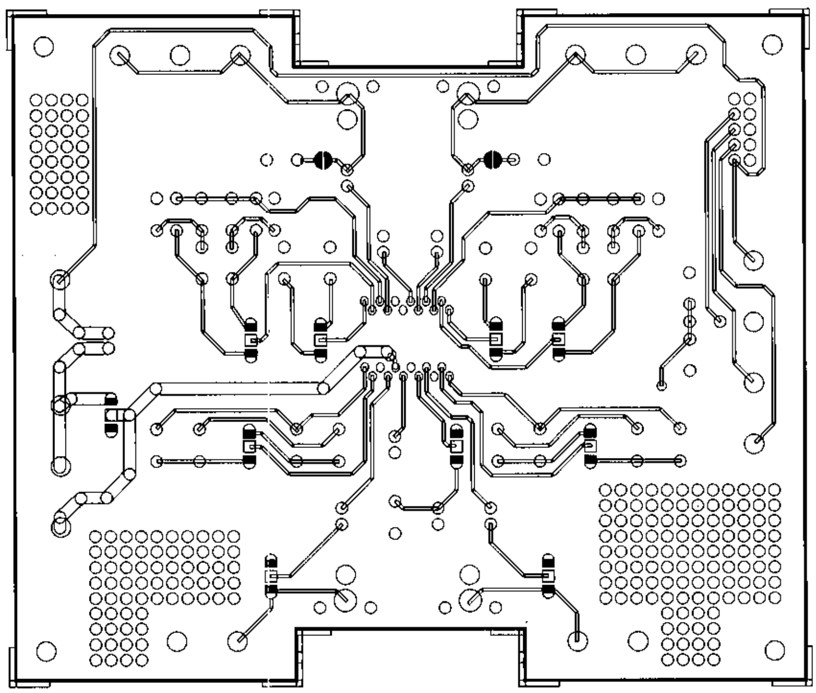


(the gain is the amount of dynamic bass boost)

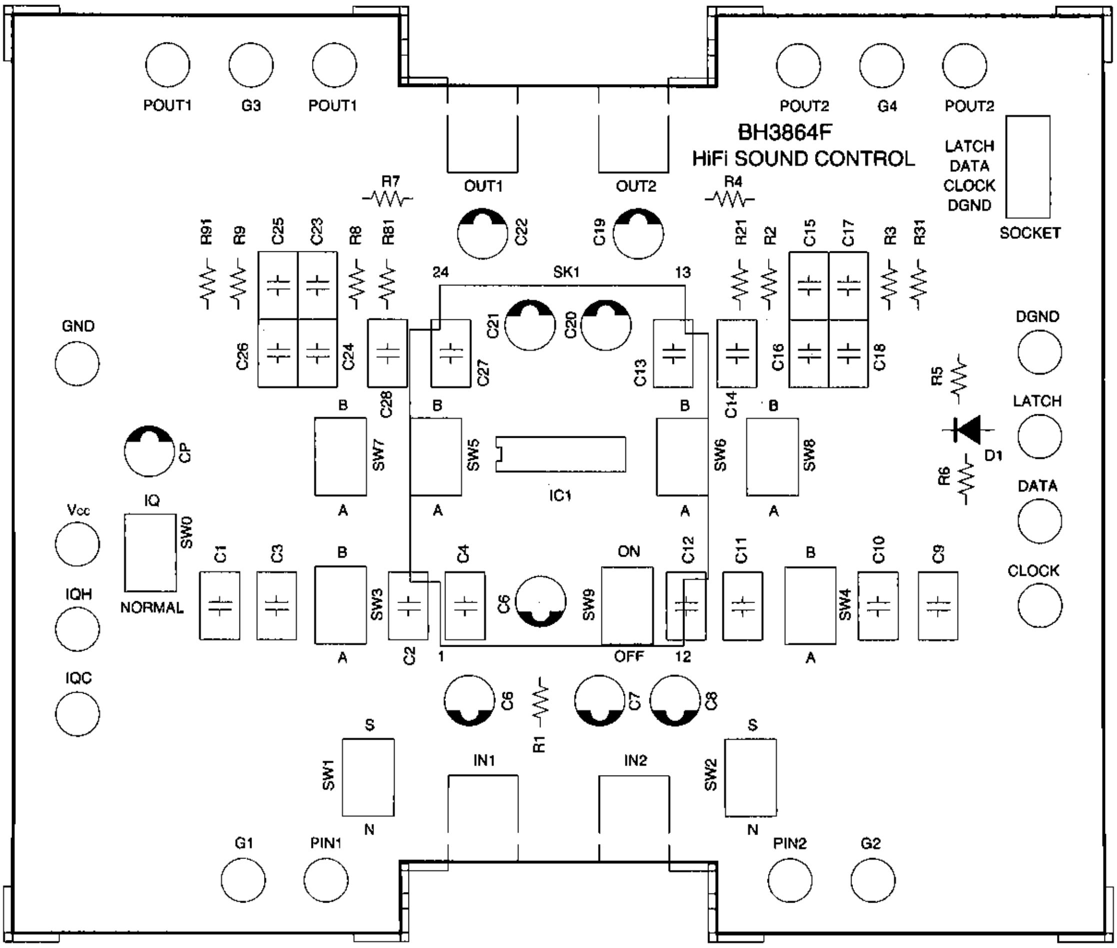
Fig. 9 ALC characteristics

●Application example circuit PCB

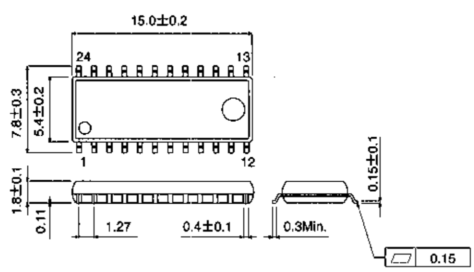




● Application example circuit component layout



● External dimensions (Unit: mm)



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