

Active Errata List

- SPI SSDIS Does Not Work
- Baud Rate Generator Idle Mode
- During UART Reception, Clearing REN May Generate Unexpected IT
- Double IT on External Falling Edge on INT1 or INT2 in X2 Mode

Errata History

Lot Number	Errata List
All date codes, starting May 2002	1, 2, 3, 4

Errata Descriptions

1. SPI SSDIS Does Not Work

The SSDIS bit in SPCON register does not work; therefore the \overline{SS} pin cannot be used as a general-purpose I/O when the SPI is used.

Workaround

None.

2. BRG Idle Mode

The BRG clock is stopped in Idle and Pseudo Idle modes.

Workaround

None. When using the BRG, use the standard conversion, the A/D resolution is nearly as good as in pseudo Idle mode.

3. During UART Reception, Clearing REN May Generate Unexpected IT

During UART reception, if the REN bit is clear between a start bit detection and the end of reception, the UART will not discard the data (RI is set).

Workaround

Test REN at the beginning of Interrupt routine just after CLR RI, and run the interrupt routine code only if REN is set.

4. Double IT on External Falling Edge on INT1 or INT2 in X2 Mode

When the CPU is in X2 mode and Timer1 or Timer0 in X1 mode (CKCON = 0x7F), IEx flag is not cleared by hardware after servicing the interrupt. In this case, the CPU executes the ISR a second time.

Workaround

The workaround is to clear IEx bit in the interrupt subroutine.

```
INT1_ISR: ; Interrupt subroutine
```

```
    CLR IE1
```

```
    .....
```



80C51 Microcontrollers

AT83C5111
AT87C5111
AT83C5112
AT87C5112
AT80C5112

Errata Sheet





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