

**0.5 Micron CMOS Pad Library  
Datasheets  
AMI500HXPM 5.0 Volt  
Section 4  
Revision 1.1**



### Input Drive Pieces

Name	Description	Page
IDCI3	Inverting, CMOS-level input buffer piece .....	4-5
IDCR0	Non-buffered, resistive analog interface input piece with ESD protection .....	4-6
IDCS3	Non-inverting, CMOS-level Schmitt trigger input buffer piece .....	4-7
IDCXx	Family of non-inverting, CMOS-level input buffer pieces .....	4-8
IDPX3	Non-inverting, PCI-level input buffer piece .....	4-9
IDQC0	Non-buffered, resistive crystal oscillator input receiver piece with ESD protection .....	4-10
IDQC3	Crystal oscillator input receiver pad piece with a non-inverting, CMOS-level input .....	4-11
IDQS3	Crystal oscillator input receiver pad piece .....	4-13
IDTS3	Non-inverting, TTL-level Schmitt input buffer piece .....	4-15
IDTXx	Family of non-inverting, TTL-level input buffer piece .....	4-16

### Pull Pieces

PLD3	Active pull-down buffer piece .....	4-52
PLP3	programmable pull-up/pull-down buffer piece .....	4-53
PLU3	Active pull-up buffer piece .....	4-54

### Output Drive Pieces

ODCHXE12	12 mA non-inverting, CMOS-level, tristate output piece with active low enable outputs .....	4-17
ODCHXX12	12 mA non-inverting, CMOS-level output piece .....	4-18
ODCSIPxx	Family of 4 to 12 mA, inverting, CMOS-level output pieces with P-channel open-drains (pull-up) and controlled slew rate outputs .....	4-19
ODCSXExx	Family of 4 to 12 mA, non-inverting, CMOS-level, tristate output pieces with active low enables and controlled slew rate outputs .....	4-21
ODCSXXxx	Family of 4 to 12 mA, non-inverting, CMOS-level, output pieces w/slew rate outputs .....	4-23
ODCXIPxx	Family of 1 to 12 mA, inverting, CMOS-level, output pieces w/P-channel, open-drains (pull-up) .....	4-25
ODCXEXx	Family of 1 to 12 mA, non-inverting, CMOS-level, tristate output w/active low enables .....	4-27
ODCXXXxx	Family of 1 to 12 mA, non-inverting, CMOS-level output pieces .....	4-29
ODTHXE12	High performance, 12 mA, non-inverting, LVTTTL-level, tristate output buffer piece .....	4-38
ODTHXX12	High performance, 12 mA, non-inverting, LVTTTL-level output buffer piece .....	4-39
ODTSXExx	Family of 4 to 12 mA, non-inverting, LVTTTL-level, tristate w/ slew output buffer pieces .....	4-40
ODTSXNxx	Family of 4 to 12 mA, non-inverting, LVTTTL-level, open drain w/ slew output buffer pieces .....	4-42
ODTSXXxx	Family of 4 to 12 mA, non-inverting, LVTTTL-level, tristate w/ slew output buffer pieces .....	4-44
ODTXXExx	Family of 1 to 12 mA, non-inverting, LVTTTL-level, tristate output buffer pieces .....	4-46
ODTXXNxx	Family of 1 to 12 mA, non-inverting, LVTTTL-level, open drain output buffer pieces .....	4-48
ODTXXXxx	Family of 1 to 12 mA, non-inverting, LVTTTL-level, output buffer pieces .....	4-50

# Selection Guide



## AMI500HXPM 0.5 micron CMOS Pad Library

### Power Pad Cells

Name	Description	Page
PWRPAD	Generic power pad .....	4-55
GNDPAD	Generic ground pad .....	4-56

### Special Pad Cells

ODQFE01M	Fundamental mode, enabled crystal oscillator output for frequency range of 32 kHz - 1 MHz .....	4-31
ODQFE20M	Fundamental mode, enabled crystal oscillator output for frequency range of 1 MHz - 20 MHz .....	4-33
ODQTE60M	Third-overtone mode, enabled crystal oscillator output for frequency range of 20 - 60 MHz .....	4-35
ODQXXX00	Non-buffered, resistive analog crystal oscillator output pad piece with ESD protection .....	4-37
SHFTOUT	Mixed voltage single output for level-shifting from a 3.3 V core to a 5.0 V pad .....	4-57
SHFTOUTT	Mixed voltage dual output for level-shifting from a 3.3 V core to a 5.0 V pad .....	4-58

Pad  
Logic

# **DATASHEETS**



### Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> </tr> </tbody> </table>	PADM	QC	L	H	H	L	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC											
L	H											
H	L											
	Load											
PADM	4.90 pF											

### HDL Syntax

Verilog ..... IDCI3 *inst\_name* (QC, PADM);

VHDL..... *inst\_name*: IDCI3 port map (QC, PADM);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	16.522	nA
$EQL_{pd}$	12.7	Eq-load

See page 2-13 for power equation.

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

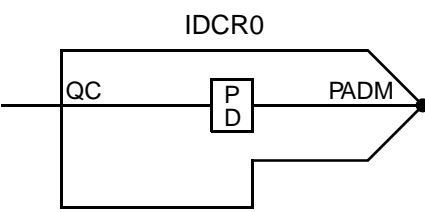
From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	$t_{PLH}$	0.602	0.728	0.811	0.873	0.931
			$t_{PHL}$	0.795	0.918	1.029	1.129	1.241

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC											
L	L											
H	H											
	Load											
PADM	4.90 pF											

### HDL Syntax

Verilog ..... IDCR0 *inst\_name* (QC, PADM);  
 VHDL ..... *inst\_name*: IDCR0 port map (QC, PADM);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	4.265	nA
$EQL_{pd}$	2.1	Eq-load

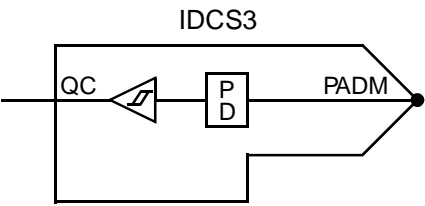
See page 2-13 for power equation.  
 Note: This special purpose, "resistive input" pad is not intended for use as a general input pad.



## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC											
L	L											
H	H											
	Load											
PADM	4.90 pF											

### HDL Syntax

Verilog ..... IDCS3 *inst\_name* (QC, PADM);

VHDL ..... *inst\_name*: IDCS3 port map (QC, PADM);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	15.963	nA
$EQL_{pd}$	17.0	Eq-load

See page 2-13 for power equation.

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	$t_{PLH}$	1.547	1.699	1.774	1.823	1.867
			$t_{PHL}$	0.969	1.162	1.305	1.407	1.503

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

## AMI500HXP 0.5 micron CMOS Pad Library

### Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H
PADM	QC						
L	L						
H	H						

### HDL Syntax

Verilog ..... IDCXx *inst\_name* (QC, PADM);

VHDL..... *inst\_name*: IDCXx port map (QC, PADM);

### Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.90	4.90

### Power Characteristics

Cell	Equivalent Gates	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
IDCX3	0.0	15.832	10.4
IDCX6	0.0	18.757	18.1

a. See page 2-13 for power equation.

### Propagation Delays (ns)

Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5.0V, Typical Process

IDCX3	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM	t <sub>PLH</sub>	0.788	0.871	0.972	1.068	1.177
To: QC	t <sub>PHL</sub>	0.524	0.695	0.833	0.941	1.051	
IDCX6	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM	t <sub>PLH</sub>	0.683	0.732	0.787	0.838	0.895
To: QC	t <sub>PHL</sub>	0.565	0.653	0.715	0.770	0.830	

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

IDPX3 is a non-inverting, PCI-level input buffer piece. IDPX3 is for the 33MHz PCI ODPSXE16 piece.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H
PADM	QC						
L	L						
H	H						

### HDL Syntax

Verilog ..... IDPX3 *inst\_name* (QC, PADM);  
 VHDL..... *inst\_name*: IDPX3 port map (QC, PADM);

### Pin Loading

Pin Name	Load
PADM (pF)	IDPX3 4.90

### Power Characteristics

Cell	Equivalent Gates	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
IDPX3	0.0	15.774	12.6

a. See page 2-13 for power equation.

### Propagation Delays (ns)

Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5.0V, Typical Process

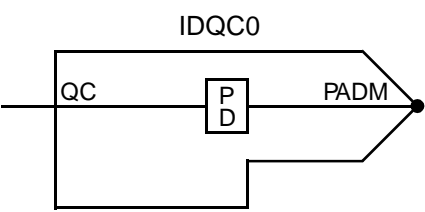
IDPX3	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM	To: QC	t <sub>PLH</sub>	t <sub>PLH</sub>	t <sub>PLH</sub>	t <sub>PLH</sub>	t <sub>PLH</sub>
			0.627	0.793	0.916	1.011	1.105
			0.702	0.852	0.964	1.050	1.135

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QO</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QO	L	L	H	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QO											
L	L											
H	H											
	Load											
PADM	4.90 pF											

### HDL Syntax

Verilog ..... IDQC0 *inst\_name* (QO, PADM);  
 VHDL..... *inst\_name*: IDQC0 port map (QO, PADM);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	4.265	nA
$EQL_{pd}$	2.1	Eq-load

See page 2-13 for power equation.

### Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS-level clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

<p><b>Logic Symbol</b></p>	<p><b>The Possible Logic Schematic Combinations</b></p>													
<p><b>Truth Table</b></p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th style="border: none;">PADM</th> <th style="border: none;">QC</th> <th style="border: none;">QO</th> </tr> </thead> <tbody> <tr> <td style="border: none;">L</td> <td style="border: none;">L</td> <td style="border: none;">L</td> </tr> <tr> <td style="border: none;">H</td> <td style="border: none;">H</td> <td style="border: none;">H</td> </tr> </tbody> </table>	PADM	QC	QO	L	L	L	H	H	H	<p><b>Pin Loading</b></p> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th style="border: none;"></th> <th style="border: none;">Load</th> </tr> </thead> <tbody> <tr> <td style="border: none;">PADM</td> <td style="border: none;">4.90 pF</td> </tr> </tbody> </table>		Load	PADM	4.90 pF
PADM	QC	QO												
L	L	L												
H	H	H												
	Load													
PADM	4.90 pF													

Pad Logic

### HDL Syntax

Verilog ..... IDQC3 *inst\_name* (QC, QO, PADM);  
 VHDL..... *inst\_name*: IDQC3 port map (QC, QO, PADM);

### Power Characteristics

Parameter	Value	Units
Static I <sub>DD</sub> (T <sub>J</sub> = 85°C)	15.832	nA
EQL <sub>pd</sub>	11.4	Eq-load

See page 2-13 for power equation.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	$t_{PLH}$	0.813	0.880	0.970	1.060	1.165
			$t_{PHL}$	0.563	0.723	0.846	0.944	1.043
PADM		QO	$t_{PLH}$	0.000				
			$t_{PHL}$	0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

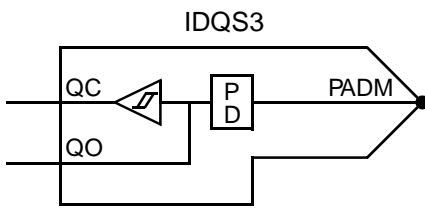
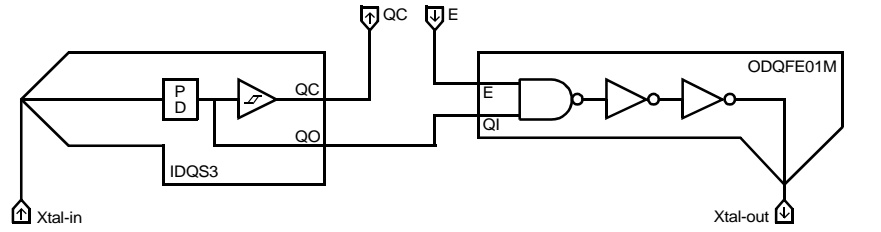
### Design Notes:

The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS-level schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

<b>Logic Symbol</b> 	<b>Logic Schematic</b> 															
<b>Truth Table</b> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th>PADM</th> <th>QC</th> <th>QO</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	QO	L	L	L	H	H	H	<b>Pin Loading</b> <table border="1" style="margin-left: auto; margin-right: auto; border-collapse: collapse;"> <thead> <tr> <th></th> <th colspan="2">Load</th> </tr> </thead> <tbody> <tr> <td>PADM</td> <td>4.90</td> <td>pF</td> </tr> </tbody> </table>		Load		PADM	4.90	pF
PADM	QC	QO														
L	L	L														
H	H	H														
	Load															
PADM	4.90	pF														

### HDL Syntax

Verilog ..... IDQS3 *inst\_name* (QC, QO, PADM);

VHDL..... *inst\_name*: IDQS3 port map (QC, QO, PADM);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	15.963	nA
$EQL_{pd}$	18.0	Eq-load

See page 2-13 for power equation.

Pad Logic

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	$t_{PLH}$	1.551	1.616	1.705	1.796	1.902
			$t_{PHL}$	1.018	1.159	1.278	1.372	1.465
PADM		QO	$t_{PLH}$	0.000				
			$t_{PHL}$	0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Design Notes:

The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.



## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

IDTS3 is a non-inverting, TTL-level Schmitt input buffer piece.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H	<table border="1"> <thead> <tr> <th>PADM</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>4.90 pF</td> </tr> </tbody> </table>	PADM	Load		4.90 pF
PADM	QC											
L	L											
H	H											
PADM	Load											
	4.90 pF											

### HDL Syntax

Verilog ..... IDTS3 inst\_IDTS3 (QC, PADM);  
 VHDL..... inst\_IDTS3 : IDTS3 port map (QC, PADM);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	15.451	nA
$EQL_{pd}$	15.8	Eq-load

See page 2-13 for power equation.

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	11	22	32	43 (max)
PADM		QC	$t_{PLH}$	0.962	1.062	1.166	1.256	1.354
			$t_{PHL}$	1.640	1.829	2.014	2.171	2.336

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Pad  
Logic

## AMI500HXP 0.5 micron CMOS Pad Library

### Description

IDTXx is a family of non-inverting, TTL-level, input buffer pieces.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>PADM</th> <th>QC</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	PADM	QC	L	L	H	H
PADM	QC						
L	L						
H	H						

### HDL Syntax

Verilog ..... IDTXx *inst\_name* (QC, PADM);  
 VHDL ..... *inst\_name*: IDTXx port map (QC, PADM);

### Pin Loading

Pin Name	Load	
	IDTX3	IDTX6
PADM (pF)	4.90	4.90

### Power Characteristics

Cell	Equivalent Gates	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
IDTX3	0.0	15.349	10.4
IDTX6	0.0	17.792	18.2

a. See page 2-13 for power equation.

### Propagation Delays (ns)

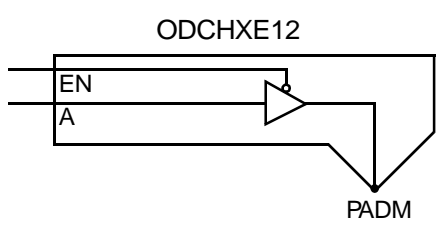
Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5.0V, Typical Process

IDTX3	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM	t <sub>PLH</sub>	0.573	0.718	0.823	0.917	1.026
	To: QC	t <sub>PHL</sub>	0.662	0.860	0.986	1.078	1.166
IDTX6	Number of Equivalent Loads		1	21	42	62	83 (max)
	From: PADM	t <sub>PLH</sub>	0.495	0.661	0.770	0.857	0.938
	To: QC	t <sub>PHL</sub>	0.634	0.818	0.937	1.037	1.135

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Description

ODCHXE12 is a high performance, 12 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol	Truth Table	Pin Loading																				
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>3.5 eqI</td> </tr> <tr> <td>EN</td> <td>6.5 eqI</td> </tr> <tr> <td>PADM</td> <td>4.73 pF</td> </tr> </tbody> </table>		Load	A	3.5 eqI	EN	6.5 eqI	PADM	4.73 pF
EN	A	PADM																				
L	L	L																				
L	H	H																				
H	X	Z																				
	Load																					
A	3.5 eqI																					
EN	6.5 eqI																					
PADM	4.73 pF																					

### HDL Syntax

Verilog ..... ODCHXE12 *inst\_name* (PADM, A, EN);

VHDL..... *inst\_name*: ODCHXE12 port map (PADM, A, EN);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	59.501	nA
$EQL_{pd}$	259.1	Eq-load

See page 2-13 for power equation.

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	100	200	300 (max)
A		PADM	$t_{PLH}$	0.000	0.000	0.000	0.000	0.000
			$t_{PHL}$	0.000	0.000	0.000	0.000	0.000
EN		PADM	$t_{HZ}$	0.064				
			$t_{LZ}$	0.064				
			$t_{ZH}$	0.000	0.000	0.000	0.000	0.000
			$t_{ZL}$	0.000	0.000	0.000	0.000	0.000

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

# ODCHXX12



## AMI500HXP 0.5 micron CMOS Pad Library

### Description

ODCHXX12 is a high performance, 12 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H	<table border="1"> <thead> <tr> <th>A</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>14.5 eqI</td> </tr> </tbody> </table>	A	Load		14.5 eqI
A	PADM											
L	L											
H	H											
A	Load											
	14.5 eqI											

### HDL Syntax

Verilog ..... ODCHXX12 *inst\_name* (PADM, A);  
 VHDL ..... *inst\_name*: ODCHXX12 port map (PADM, A);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	51.517	nA
$EQL_{pd}$	216.6	Eq-load

See page 2-13 for power equation.

### Output Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

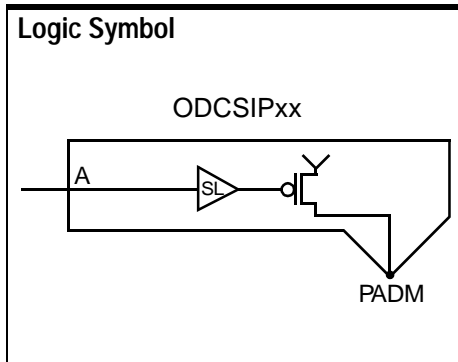
Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	PADM	$t_{PLH}$	0.708	1.513	2.653	4.924	7.191
		$t_{PHL}$	0.778	1.470	2.462	4.437	6.395

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Pad Logic

### Description

ODCSIPxx is a family of 4 to 12 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>Z</td> </tr> </tbody> </table> <p>Z = High Impedance</p>	A	PADM	L	H	H	Z
A	PADM						
L	H						
H	Z						

### HDL Syntax

Verilog ..... ODCSIPxx *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODCSIPxx port map (PADM, A);

### Pin Loading

Pin Name	Load		
	ODCSIP04	ODCSIP08	ODCSIP12
A (eq-load)	4.1	4.1	4.1
PADM (pF)	4.90	4.90	4.90

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODCSIP04	4	56.824	198.7
ODCSIP08	8	56.824	211.8
ODCSIP12	12	56.824	219.2

a. See page 2-13 for power equation.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

Cell	Capacitive Load (pF)		15	50	100	200	300 (max)
	ODCSIP04	From: A To: PADM	$t_{ZH}$	2.444	6.591	12.223	23.247
ODCSIP08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{ZH}$	1.759	3.800	6.642	12.269	17.930
ODCSIP12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{ZH}$	1.754	3.265	5.450	9.928	14.494

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

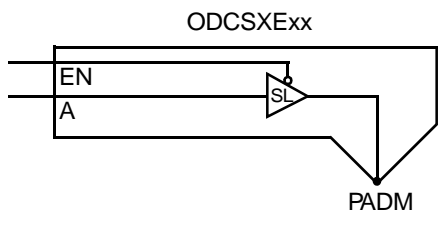
### Tristate Timing

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns) To	Parameter	Cell		
			ODCSIP04	ODCSIP08	ODCSIP12
A	PADM	$t_{HZ}$	0.787	1.011	1.142

### Description

ODCSXExx is a family of 4 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol	Truth Table												
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z
EN	A	PADM											
L	L	L											
L	H	H											
H	X	Z											

### HDL Syntax

Verilog ..... ODCSXExx *inst\_name* (PADM, A, EN);

VHDL..... *inst\_name*: ODCSXExx port map (PADM, A, EN);

### Pin Loading

Pin Name	Load		
	ODCSXE04	ODCSXE08	ODCSXE12
A (eq-load)	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9
PADM (pF)	4.90	4.90	4.90

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODCSXE04	4	58.395	227.1
ODCSXE08	8	58.395	247.8
ODCSXE12	12	58.395	262.0

a. See page 2-13 for power equation.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
	ODCSXE04	From: A	$t_{PLH}$	3.318	7.321	12.855	23.637
To: PADM		$t_{PHL}$	3.299	7.414	13.262	24.910	36.522
From: EN		$t_{ZH}$	2.930	6.879	12.497	23.365	33.841
	To: PADM	$t_{ZL}$	3.219	7.240	12.976	24.602	36.372
ODCSXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	2.407	4.389	7.216	12.864	18.508
	To: PADM	$t_{PHL}$	2.326	4.417	7.399	13.359	19.326
	From: EN	$t_{ZH}$	2.076	4.072	6.920	12.574	18.193
	To: PADM	$t_{ZL}$	1.987	4.176	7.184	13.120	19.106
ODCSXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	2.234	3.820	6.078	10.577	15.065
	To: PADM	$t_{PHL}$	2.150	3.534	5.497	9.439	13.398
	From: EN	$t_{ZH}$	1.797	3.489	5.763	10.225	14.746
	To: PADM	$t_{ZL}$	1.970	3.189	5.152	9.117	13.047

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Tristate Timing

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

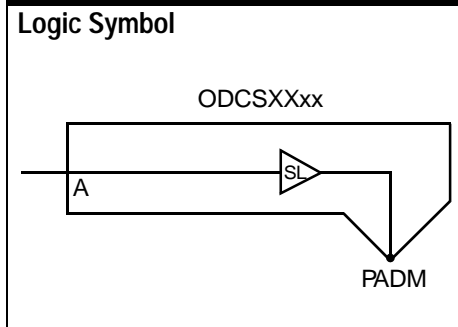
From	Delay (ns)	To	Parameter	Cell		
				ODCSXE04	ODCSXE08	ODCSXE12
EN		PADM	$t_{HZ}$	0.825	1.051	1.180
			$t_{LZ}$	0.914	1.082	1.229

Pad Logic



### Description

ODCSXXxx is a family of 4 to 12 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H
A	PADM						
L	L						
H	H						

### HDL Syntax

Verilog ..... ODCSXXxx *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODCSXXxx port map (PADM, A);

### Pin Loading

Pin Name	Load		
	ODCSXX04	ODCSXX08	ODCSXX12
A (eq-load)	9.3	9.3	9.3

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODCSXX04	4	54.738	206.8
ODCSXX08	8	54.738	227.5
ODCSXX12	12	54.738	241.7

a. See page 2-13 for power equation.

## AMI500HXP 0.5 micron CMOS Pad Library

### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

Device	Capacitive Load (pF)		15	50	100	200	300 (max)
	ODCSXX04	From: A	$t_{PLH}$	2.506	6.388	11.894	22.615
To: PADM		$t_{PHL}$	2.731	6.772	12.584	24.242	35.895
ODCSXX08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.593	3.544	6.341	11.947	17.564
ODCSXX12	To: PADM	$t_{PHL}$	1.719	3.789	6.755	12.699	18.653
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXX12	From: A	$t_{PLH}$	1.536	3.071	5.272	9.728	14.250
	To: PADM	$t_{PHL}$	1.364	2.770	4.739	8.654	12.610

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

ODCXIPxx is a family of 1 to 12 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol	Truth Table						
	<table border="1" style="margin: auto;"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>Z</td> </tr> </tbody> </table> <p>Z = High Impedance</p>	A	PADM	L	H	H	Z
A	PADM						
L	H						
H	Z						

### HDL Syntax

Verilog ..... ODCXIPxx *inst\_name* (PADM, A);  
 VHDL ..... *inst\_name*: ODCXIPxx port map (PADM, A);

### Pin Loading

Pin Name	Load				
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
A (eq-load)	2.8	2.8	2.8	3.9	3.9
PADM (pF)	4.90	4.90	4.90	4.90	4.90

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static IDD (T <sub>J</sub> = 85°C) (nA)	EQLpd (Eq-load)
ODCXIP01	1	46.245	158.6
ODCXIP02	2	46.764	163.4
ODCXIP04	4	47.309	172.7
ODCXIP08	8	48.374	188.7
ODCXIP12	12	49.438	198.8

a. See page 2-13 for power equation.

### Propagation Delays (ns)

Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5.0V, Typical Process

ODCXIP01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t <sub>ZH</sub>	4.792	7.018	9.250	12.605	18.208

Pad Logic

## AMI500HXPM 0.5 micron CMOS Pad Library

ODCXIP02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	$t_{ZH}$	2.752	6.634	9.391	12.160	17.751
ODCXIP04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{ZH}$	1.748	3.690	6.473	12.023	17.547
ODCXIP08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{ZH}$	1.278	2.311	3.747	6.575	9.372
ODCXIP12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{ZH}$	1.198	2.058	3.236	5.500	9.372

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Tristate Timing

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns) To	Parameter	Cell				
			ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12
APADM		$t_{HZ}$	0.963	0.874	1.089	1.382	1.444

### Description

ODCXXExx is a family of 1 to 12 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol	Truth Table												
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z
EN	A	PADM											
L	L	L											
L	H	H											
H	X	Z											

### HDL Syntax

Verilog ..... ODCXXExx *inst\_name* (PADM, A, EN);

VHDL..... *inst\_name*: ODCXXExx port map (PADM, A, EN);

### Pin Loading

Pin Name	Load				
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12
A (eq-load)	5.6	7.9	7.9	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5
PADM (pF)	4.90	4.90	4.90	4.90	4.90

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODCXXE01	1	37.149	20.1
ODCXXE02	2	49.110	174.0
ODCXXE04	4	49.110	185.5
ODCXXE08	8	55.615	232.0
ODCXXE12	12	55.615	246.7

a. See page 2-13 for power equation.

## AMI500HXPm 0.5 micron CMOS Pad Library

### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
	ODCXE01	From: A	$t_{PLH}$	4.754	7.026	9.282	12.637
To: PADM		$t_{PHL}$	5.210	7.471	9.760	13.249	19.186
From: EN		$t_{ZH}$	4.938	7.236	9.504	12.857	18.356
	To: PADM	$t_{ZL}$	5.224	7.550	9.877	13.370	19.207
	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A	$t_{PLH}$	2.556	6.441	9.221	12.000	17.551
ODCXE02	To: PADM	$t_{PHL}$	2.779	6.861	9.776	12.690	18.518
	From: EN	$t_{ZH}$	2.705	6.646	9.466	12.254	17.726
	To: PADM	$t_{ZL}$	2.818	6.827	9.727	12.645	18.519
	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.720	3.690	6.474	12.017	17.551
ODCXE04	To: PADM	$t_{PHL}$	1.831	3.880	6.813	12.656	18.463
	From: EN	$t_{ZH}$	1.830	3.832	6.658	12.212	17.689
	To: PADM	$t_{ZL}$	1.836	3.908	6.839	12.672	18.487
	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.934	2.913	4.306	7.124	9.966
ODCXE08	To: PADM	$t_{PHL}$	1.654	2.698	4.186	7.159	10.143
	From: EN	$t_{ZH}$	1.597	2.584	3.991	6.812	9.638
	To: PADM	$t_{ZL}$	1.463	2.530	4.012	6.982	9.985
	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.990	2.778	3.898	6.147	8.404
ODCXE12	To: PADM	$t_{PHL}$	1.614	2.335	3.300	5.248	7.255
	From: EN	$t_{ZH}$	1.473	2.323	3.477	5.731	7.963
	To: PADM	$t_{ZL}$	1.344	2.092	3.115	5.102	7.049

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

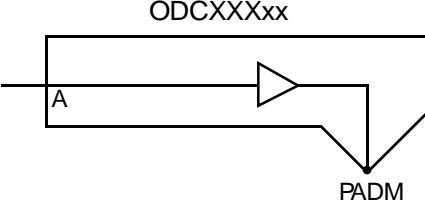
### Tristate Timing

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

Delay (ns)		Parameter	Cell				
From	To		ODCXE01	ODCXE02	ODCXE04	ODCXE08	ODCXE12
EN	PADM	$t_{HZ}$	1.368	1.181	1.633	1.241	1.435
		$t_{LZ}$	0.447	0.413	0.580	1.098	1.330

### Description

ODCXXXxx is a family of 1 to 12 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H
A	PADM						
L	L						
H	H						

### HDL Syntax

Verilog ..... ODCXXXxx *inst\_name* (PADM, A);

VHDL..... *inst\_name*: ODCXXXxx port map (PADM, A);

### Pin Loading

Pin Name	Load				
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12
A (eq-load)	4.3	3.7	5.0	6.5	8.2

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODCXXX01	1	46.179	159.3
ODCXXX02	2	46.179	161.9
ODCXXX04	4	47.216	170.4
ODCXXX08	8	48.303	187.0
ODCXXX12	12	48.303	213.5

a. See page 2-13 for power equation.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

ODCXXX01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A	$t_{PLH}$	4.601	6.825	9.054	12.403	17.995
To: PADM	$t_{PHL}$	4.928	7.268	9.587	13.053	18.884	
ODCXXX02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A	$t_{PLH}$	2.549	6.430	9.236	12.030	17.535
To: PADM	$t_{PHL}$	2.872	6.940	9.849	12.761	18.593	
ODCXXX04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.499	3.429	6.207	11.764	17.283
To: PADM	$t_{PHL}$	1.733	3.753	6.651	12.471	18.312	
ODCXXX08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.174	2.191	3.627	6.459	9.255
To: PADM	$t_{PHL}$	1.283	2.304	3.773	6.754	9.724	
ODCXXX12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.144	1.952	3.054	5.188	7.356
To: PADM	$t_{PHL}$	1.217	1.848	2.728	4.520	6.275	

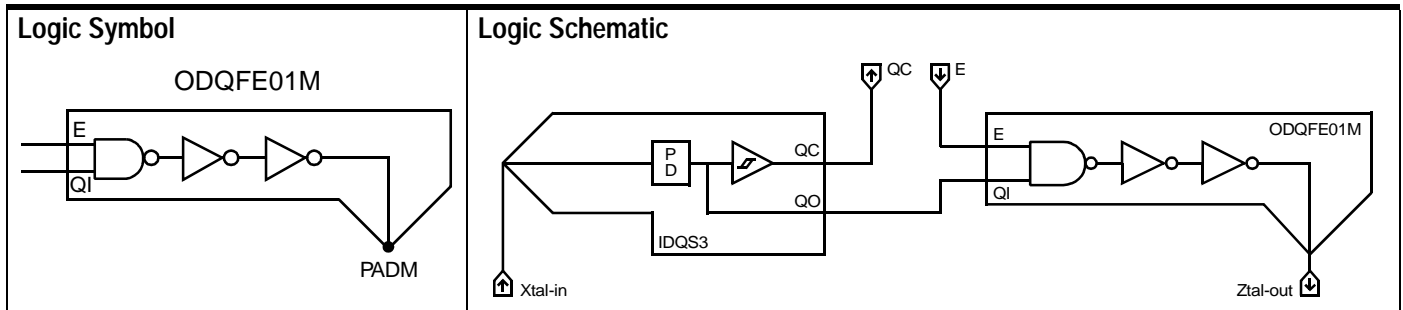
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Pad Logic



### Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.



<p><b>Truth Table</b></p> <table border="1"> <thead> <tr> <th>PADM</th> <th>E</th> <th>QI</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>X</td> </tr> </tbody> </table>	PADM	E	QI	L	H	H	H	H	L	H	L	X	<p><b>Pin Loading</b></p> <table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>E</td> <td>3.5 eqI</td> </tr> <tr> <td>QI</td> <td>3.1 eqI</td> </tr> </tbody> </table>		Load	E	3.5 eqI	QI	3.1 eqI
PADM	E	QI																	
L	H	H																	
H	H	L																	
H	L	X																	
	Load																		
E	3.5 eqI																		
QI	3.1 eqI																		

### HDL Syntax

Verilog ..... ODQFE01M *inst\_name* (PADM, E, QI);

VHDL..... *inst\_name*: ODQFE01M port map (PADM, E, QI);

### Power Characteristics

Parameter	Value	Units
Static I <sub>DD</sub> (T <sub>J</sub> = 85°C)	47.039	nA
EQL <sub>pd</sub>	159.7	Eq-load

See page 2-13 for power equation.

Pad  
Logic

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	25	35	50	75 (max)
E	PADM		$t_{PLH}$	4.951	7.170	9.398	12.753	18.369
			$t_{PHL}$	5.899	8.211	10.520	14.003	19.875
QI	PADM		$t_{PLH}$	5.082	7.299	9.499	12.819	18.472
			$t_{PHL}$	5.981	8.314	10.652	14.155	19.967

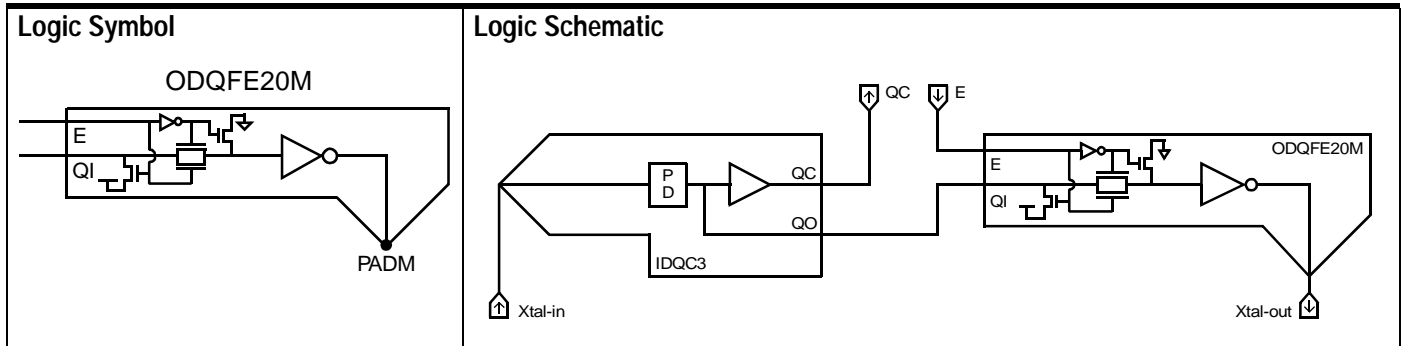
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

### Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.



Truth Table			Pin Loading	
PADM	E	QI		Load
H	L	X	E	5.3 eqI
H	H	L	QI	5.5 eqI
L	H	H		

### HDL Syntax

Verilog ..... ODQFE20M *inst\_name* (PADM, E, QI);

VHDL..... *inst\_name*: ODQFE20M port map (PADM, E, QI);

### Power Characteristics

Parameter	Value	Units
Static I <sub>DD</sub> (T <sub>J</sub> = 85°C)	46.401	nA
EQL <sub>pd</sub>	170.8	Eq-load

See page 2-13 for power equation.

Pad Loading

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	75	100	150 (max)
E	PADM		$t_{PLH}$	3.458	7.343	10.118	12.894	18.450
			$t_{PHL}$	2.637	6.711	9.613	12.520	18.369
QI	PADM		$t_{PLH}$	2.414	6.330	9.106	11.871	17.379
			$t_{PHL}$	2.714	6.786	9.687	12.593	18.421

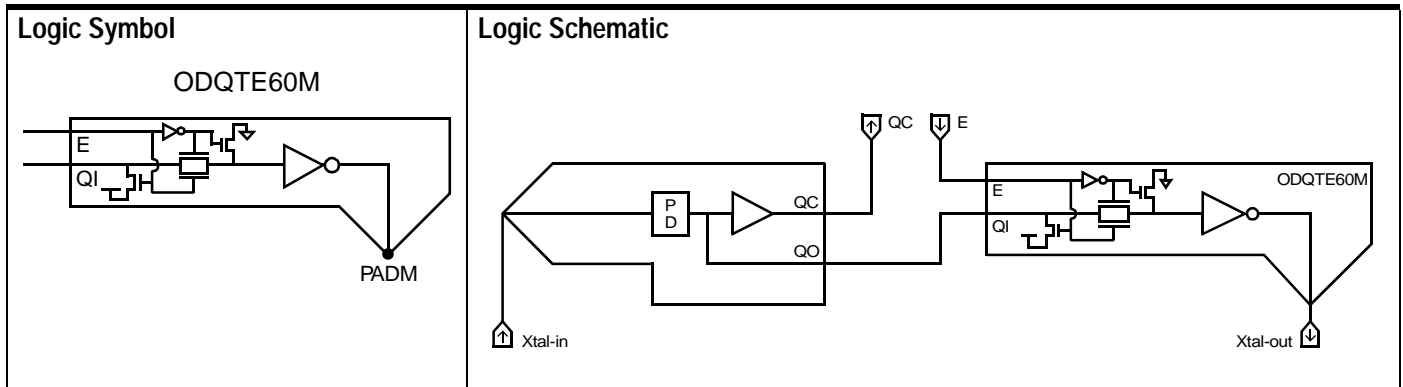
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

### Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.



Truth Table			Pin Loading	
PADM	E	QI		Load
H	L	X	E	5.3 eqI
H	H	L	QI	5.5 eqI
L	H	H		

### HDL Syntax

Verilog ..... ODQTE60M *inst\_name* (PADM, E, QI);  
 VHDL..... *inst\_name*: ODQTE60M port map (PADM, E, QI);

### Power Characteristics

Parameter	Value	Units
Static I <sub>DD</sub> (T <sub>J</sub> = 85°C)	46.401	nA
EQL <sub>pd</sub>	179.5	Eq-load

See page 2-13 for power equation.

Pad  
Logic

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	100	200	300 (max)
E		PADM	$t_{PLH}$	2.700	4.705	7.491	13.007	18.563
			$t_{PHL}$	1.704	3.707	6.597	12.423	18.284
QI		PADM	$t_{PLH}$	1.445	3.486	6.272	11.759	17.310
			$t_{PHL}$	1.721	3.803	6.701	12.493	18.343

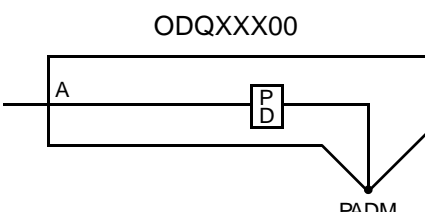
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

### Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>2.4 eqI</td> </tr> </tbody> </table>		Load	A	2.4 eqI
A	PADM											
L	L											
H	H											
	Load											
A	2.4 eqI											

### HDL Syntax

Verilog ..... ODQXXX00 *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODQXXX00 port map (PADM, A);

### Power Characteristics

Parameter	Value	Units
Static I <sub>DD</sub> (T <sub>J</sub> = 85°C)	45.048	nA
EQL <sub>pd</sub>	148.8	Eq-load

See page 2-13 for power equation.

# ODTHXE12

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

ODTHXE12 is a high performance, 12 mA, non-inverting, LVTTTL-level, tristate output buffer piece with active low enable.

Logic Symbol	Truth Table	Pin Loading																				
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>3.5 eqI</td> </tr> <tr> <td>EN</td> <td>6.5 eqI</td> </tr> <tr> <td>PADM</td> <td>4.90 pF</td> </tr> </tbody> </table>		Load	A	3.5 eqI	EN	6.5 eqI	PADM	4.90 pF
EN	A	PADM																				
L	L	L																				
L	H	H																				
H	X	Z																				
	Load																					
A	3.5 eqI																					
EN	6.5 eqI																					
PADM	4.90 pF																					

### HDL Syntax

Verilog ..... ODTXHE12 *inst\_name* (PADM, A, EN);

VHDL..... *inst\_name*: ODTXHE12 port map (PADM, A, EN);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	59.501	nA
$EQL_{pd}$	263.8	Eq-load

See page 2-13 for power equation.

### Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ , Typical Process

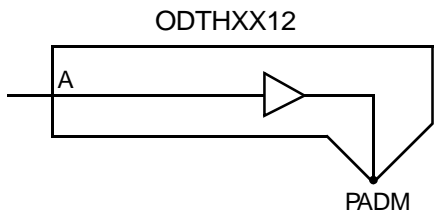
From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	100	200	300 (max)
A		PADM	$t_{PLH}$	0.964	1.380	1.981	3.194	4.416
			$t_{PHL}$	1.582	2.500	4.055	7.250	10.395
EN		PADM	$t_{HZ}$	0.929				
			$t_{LZ}$	0.941				
			$t_{ZH}$	0.788	1.221	1.822	3.028	4.249
			$t_{ZL}$	1.446	2.493	4.062	7.252	10.412

Delay will vary with input conditions. See page 2-15 for interconnect estimates.



### Description

ODTHXX12 is a high performance, 12 mA, non-inverting, LVTTTL-level output buffer piece.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H	<table border="1"> <thead> <tr> <th>A</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>14.5 eqI</td> </tr> </tbody> </table>	A	Load		14.5 eqI
A	PADM											
L	L											
H	H											
A	Load											
	14.5 eqI											

### HDL Syntax

Verilog ..... ODTXXX12 *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODTXXX12 port map (PADM, A);

### Power Characteristics

Parameter	Value	Units
Static I <sub>DD</sub> (T <sub>J</sub> = 85°C)	51.517	nA
EQL <sub>pd</sub>	216.6	Eq-load

See page 2-13 for power equation.

### Output Propagation Delays

Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5V, Typical Process

From	Delay (ns)	To	Parameter	Capacitive Load (pF)				
				15	50	100	200	300 (max)
A		PADM	t <sub>PLH</sub>	0.516	0.942	1.551	2.761	3.958
			t <sub>PHL</sub>	1.042	2.158	3.727	6.876	10.068

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

ODTSXExx is a family of 4 to 12 mA, non-inverting, LVTTTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol	Truth Table												
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table>	EN	A	PADM	L	L	L	L	H	H	H	X	Z
EN	A	PADM											
L	L	L											
L	H	H											
H	X	Z											

### HDL Syntax

Verilog ..... ODTSXExx *inst\_name* (PADM, A, EN);

VHDL..... *inst\_name*: ODTSXExx port map (PADM, A, EN);

### Pin Loading

Pin Name	Load		
	ODTSXE04	ODTSXE08	ODTSXE12
A (eq-load)	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9
PADM (pF)	4.90	4.90	4.90

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODTSXE04	4	58.395	227.1
ODTSXE08	8	58.395	247.8
ODTSXE12	12	58.395	262.0

a. See page 2-13 for power equation.

Pad Logic

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ , Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
	ODTSXE04	From: A	$t_{PLH}$	2.457	4.509	7.440	13.424
To: PADM		$t_{PHL}$	4.724	10.910	19.331	35.806	52.288
From: EN		$t_{ZH}$	1.998	4.103	7.098	13.098	19.116
	To: PADM	$t_{ZL}$	4.854	10.798	19.063	35.664	52.049
ODTSXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.916	3.002	4.516	7.552	10.621
	To: PADM	$t_{PHL}$	3.141	6.486	10.986	19.692	28.228
	From: EN	$t_{ZH}$	1.536	2.648	4.162	7.169	10.260
	To: PADM	$t_{ZL}$	2.736	6.203	10.776	19.452	27.996
ODTSXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.805	2.692	3.932	6.345	8.783
	To: PADM	$t_{PHL}$	2.486	4.675	7.838	13.877	19.412
	From: EN	$t_{ZH}$	1.557	2.371	3.555	5.975	8.436
	To: PADM	$t_{ZL}$	2.222	4.530	7.657	13.584	19.264

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Tristate Timing

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ , Typical Process

From	Delay (ns) To	Parameter	Cell		
			ODTSXE04	ODTSXE08	ODTSXE12
EN	PADM	$t_{HZ}$	0.825	1.051	1.180
		$t_{LZ}$	0.914	1.082	1.229

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

ODTSXNxx is a family of 4 to 12 mA, non-inverting, LVTTTL-level, output buffer pieces with N-channel open-drains (pull-down) and controlled slew rate outputs.

<p><b>Logic Symbol</b></p>	<p><b>Truth Table</b></p> <table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>Z</td> </tr> </tbody> </table> <p>Z = High Impedance</p>	A	PADM	L	L	H	Z
A	PADM						
L	L						
H	Z						

### HDL Syntax

Verilog ..... ODT SXNxx *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODT SXNxx port map (PADM, A);

Pad Logic

### Pin Loading

Pin Name	Load		
	ODTSXN04	ODTSXN08	ODTSXN12
A (eq-load)	8.1	8.1	8.1
PADM (pF)	4.90	4.90	4.90

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODTSXN04	4	51.481	175.6
ODTSXN08	8	51.481	183.2
ODTSXN12	12	51.481	190.0

a. See page 2-13 for power equation.

### Propagation Delays (ns)

Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5V, Typical Process

ODTSXN04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	To: PADM	t <sub>ZL</sub>	3.612	9.523	17.805	34.107

## AMI500HXPM 0.5 micron CMOS Pad Library

ODTSXN08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{zL}$	2.405	5.407	9.648	18.110	26.559
ODTSXN12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{zL}$	1.643	3.809	6.700	12.319	17.893

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Tristate Timing

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ , Typical Process

From	Delay (ns) To	Parameter	Cell		
			ODTSXN04	ODTSXN08	ODTSXN12
A	PADM	$t_{LZ}$	0.844	0.959	1.066

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

ODTSXXxx is a family of 4 to 12 mA, non-inverting, LVTTTL-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H
A	PADM						
L	L						
H	H						

### HDL Syntax

Verilog ..... ODTSXXxx *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODTSXXxx port map (PADM, A);

### Pin Loading

Pin Name	Load		
	ODTSXX04	ODTSXX08	ODTSXX12
A (eq-load)	9.3	9.3	9.3

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODTSXX04	4	54.738	206.8
ODTSXX08	8	54.738	227.5
ODTSXX12	12	54.738	241.7

a. See page 2-13 for power equation.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ , Typical Process

ODTSXX04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.492	3.555	6.574	12.599	18.563
To: PADM	$t_{PLH}$	4.032	10.055	18.434	34.926	51.255	
ODTSXX08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	0.999	2.088	3.633	6.677	9.684
To: PADM	$t_{PLH}$	2.503	5.772	10.191	18.790	27.319	
ODTSXX12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.272	1.890	3.054	5.506	7.890
To: PADM	$t_{PLH}$	1.919	4.130	7.163	12.984	18.615	

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

## AMI500HXP 0.5 micron CMOS Pad Library

### Description

ODTXXE<sub>xx</sub> is a family of 1 to 12 mA, non-inverting, LVTTTL-level, tristate output buffer pieces with active low enables.

Logic Symbol	Truth Table												
	<table border="1"> <thead> <tr> <th>EN</th> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>X</td> <td>Z</td> </tr> </tbody> </table> <p>Z = High Impedance</p>	EN	A	PADM	L	L	L	L	H	H	H	X	Z
EN	A	PADM											
L	L	L											
L	H	H											
H	X	Z											

### HDL Syntax

Verilog ..... ODTXXE<sub>xx</sub> *inst\_name* (PADM, A, EN);

VHDL ..... *inst\_name*: ODTXXE<sub>xx</sub> port map (PADM, A, EN);

### Pin Loading

Pin Name	Load				
	ODTXXE01	ODTXXE02	ODTXXE04	ODTXXE08	ODTXXE12
A (eq-load)	5.6	7.9	7.9	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5
PADM (pF)	4.90	4.90	4.90	4.90	4.90

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODTXXE01	1	47.619	164.6
ODTXXE02	2	49.110	174.0
ODTXXE04	4	49.110	185.5
ODTXXE08	8	55.615	232.0
ODTXXE12	12	55.615	246.7

a. See page 2-13 for power equation.



## AMI500HXPM 0.5 micron CMOS Pad Library

### Propagation Delays (ns)

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ , Typical Process

ODTXE01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	$t_{PLH}$ $t_{PHL}$	2.789 7.761	4.059 11.472	5.298 15.187	7.111 20.761	10.049 30.058
	From: EN To: PADM	$t_{ZH}$ $t_{ZL}$	2.999 7.677	4.191 11.437	5.361 15.188	7.137 20.775	10.233 29.981
ODTXE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	$t_{PLH}$ $t_{PHL}$	1.645 4.089	3.723 10.608	5.200 15.261	6.697 19.906	9.752 29.173
	From: EN To: PADM	$t_{ZH}$ $t_{ZL}$	1.856 4.167	3.933 10.660	5.438 15.300	6.947 19.943	9.941 29.241
ODTXE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{PLH}$ $t_{PHL}$	1.250 2.526	2.308 5.789	3.798 10.432	6.791 19.716	9.799 29.008
	From: EN To: PADM	$t_{ZH}$ $t_{ZL}$	1.383 2.505	2.492 5.769	3.986 10.412	6.951 19.717	9.981 29.053
ODTXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{PLH}$ $t_{PHL}$	1.502 2.055	2.116 3.704	2.932 6.099	4.469 10.920	5.937 15.732
	From: EN To: PADM	$t_{ZH}$ $t_{ZL}$	1.191 1.706	1.780 3.470	2.570 5.893	4.102 10.699	5.606 15.531
ODTXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{PLH}$ $t_{PHL}$	1.589 1.860	2.082 2.961	2.742 4.567	3.985 7.764	5.166 10.900
	From: EN To: PADM	$t_{ZH}$ $t_{ZL}$	1.304 1.652	1.794 2.804	2.406 4.379	3.620 7.542	4.858 10.747

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Tristate Timing

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ , Typical Process

From	Delay (ns) To	Parameter	Cell				
			ODTXE01	ODTXE02	ODTXE04	ODTXE08	ODTXE12
EN	PADM	$t_{HZ}$	1.368	1.181	1.633	1.241	1.435
		$t_{LZ}$	0.447	0.413	0.580	1.098	1.330

Pad  
Logic

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

ODTXXNxx is a family of 1 to 12 mA, non-inverting, LVTTTL-level, output buffer pieces with N-channel, open-drains (pull-down).

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>Z</td> </tr> </tbody> </table> <p>Z = High Impedance</p>	A	PADM	L	L	H	Z
A	PADM						
L	L						
H	Z						

### HDL Syntax

Verilog ..... ODTXXNxx *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODTXXNxx port map (PADM, A);

### Pin Loading

Pin Name	Load				
	ODTXXN01	ODTXXN02	ODTXXN04	ODTXXN08	ODTXXN12
A (eq-load)	4.3	4.3	4.3	8.3	8.3
PADM (pF)	4.90	4.90	4.90	4.90	4.90

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODTXXN01	1	46.168	153.0
ODTXXN02	2	46.168	154.9
ODTXXN04	4	46.168	158.9
ODTXXN08	8	48.292	167.4
ODTXXN12	12	48.292	174.7

a. See page 2-13 for power equation.

### Propagation Delays (ns)

Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5V, Typical Process

ODTXXN01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A	To: PADM	t <sub>ZL</sub>				
			6.683	10.064	13.445	18.487	26.806

## AMI500HXPM 0.5 micron CMOS Pad Library

Cell	Capacitive Load (pF)		15	50	75	100	150 (max)
	ODTXXN02	From: A To: PADM	$t_{zL}$	3.507	9.368	13.551	17.739
ODTXXN04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{zL}$	2.027	4.975	9.162	17.540	25.919
ODTXXN08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{zL}$	1.208	2.732	4.882	9.165	13.443
ODTXXN12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	$t_{zL}$	1.034	2.067	3.512	6.354	9.160

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

### Tristate Timing

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ , Typical Process

From	Delay (ns) To	Parameter	Cell				
			ODTXXN01	ODTXXN02	ODTXXN04	ODTXXN08	ODTXXN12
A	PADM	$t_{LZ}$	0.246	0.337	0.516	0.568	0.784

## AMI500HXP 0.5 micron CMOS Pad Library

### Description

ODTXXXxx is a family of 1 to 12 mA, non-inverting, LVTTTL-level output buffer pieces.

Logic Symbol	Truth Table						
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H
A	PADM						
L	L						
H	H						

### HDL Syntax

Verilog ..... ODTXXXxx *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODTXXXxx port map (PADM, A);

### Pin Loading

Pin Name	Load				
	ODTXXX01	ODTXXX02	ODTXXX04	ODTXXX08	ODTXXX12
A (eq-load)	4.3	4.3	6.2	8.3	8.2

### Power Characteristics

Cell	Output Drive (mA)	Power Characteristics <sup>a</sup>	
		Static I <sub>DD</sub> (T <sub>J</sub> = 85°C) (nA)	EQL <sub>pd</sub> (Eq-load)
ODTXXX01	1	46.179	159.3
ODTXXX02	2	46.179	164.8
ODTXXX04	4	47.216	176.3
ODTXXX08	8	48.303	198.8
ODTXXX12	12	48.303	213.5

a. See page 2-13 for power equation.

### Propagation Delays (ns)

Conditions: T<sub>J</sub> = 25°C, V<sub>DD</sub> = 5V, Typical Process

ODTXXX01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A	t <sub>PLH</sub>	2.614	3.815	5.001	6.790	9.853
	To: PADM	t <sub>PHL</sub>	7.546	11.250	14.965	20.542	29.823

Pad Logic

## AMI500HXPM 0.5 micron CMOS Pad Library

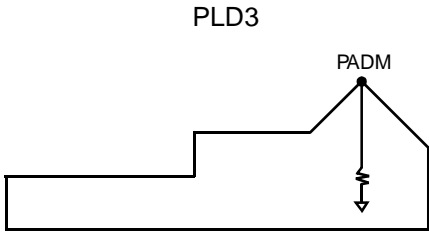
ODTXXX02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A	$t_{PLH}$	1.632	3.729	5.212	6.705	9.737
To: PADM	$t_{PHL}$	4.198	10.680	15.322	19.970	29.279	
ODTXXX04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	1.065	2.116	3.608	6.605	9.596
To: PADM	$t_{PHL}$	2.388	5.610	10.252	19.555	28.823	
ODTXXX08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	0.855	1.461	2.243	3.761	5.288
To: PADM	$t_{PHL}$	1.641	3.316	5.720	10.532	15.340	
ODTXXX12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A	$t_{PLH}$	0.905	1.365	1.970	3.136	4.277
To: PADM	$t_{PHL}$	1.354	2.381	3.836	6.683	9.473	

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
 <p>The logic symbol for PLD3 is a buffer with a pull-down resistor. The input is on the left, and the output is on the right. A resistor labeled PADM is connected between the output and ground.</p>	<p>N/A</p>	<p>N/A</p>

### HDL Syntax

Verilog ..... PLD3 *inst\_name* (PADM);  
 VHDL..... *inst\_name*: PLD3 port map (PADM);

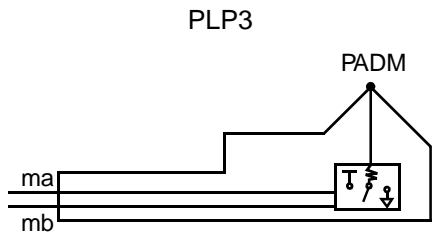
### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	13.883	nA
$EQL_{pd}$	149.6	Eq-load

See page 2-13 for power equation.

### Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading																					
	<table border="1"> <thead> <tr> <th>MA</th> <th>MB</th> <th>PADM Function</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Pull-down</td> </tr> <tr> <td>H</td> <td>H</td> <td>Pull-up</td> </tr> <tr> <td>H</td> <td>L</td> <td>Tristate</td> </tr> <tr> <td>L</td> <td>H</td> <td>Tristate</td> </tr> </tbody> </table>	MA	MB	PADM Function	L	L	Pull-down	H	H	Pull-up	H	L	Tristate	L	H	Tristate	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td>MA</td> <td>2.1 eqI</td> </tr> <tr> <td>MB</td> <td>1.8 eqI</td> </tr> </tbody> </table>		Load	MA	2.1 eqI	MB	1.8 eqI
MA	MB	PADM Function																					
L	L	Pull-down																					
H	H	Pull-up																					
H	L	Tristate																					
L	H	Tristate																					
	Load																						
MA	2.1 eqI																						
MB	1.8 eqI																						

### HDL Syntax

Verilog ..... PLP3 *inst\_name* (PADM, MA, MB);

VHDL..... *inst\_name*: PLP3 port map (PADM, MA, MB);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	13.883	nA
$EQL_{pd}$	146.6	Eq-load

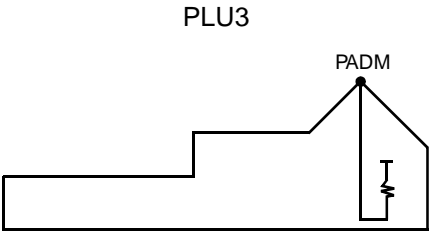
See page 2-13 for power equation.

# PLU3

## AMI500HXPM 0.5 micron CMOS Pad Library

### Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
 <p>The logic symbol for PLU3 is a buffer with a pull-up resistor. The input is on the left, and the output is on the right. A pull-up resistor is connected to the output node, labeled PADM. The resistor is connected to a supply voltage source, represented by a battery symbol.</p>	<p>N/A</p>	<p>N/A</p>

### HDL Syntax

Verilog ..... PLU3 *inst\_name* (PADM);  
 VHDL..... *inst\_name*: PLU3 port map (PADM);

### Power Characteristics

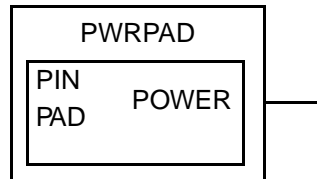
Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	13.892	nA
$EQL_{pd}$	149.5	Eq-load

See page 2-13 for power equation.  
 Delay will vary with input conditions. See page 2-15 for interconnect estimates.



### Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see "Interconnect Load Estimation" on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

### Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
        SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

### VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
port map (PADM => VDD_5V);
```

### Bolt syntax

```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

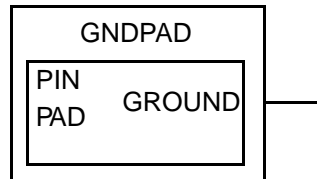
where:

- SUPPLY\_5V is the instance name for PWRPAD
- PAD\_5V is the name of the supply
- IPWR, OPWR1 are logical buses (see section ...)
- VDD\_5V is the chip port name

## AMI500HXP 0.5 micron CMOS Pad Library

### Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see "Interconnect Load Estimation" on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

### Verilog syntax

```
defparam GROUND1.LVSS = "VSS",  
         GROUND1.CONTACT = "CGND,OGND";  
GNDPAD GROUND1 (.PADM(VSS1));
```

### VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")  
port map (PADM => VSS1);
```

### Bolt syntax

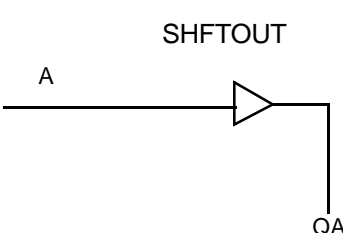
```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses (see section ...)
- VSS1 is the chip port name

### Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 3.3V core to a 5.0V pad.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>A</th> <th>QA</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	QA	L	L	H	H	<table border="1"> <thead> <tr> <th>A</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>4.1</td> </tr> </tbody> </table>	A	Load		4.1
A	QA											
L	L											
H	H											
A	Load											
	4.1											

### HDL Syntax

Verilog ..... SHFTOUT *inst\_name* (QA, A);

VHDL..... *inst\_name*: SHFTOUT port map (QA, A);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	12.309	nA
$EQL_{pd}$	8.3	eql

### Propagation Delays

\*See note at beginning of section to compute total delay.

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	3	6	10	13 (max)
A		QA	$t_{PLH}$	0.274	0.309	0.352	0.407	0.450
			$t_{PHL}$	0.252	0.289	0.345	0.418	0.472

Pad  
Logic

# SHFTOUTT

## AMI500HXP 0.5 micron CMOS Pad Library

### Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 3.3V core to a 5.0V pad.

Logic Symbol	Truth Table	Pin Loading																										
	<table border="1"> <thead> <tr> <th>A</th> <th>EN</th> <th>QA</th> <th>QEN</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>X</td> <td>L</td> <td>X</td> </tr> <tr> <td>H</td> <td>X</td> <td>H</td> <td>X</td> </tr> <tr> <td>X</td> <td>L</td> <td>X</td> <td>L</td> </tr> <tr> <td>X</td> <td>H</td> <td>X</td> <td>H</td> </tr> </tbody> </table>	A	EN	QA	QEN	L	X	L	X	H	X	H	X	X	L	X	L	X	H	X	H	<table border="1"> <thead> <tr> <th></th> <th>Load</th> </tr> </thead> <tbody> <tr> <td><b>A(eql)</b></td> <td>3.0</td> </tr> <tr> <td><b>EN(eql)</b></td> <td>3.2</td> </tr> </tbody> </table>		Load	<b>A(eql)</b>	3.0	<b>EN(eql)</b>	3.2
A	EN	QA	QEN																									
L	X	L	X																									
H	X	H	X																									
X	L	X	L																									
X	H	X	H																									
	Load																											
<b>A(eql)</b>	3.0																											
<b>EN(eql)</b>	3.2																											

### HDL Syntax

Verilog ..... SHFTOUTT *inst\_name* (QA, QEN, A, EN);

VHDL..... *inst\_name*: SHFTOUTT port map (QA, QEN, A, EN);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	13.217	nA
$EQL_{pd}$	10.6	eql

### Propagation Delays

\*See note at beginning of section to compute total delay.

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$ , Typical Process

From	Delay (ns)	To	Parameter	Number of Equivalent Loads				
				1	2	4	6	8 (max)
A		QA	$t_{PLH}$	0.292	0.321	0.374	0.427	0.484
			$t_{PHL}$	0.290	0.331	0.411	0.489	0.567
EN		QEN	$t_{PLH}$	0.294	0.327	0.390	0.448	0.503
			$t_{PHL}$	0.303	0.345	0.423	0.497	0.568

Pad Logic