# AH5020C

***AH5020C Monolithic Analog Current Switch***

Literature Number: SNOSBD5A

National Semiconductor

July 1987

# AH5020C Monolithic Analog Current Switch

## General Description

This versatile dual monolithic JFET analog switch economically fulfills a wide variety of multiplexing and analog switching applications.

These switches may be driven directly from standard 5V logic.

The monolithic construction guarantees tight resistance match and track.

## Features

- Interfaces with standard TTL
- "ON" resistance match — 2Ω
- Low "ON" resistance — 150Ω
- Very low leakage — 50 pA
- Large analog signal range — ±10V peak
- High switching speed — 150 ns
- Excellent isolation between channels — 80 dB at 1 kHz

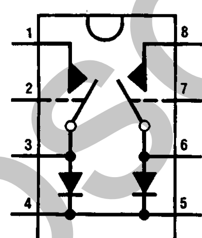
## Applications

- A/D and D/A converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

For voltage switching applications see LF13201, LF13202, LF13331, LF13332, and LF13333 Analog Switch Family, or the CMOS Analog Switch Family.

## Connection and Schematic Diagrams (All switches shown are for logical "1")

**Dual-In-Line Package**

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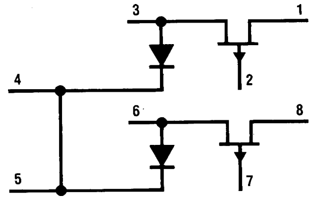
**Top View**

**Order Number AH5020CJ**
**See NS Package Number J08A**

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**Note:** All diode cathodes are internally connected to the substrate.



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RRD-B30M115/Printed in U. S. A.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Input Voltage | 30V |
| Positive Analog Signal Voltage | 30V |
| Negative Analog Signal Voltage | −15V |
| Diode Current | 10 mA |
| Drain Current | 30 mA |
| Power Dissipation | 500 mW |
| Operating Temp. Range | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temp. (Soldering, 10 seconds) | 300°C |

## Electrical Characteristics (Notes 2 and 3)

| Symbols | Parameter | Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{GSX}$ | Input Current "OFF" | $V_{GD}$ = 4.5V, $V_{SD}$ = 0.7V | 0.01 | 0.1 | nA |
| | | $V_{GD}$ = 11V, $V_{SD}$ = 0.7V | 0.01 | 0.2 | nA |
| | | $T_A$ = 85°C, $V_{GD}$ = 11V, $V_{SD}$ = 0.7V | | 10 | nA |
| $I_{D(OFF)}$ | Leakage Current "OFF" | $V_{SD}$ = 0.7V, $V_{GS}$ = 3.8V | 0.01 | 0.2 | nA |
| | | $T_A$ = 85°C | | 10 | nA |
| $I_{G(ON)}$ | Leakage Current "ON" | $V_{GD}$ = 0V, $I_S$ = 1 mA | 0.08 | 1 | nA |
| | | $T_A$ = 85°C | | 200 | nA |
| $I_{G(ON)}$ | Leakage Current "ON" | $V_{GD}$ = 0V, $I_S$ = 2 mA | 0.13 | 5 | nA |
| | | $T_A$ = 85°C | | 10 | μA |
| $I_{G(ON)}$ | Leakage Current "ON" | $V_{GD}$ = 0V, $I_S$ = −2 mA | 0.1 | 10 | nA |
| | | $T_A$ = 85°C | | 20 | μA |
| $r_{DS(ON)}$ | Drain-Source Resistance | $V_{GS}$ = 0.5V, $I_S$ = 2 mA | 90 | 150 | Ω |
| | | $T_A$ = +85°C | | 240 | Ω |
| $V_{DIODE}$ | Forward Diode Drop | $I_D$ = 0.5 mA | | 0.8 | V |
| $r_{DS(ON)}$ | Match | $V_{GS}$ = 0, $I_D$ = 1 mA | 2 | 20 | Ω |
| $T_{ON}$ | Turn "ON" Time | See ac Test Circuit | 150 | 500 | ns |
| $T_{OFF}$ | Turn "OFF" Time | See ac Test Circuit | 300 | 500 | ns |
| CT | Cross Talk | See ac Test Circuit | 120 | | dB |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

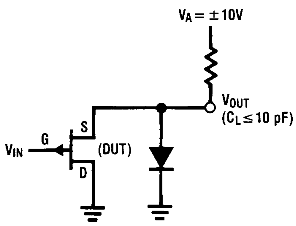
**Note 2:** Test conditions 25°C unless otherwise noted.

**Note 3:** "OFF" and "ON" notation refers to the conduction state of the FET switch.

**Note 4:** Thermal Resistance:
$\theta_{JA}$ (Junction to Ambient) ..........N/A
$\theta_{JC}$ (Junction to Case) .............N/A

# Test Circuits

### AC Test Circuit

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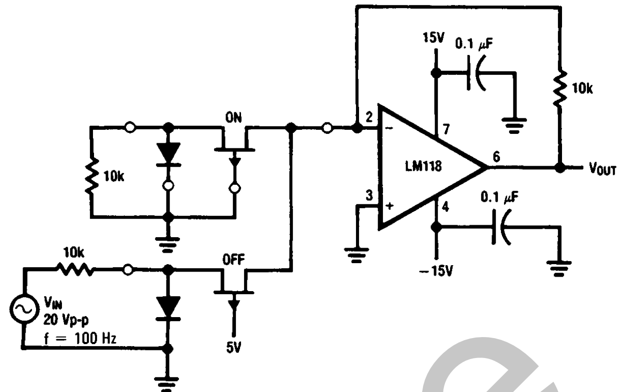
### Cross Talk Test Circuit

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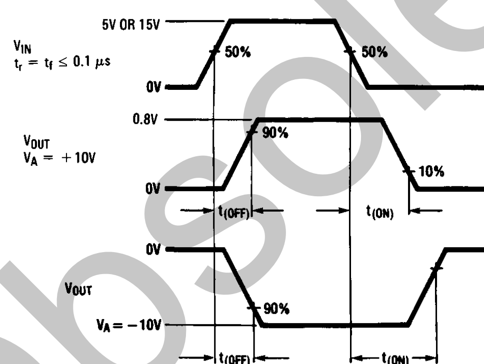
# Switching Time Waveforms

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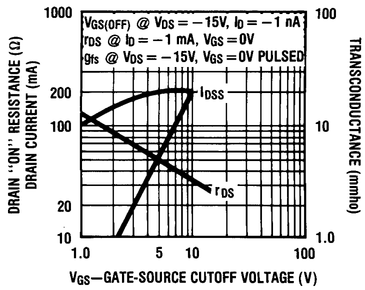
## Typical Performance Characteristics

### Parameter Interaction

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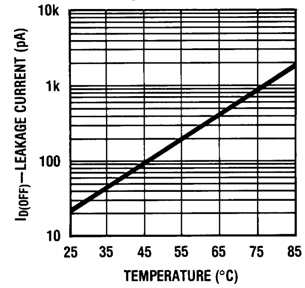
### Leakage Current, $I_{D(OFF)}$ vs Temperature

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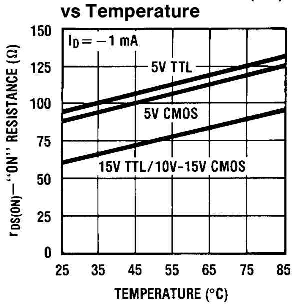
### "ON" Resistance, $r_{DS(ON)}$ vs Temperature

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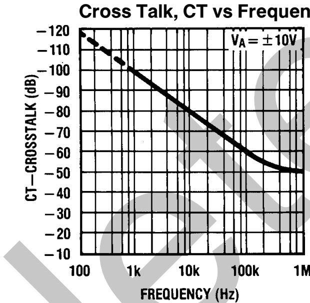
### Cross Talk, CT vs Frequency

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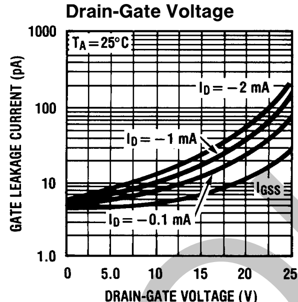
### Leakage Current vs Drain-Gate Voltage

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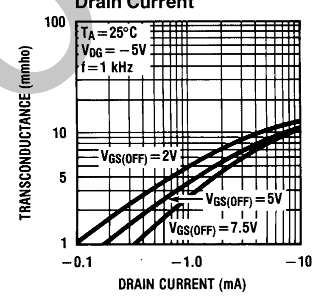
### Transconductance vs Drain Current

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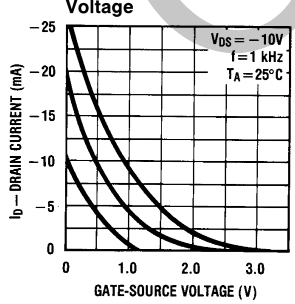
### Drain Current vs Bias Voltage

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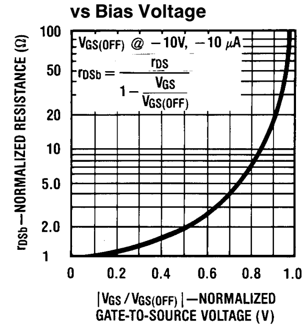
### Normalized Drain Resistance vs Bias Voltage

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## Applications Information

### THEORY OF OPERATION

The AH5020 analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL.

If only one of the two switches in each package is used to apply an input signal to the input of an op amp, the other switch FET can be placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = -\frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 2Ω resulting in a gain accuracy of 0.02% (for R1 = R2 = 10 kΩ).

### NOISE IMMUNITY

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With $V_{IN}$ = 15V and the $V_A$ = 10V, the source of Q1 is clamped to about 0.7V by the diode ($V_{GS}$ = 14.3V) ensuring that ac signals imposed on the 10V input will not gate the FET "ON".

### SELECTION OF GAIN SETTING RESISTORS

Since the AH5020 analog switches are operated in current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as $I_S$ approaches $I_{DSS}$. A practical rule of thumb is to maintain $I_S$ at less than 1⁄10 of $I_{DSS}$.

Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\,A_D}{I_{G(ON)}} \qquad (2a)$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \qquad (2b)$$

whichever is larger.

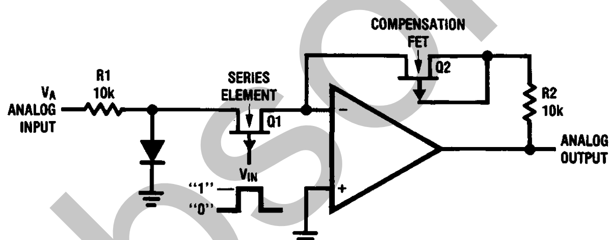


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FIGURE 1. Use of Compensation FET

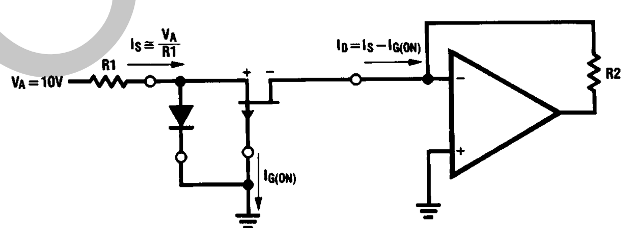


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FIGURE 2. On Leakage Current, $I_{G(ON)}$

## Applications Information (Continued)

Where $V_{A(MAX)}$ = Peak amplitude of the analog input signal
$A_D$ = Desired accuracy
$I_{G(ON)}$ = Leakage at a given $I_S$
$I_{DSS}$ = Saturation current of the FET switch = 20 mA

In a typical application, $V_A$ might $= \pm 10V$, $A_D = 0.1\%$, 0°C $\leq T_A \leq$ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{10V}{\frac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1 \mu A$ at 85°C for the AH5020. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

Where $V_{A(MIN)}$ = Minimum value for the analog input signal
$A_D$ = Desired accuracy
N = Number of channels
$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, $A_D = 0.1\%$, and $I_{D(OFF)} \leq$ 10 nA at 85°C for the AH5020. $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp — all of which should be considered in setting the overall gain accuracy of the circuit.

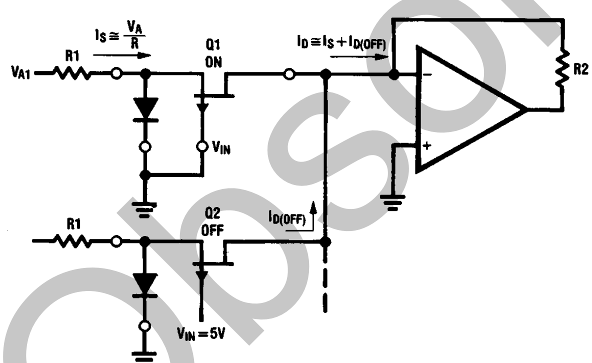


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**FIGURE 3. Off Leakage Current, $I_{D(OFF)}$**

## Applications Information (Continued)

**TTL COMPATIBILITY**

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the AH5020, a pull-up resistor, $R_{EXT}$ of at least 10 kΩ should be placed between the 5V $V_{cc}$ and the gate output as shown in *Figure 4*.

**DEFINITION OF TERMS**

The terms referred to in the electrical characteristics tables are as defined in *Figure 5*.

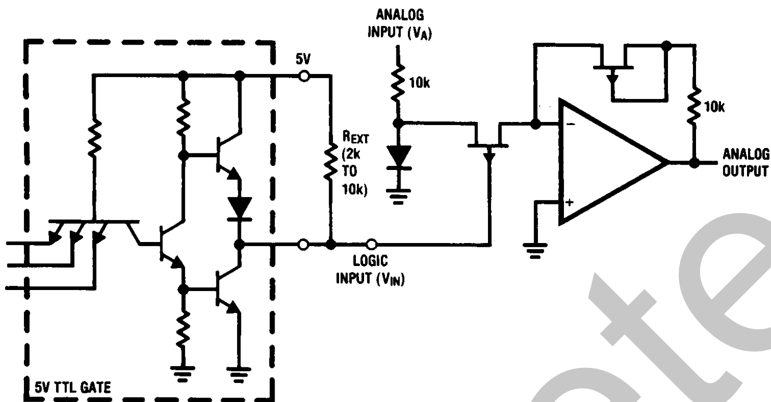


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**FIGURE 4. Interfacing with +5V TTL**

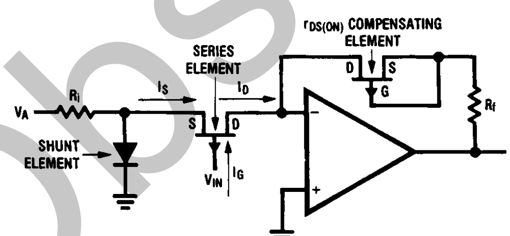


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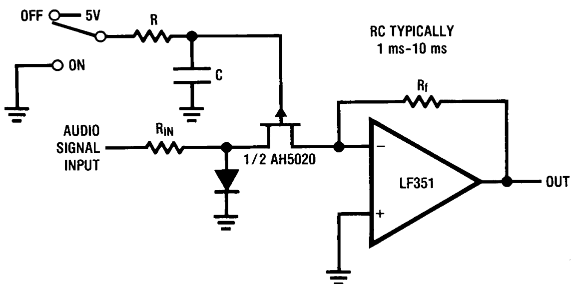
**FIGURE 5. Definition of Terms**

## Typical Applications

**Deglitched Switch for Noiseless Audio Switching**

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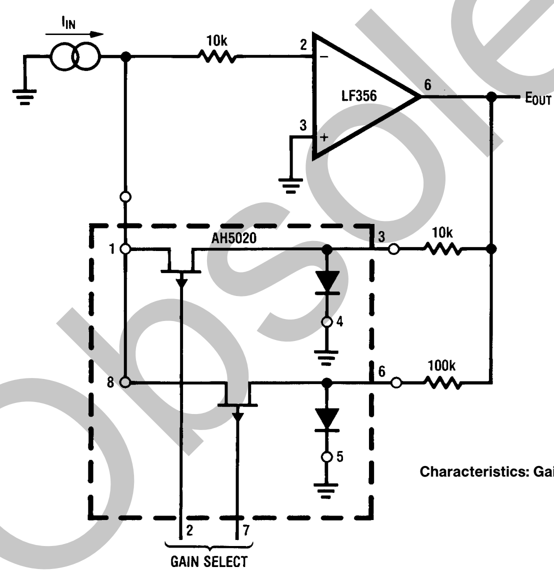
**Gain Programmable Amplifier**




Characteristics: Gain $= \frac{-E_{OUT}}{I_{IN}} = R_{FS}$

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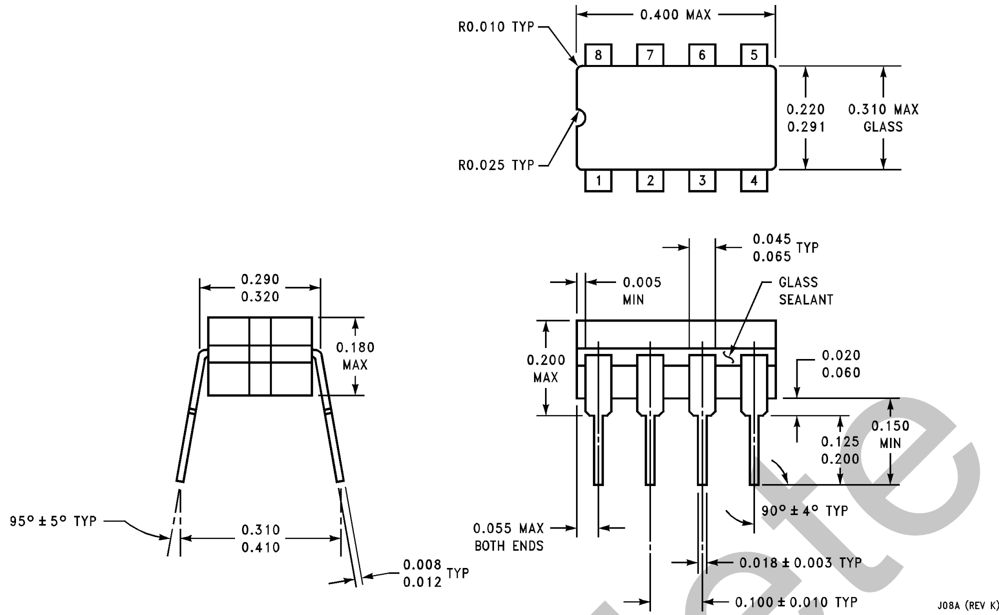
## Physical Dimensions inches (millimeters)




**Cavity Dual-In-Line Package (J)**
**Order Number AH5020CJ**
**NS Package Number J08A**



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**National Semiconductor Corporation**
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

**National Semiconductor Europe**
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
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**National Semiconductor Hong Kong Ltd.**
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
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