

16-BIT, 750-kHz, UNIPOLAR INPUT, MICRO POWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

FEATURES

- 750-KSPS Sample Rate
- High Linearity:
 - +0.9 LSB INL Typ, ± 1.5 LSB Max
 - -0.4/+0.6 LSB DNL Typ, ± 1 LSB Max
- Onboard Reference Buffer and Conversion Clock
- 0 V to 4.096 V Unipolar Inputs
- Low Noise: 88 dB SNR
- High Dynamic Range: 110 dB SFDR
- Very Low Offset and Offset Drift
- Low Power: 130 mW at 750 KSPS
- Wide Buffer Supply, 2.7 V to 5.25 V
- Flexible 8-/16-Bit Parallel Interface
- Direct Pin Compatible With ADS8381/ADS8383
- 48-Pin TQFP Package

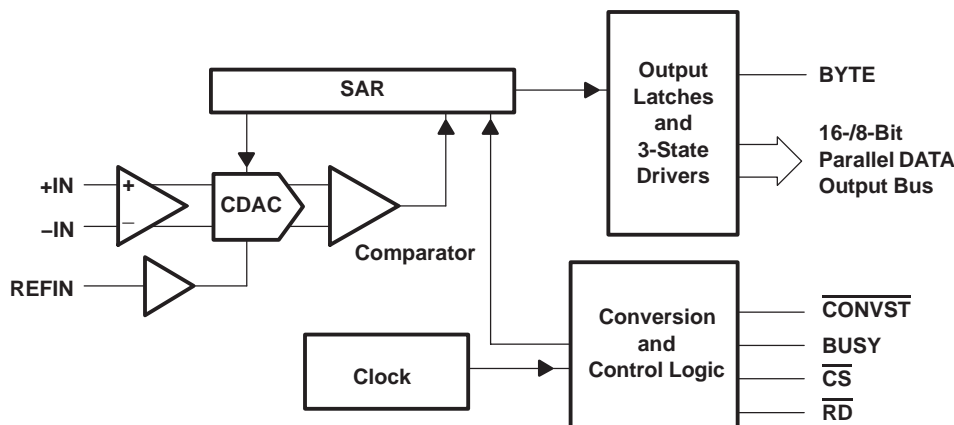
APPLICATIONS

- Medical Instruments
- Optical Networking
- Transducer Interface
- High Accuracy Data Acquisition Systems
- Magnetometers

DESCRIPTION

The ADS8371 is an 16-bit, 750 kHz A/D converter. The device includes a 16-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8371 offers a full 16-bit interface or an 8-bit bus option using two read cycles.

The ADS8371 is available in a 48-lead TQFP package and is characterized over the industrial -40°C to 85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ADS8371

SLAS390B – JUNE 2003 – REVISED FEBRUARY 2005



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

| MODEL | MAXIMUM INTEGRAL LINEARITY (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | NO MISSING CODES RESOLUTION (BIT) | PACKAGE TYPE | PACKAGE DESIGNATOR | TEMPERATURE RANGE | ORDERING INFORMATION | TRANSPORT MEDIA QUANTITY |
|-----------|----------------------------------|--------------------------------------|-----------------------------------|--------------|--------------------|-------------------|----------------------|--------------------------|
| ADS8371I | ±2.5 | -1/1.5 | 16 | 48 Pin TQFP | PFB | -40°C to 85°C | ADS8371IPFBT | Tape and reel 250 |
| | | | | | | | ADS8371IPFBR | Tape and reel 1000 |
| ADS8371IB | ±1.5 | ±1 | 16 | 48 Pin TQFP | PFB | -40°C to 85°C | ADS8371IBPFBT | Tape and reel 250 |
| | | | | | | | ADS8371IBPFBR | Tape and reel 1000 |

NOTE: For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | | UNIT |
|--|-----------------------------------|--|
| Voltage | +IN to AGND | -0.4 V to +VA + 0.1 V |
| | -IN to AGND | -0.4 V to 0.5 V |
| Voltage range | +VA to AGND | -0.3 V to 7 V |
| | +VBD to BDGND | -0.3 V to 7 V |
| | +VA to +VBD | -0.3 V to 2.55 V |
| Digital input voltage to BDGND | | -0.3 V to +VBD + 0.3 V |
| Digital output voltage to BDGND | | -0.3 V to +VBD + 0.3 V |
| Operating free-air temperature range, T _A | | -40°C to 85°C |
| Storage temperature range, T _{stg} | | -65°C to 150°C |
| Junction temperature (T _J max) | | 150°C |
| TQFP package | Power dissipation | (T _J Max - T _A)/θ _{JA} |
| | θ _{JA} thermal impedance | 86°C/W |
| Lead temperature, soldering | Vapor phase (60 sec) | 215°C |
| | Infrared (15 sec) | 220°C |

⁽¹⁾ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS
 $T_A = -40^{\circ}\text{C}$ to 85°C , $+V_A = 5\text{ V}$, $+V_{BD} = 3\text{ V}$ or 5 V , $V_{ref} = 4.096\text{ V}$, $f_{SAMPLE} = 750\text{ kHz}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | ADS8371IB | | | ADS8371I | | | UNIT |
|--|-----------------------|-----------|------------|-----------------|----------|-----------|-----------------|-------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Analog Input | | | | | | | | |
| Full-scale input voltage (see Note 1) | +IN – –IN | 0 | | V_{ref} | 0 | | V_{ref} | V |
| Absolute input voltage | +IN | –0.2 | | $V_{ref} + 0.2$ | –0.2 | | $V_{ref} + 0.2$ | V |
| | –IN | –0.2 | | 0.2 | –0.2 | | 0.2 | |
| Input capacitance | | | 45 | | | 45 | | pF |
| Input leakage current | | | 1 | | | 1 | | nA |
| System Performance | | | | | | | | |
| Resolution | | | 16 | | | 16 | | Bits |
| No missing codes | | 16 | | | 16 | | | Bits |
| Integral linearity (see Notes 2 and 3) | | –1.5 | –0.8/0.9 | 1.5 | –2.5 | | 2.5 | LSB |
| Differential linearity | | –1 | –0.4/0.6 | 1 | –1 | | 1.5 | LSB |
| Offset error | | –0.75 | ± 0.25 | 0.75 | –1 | ± 0.5 | 1 | mV |
| Gain error (see Note 4) | | –0.075 | | 0.075 | –0.15 | | 0.15 | %FS |
| Noise | | | 60 | | | 60 | | $\mu\text{V RMS}$ |
| Power supply rejection ratio | At 3FFFFh output code | | 75 | | | 75 | | dB |
| Sampling Dynamics | | | | | | | | |
| Conversion time | | | | 1.13 | | | 1.13 | μs |
| Acquisition time | | 0.2 | | | 0.2 | | | μs |
| Throughput rate | | | | 750 | | | 750 | kHz |
| Aperture delay | | | 4 | | | 4 | | ns |
| Aperture jitter | | | 15 | | | 15 | | ps |
| Step response | | | 150 | | | 150 | | ns |
| Over voltage recovery | | | 150 | | | 150 | | ns |

(1) Ideal input span, does not include gain or offset error.

(2) LSB means least significant bit

(3) This is endpoint INL, not best fit.

(4) Measured relative to an ideal full-scale input (+IN – –IN) of 4.096 V

ADS8371

SLAS390B – JUNE 2003 – REVISED FEBRUARY 2005

SPECIFICATIONS (CONTINUED)

 $T_A = -40^{\circ}\text{C}$ to 85°C , $+V_A = +5\text{ V}$, $+V_{BD} = 3\text{ V}$ or 5 V , $V_{\text{ref}} = 4.096\text{ V}$, $f_{\text{SAMPLE}} = 750\text{ kHz}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | ADS8371IB | | | ADS8371I | | | UNIT |
|---|------------------------|-----------|-------|-----|----------|-------|-----|------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
| Dynamic Characteristics | | | | | | | | |
| Total harmonic distortion (THD) (see Note 1) | 1 kHz | | -106 | | | -100 | | dB |
| | 10 kHz | | -99 | | | -96 | | |
| | 50 kHz | | -92 | | | -90 | | |
| | 100 kHz | | -90 | | | -88 | | |
| Signal to noise ratio (SNR) (see Note 1) | 1 kHz | | 87.7 | | | 87 | | dB |
| | 10 kHz | | 87.5 | | | 87 | | |
| | 50 kHz | | 87.2 | | | 87 | | |
| | 100 kHz | | 87 | | | 87 | | |
| Signal to noise + distortion (SINAD) (see Note 1) | 1 kHz | | 87.6 | | | 87 | | dB |
| | 10 kHz | | 87 | | | 86 | | |
| | 50 kHz | | 86 | | | 85 | | |
| | 100 kHz | | 85 | | | 84 | | |
| Spurious free dynamic range (SFDR) (see Note 1) | 1 kHz | | 110 | | | 106 | | dB |
| | 10 kHz | | 100 | | | 97 | | |
| | 50 kHz | | 95 | | | 92 | | |
| | 100 kHz | | 94 | | | 90 | | |
| -3dB Small signal bandwidth | | | 3 | | | 3 | | MHz |
| Voltage Reference Input | | | | | | | | |
| Reference voltage at REFIN, V_{ref} | | 2.5 | 4.096 | 4.2 | 2.5 | 4.096 | 4.2 | V |
| Reference resistance (see Note 2) | | | 500 | | | 500 | | k Ω |
| Reference current drain | $f_s = 750\text{ kHz}$ | | | 1 | | | 1 | mA |

(1) Calculated on the first nine harmonics of the input frequency

 (2) Can vary $\pm 20\%$

SPECIFICATIONS (CONTINUED)
 $T_A = -40^\circ\text{C}$ to 85°C , $+V_A = +5\text{ V}$, $+V_{BD} = 3\text{ V}$ or 5 V , $V_{\text{ref}} = 4.096\text{ V}$, $f_{\text{SAMPLE}} = 750\text{ kHz}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------|-------------------------------|-----------------|-----|-----------------|------------------|
| Digital Input/Output | | | | | | |
| Logic family | | | CMOS | | | |
| Logic level | V_{IH} | $I_{IH} = 5\ \mu\text{A}$ | $+V_{BD}-1$ | | $+V_{BD} + 0.3$ | V |
| | V_{IL} | $I_{IL} = 5\ \mu\text{A}$ | -0.3 | | 0.8 | |
| | V_{OH} | $I_{OH} = 2\text{ TTL loads}$ | $+V_{BD} - 0.6$ | | | |
| | V_{OL} | $I_{OL} = 2\text{ TTL loads}$ | | | 0.4 | |
| Data format | | | Straight Binary | | | |
| Power Supply Requirements | | | | | | |
| Power supply voltage | +VBD Buffer supply | | 2.7 | 3.3 | 5.25 | V |
| | +VA Analog Supply | | 4.75 | 5 | 5.25 | V |
| Supply current, 750-kHz sample rate (1) | | | | 26 | 28 | mA |
| Power dissipation, 750-kHz sample rate (1) | | | | 130 | 140 | mW |
| Temperature Range | | | | | | |
| Operating free-air | | | -40 | | 85 | $^\circ\text{C}$ |

(1) This includes only +VA current. +VBD current is typical 1 mA with 5 pF load capacitance on all output pins.

ADS8371

SLAS390B – JUNE 2003 – REVISED FEBRUARY 2005

TIMING CHARACTERISTICS

 All specifications typical at -40°C to 85°C , $+V_A = +V_{BD} = 5\text{ V}$ (see Notes 1, 2, and 3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--|--|-------------------------|------------------------|------|---------------|
| t_{CONV} | Conversion time | | | 1.13 | μs |
| t_{ACQ} | Acquisition time | 0.2 | | | μs |
| t_{HOLD} | Sampling capacitor hold time | | | 25 | ns |
| t_{pd1} | $\overline{\text{CONVST}}$ low to conversion started (BUSY high) | | | 45 | ns |
| t_{pd2} | Propagation delay time, End of conversion to BUSY low | | | 20 | ns |
| t_{pd3} | Propagation delay time, from start of conversion (internal state) to rising edge of BUSY | | | 20 | ns |
| t_{w1} | Pulse duration, $\overline{\text{CONVST}}$ low | 40 | | 400 | ns |
| t_{su1} | Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low | 20 | | | ns |
| t_{w2} | Pulse duration, $\overline{\text{CONVST}}$ high | 20 | | | ns |
| | $\overline{\text{CONVST}}$ falling edge jitter | | | 10 | ps |
| t_{w3} | Pulse duration, BUSY signal low | Min(t_{ACQ}) | | | μs |
| t_{w4} | Pulse duration, BUSY signal high | | | 1.13 | μs |
| t_{h1} | Hold time, First data bus data transition ($\overline{\text{CS}}$ low for read cycle, or $\overline{\text{RD}}$ or BYTE input changes) after $\overline{\text{CONVST}}$ low | 40 | | 400 | ns |
| t_{d1} | Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low | 0 | | | ns |
| t_{su2} | Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high | 0 | | | ns |
| t_{w5} | Pulse duration, $\overline{\text{RD}}$ low time | 50 | | | ns |
| t_{en} | Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid | | | 20 | ns |
| t_{d2} | Delay time, data hold from $\overline{\text{RD}}$ high | 5 | | | ns |
| t_{d3} | Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid | 10 | | 20 | ns |
| t_{w6} | Pulse duration, $\overline{\text{RD}}$ high | 20 | | | ns |
| t_{w7} | Pulse duration, $\overline{\text{CS}}$ high time | 20 | | | ns |
| t_{h2} | Hold time, last $\overline{\text{CS}}$ rising edge or changes of $\overline{\text{RD}}$ or BYTE to $\overline{\text{CONVST}}$ falling edge | 125 | | | ns |
| t_{pd4} | Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge | | Max(t_{d5}) | | ns |
| t_{su3} | Setup time, BYTE transition to $\overline{\text{RD}}$ falling edge | 10 | | | ns |
| t_{h3} | Hold time, BYTE transition to $\overline{\text{RD}}$ falling edge | 10 | | | ns |
| t_{dis} | Disable time, $\overline{\text{RD}}$ High ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus | | | 20 | ns |
| t_{d5} | Delay time, BUSY low to MSB data valid | | | 30 | ns |
| t_{su5} | Setup time, BYTE transition to next BYTE transition | 50 | | | ns |
| $t_{\text{su(AB)}}$ | Setup time, from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when $\overline{\text{CS}} = 0$ and $\overline{\text{CONVST}}$ used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort). | 65 | | 700 | ns |
| $t_{\text{f(}(\overline{\text{CONVST}})$ | Falling time, ($\overline{\text{CONVST}}$ falling edge) | 10 | | 30 | ns |
| t_{su6} | Setup time, $\overline{\text{CS}}$ falling edge to $\overline{\text{CONVST}}$ falling edge when $\overline{\text{RD}} = 0$ | 125 | | | ns |

 (1) All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of $+V_{BD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$ except for $\overline{\text{CONVST}}$.

(2) See timing diagrams.

(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

TIMING CHARACTERISTICS

All specifications typical at -40°C to 85°C , $+V_A = 5\text{ V}$, $+V_{BD} = 3\text{ V}$ (see Notes 1, 2, and 3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------------|--|------------------------|-----|------|------|
| t _{CONV} | Conversion time | | | 1.13 | μs |
| t _{ACQ} | Acquisition time | 0.2 | | | μs |
| t _{HOLD} | Sampling capacitor hold time | | | 25 | ns |
| t _{pd1} | $\overline{\text{CONVST}}$ low to conversion started (BUSY high) | | | 50 | ns |
| t _{pd2} | Propagation delay time, end of conversion to BUSY low | | | 25 | ns |
| t _{pd3} | Propagation delay time, from start of conversion (internal state) to rising edge of BUSY | | | 25 | ns |
| t _{w1} | Pulse duration, $\overline{\text{CONVST}}$ low | 40 | | 400 | ns |
| t _{su1} | Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low | 20 | | | ns |
| t _{w2} | Pulse duration, $\overline{\text{CONVST}}$ high | 20 | | | ns |
| | $\overline{\text{CONVST}}$ falling edge jitter | | | 10 | ps |
| t _{w3} | Pulse duration, BUSY signal low | Min(t _{ACQ}) | | | μs |
| t _{w4} | Pulse duration, BUSY signal high | | | 1.13 | μs |
| t _{h1} | Hold time, first data bus transition ($\overline{\text{CS}}$ low for read cycle, or $\overline{\text{RD}}$ or BYTE input changes) after $\overline{\text{CONVST}}$ low | 40 | | 400 | ns |
| t _{d1} | Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low | 0 | | | ns |
| t _{su2} | Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high | 0 | | | ns |
| t _{w5} | Pulse duration, $\overline{\text{RD}}$ low | 50 | | | ns |
| t _{en} | Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid | | | 30 | ns |
| t _{d2} | Delay time, data hold from $\overline{\text{RD}}$ high | 10 | | | ns |
| t _{d3} | Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid | 10 | | 30 | ns |
| t _{w6} | Pulse duration, $\overline{\text{RD}}$ high time | 20 | | | ns |
| t _{w7} | Pulse duration, $\overline{\text{CS}}$ high time | 20 | | | ns |
| t _{h2} | Hold time, last $\overline{\text{CS}}$ rising edge or changes of $\overline{\text{RD}}$, or BYTE to $\overline{\text{CONVST}}$ falling edge | 125 | | | ns |
| t _{pd4} | Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge | Max(td5) | | | ns |
| t _{su3} | Setup time, BYTE transition to $\overline{\text{RD}}$ falling edge | 10 | | | ns |
| t _{h3} | Hold time, BYTE transition to $\overline{\text{RD}}$ falling edge | 10 | | | ns |
| t _{dis} | Disable time, $\overline{\text{RD}}$ High ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus | | | 30 | ns |
| t _{d5} | Delay time, BUSY low to MSB data valid delay time | | | 40 | ns |
| t _{su5} | Setup time, BYTE transition to next BYTE transition | 50 | | | ns |
| t _{su(AB)} | Setup time, from the falling edge of $\overline{\text{CONVST}}$ (used to start the valid conversion) to the next falling edge of $\overline{\text{CONVST}}$ (when $\overline{\text{CS}} = 0$ and $\overline{\text{CONVST}}$ used to abort) or to the next falling edge of $\overline{\text{CS}}$ (when $\overline{\text{CS}}$ is used to abort). | 70 | | 700 | ns |
| t _{f(CONVST)} | Falling time, ($\overline{\text{CONVST}}$ falling edge) | 10 | | 30 | ns |
| t _{su6} | Setup time, $\overline{\text{CS}}$ falling edge to $\overline{\text{CONVST}}$ falling edge when $\overline{\text{RD}} = 0$ | 125 | | | ns |

(1) All input signals are specified with $t_r = t_f = 5\text{ ns}$ (10% to 90% of $+V_{BD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$ except for $\overline{\text{CONVST}}$.

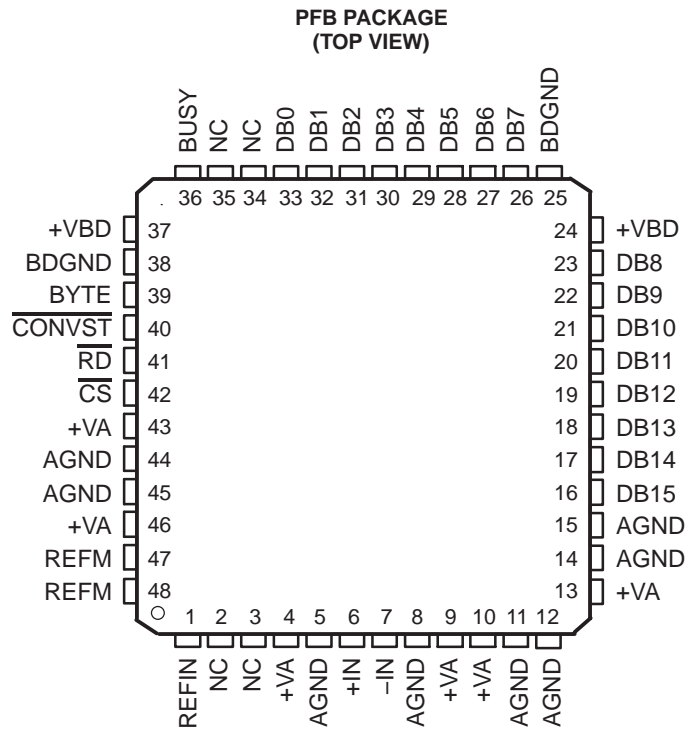
(2) See timing diagrams.

(3) All timing are measured with 10 pF equivalent loads on all data bits and BUSY pins.

ADS8371

SLAS390B – JUNE 2003 – REVISED FEBRUARY 2005

PIN ASSIGNMENTS



NC – No connection.

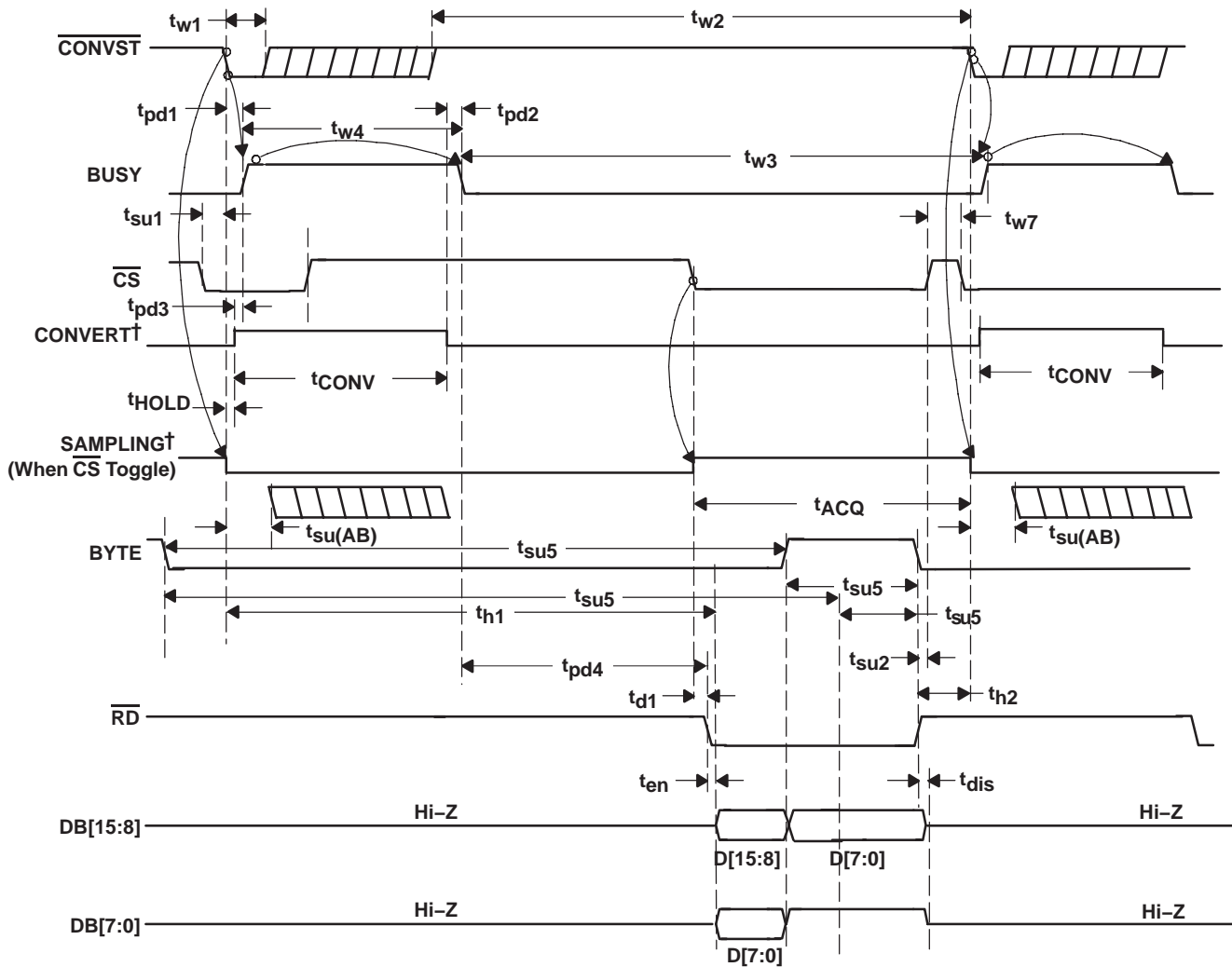
TERMINAL FUNCTIONS

| NAME | NO. | I/O | DESCRIPTION | | |
|----------------------------|---------------------------------|-----|---|----------|------------|
| AGND | 5, 8, 11, 12, 14, 15, 44, 45 | – | Analog ground | | |
| BDGND | 25, 38 | – | Digital ground for buffer supply | | |
| BUSY | 36 | O | Status output. High when a conversion is in progress. | | |
| BYTE | 39 | I | Byte select input. Used for 8-bit bus reading. 0: No fold back 1: Low byte D[7:0] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[15:8]. | | |
| $\overline{\text{CONVST}}$ | 40 | I | Convert start. The falling edge of this input ends the acquisition period and starts the hold period. | | |
| $\overline{\text{CS}}$ | 42 | I | Chip select. The falling edge of this input starts the acquisition period. | | |
| Data Bus | | | 8-Bit Bus | | 16-Bit Bus |
| | | | BYTE = 0 | BYTE = 1 | BYTE = 0 |
| DB15 | 16 | O | D15 (MSB) | D7 | D15 (MSB) |
| DB14 | 17 | O | D14 | D6 | D14 |
| DB13 | 18 | O | D13 | D5 | D13 |
| DB12 | 19 | O | D12 | D4 | D12 |
| DB11 | 20 | O | D11 | D3 | D11 |
| DB10 | 21 | O | D10 | D2 | D10 |
| DB9 | 22 | O | D9 | D1 | D9 |
| DB8 | 23 | O | D8 | D0 (LSB) | D8 |
| DB7 | 26 | O | D7 | All ones | D7 |
| DB6 | 27 | O | D6 | All ones | D6 |
| DB5 | 28 | O | D5 | All ones | D5 |
| DB4 | 29 | O | D4 | All ones | D4 |
| DB3 | 30 | O | D3 | All ones | D3 |
| DB2 | 31 | O | D2 | All ones | D2 |
| DB1 | 32 | O | D1 | All ones | D1 |
| DB0 | 33 | O | D0 (LSB) | All ones | D0 (LSB) |
| –IN | 7 | I | Inverting input channel | | |
| +IN | 6 | I | Non inverting input channel | | |
| NC | 2, 3, 34, 35 | – | No connection | | |
| REFIN | 1 | I | Reference input | | |
| REFM | 47, 48 | I | Reference ground | | |
| $\overline{\text{RD}}$ | 41 | I | Synchronization pulse for the parallel output. When $\overline{\text{CS}}$ is low, this serves as the output enable and puts the previous conversion result on the bus. | | |
| +VA | 4, 9, 10, 13, 43, 46 | – | Analog power supplies, 5-V dc | | |
| +VBD | 24, 37 | – | Digital power supply for the buffer | | |

ADS8371

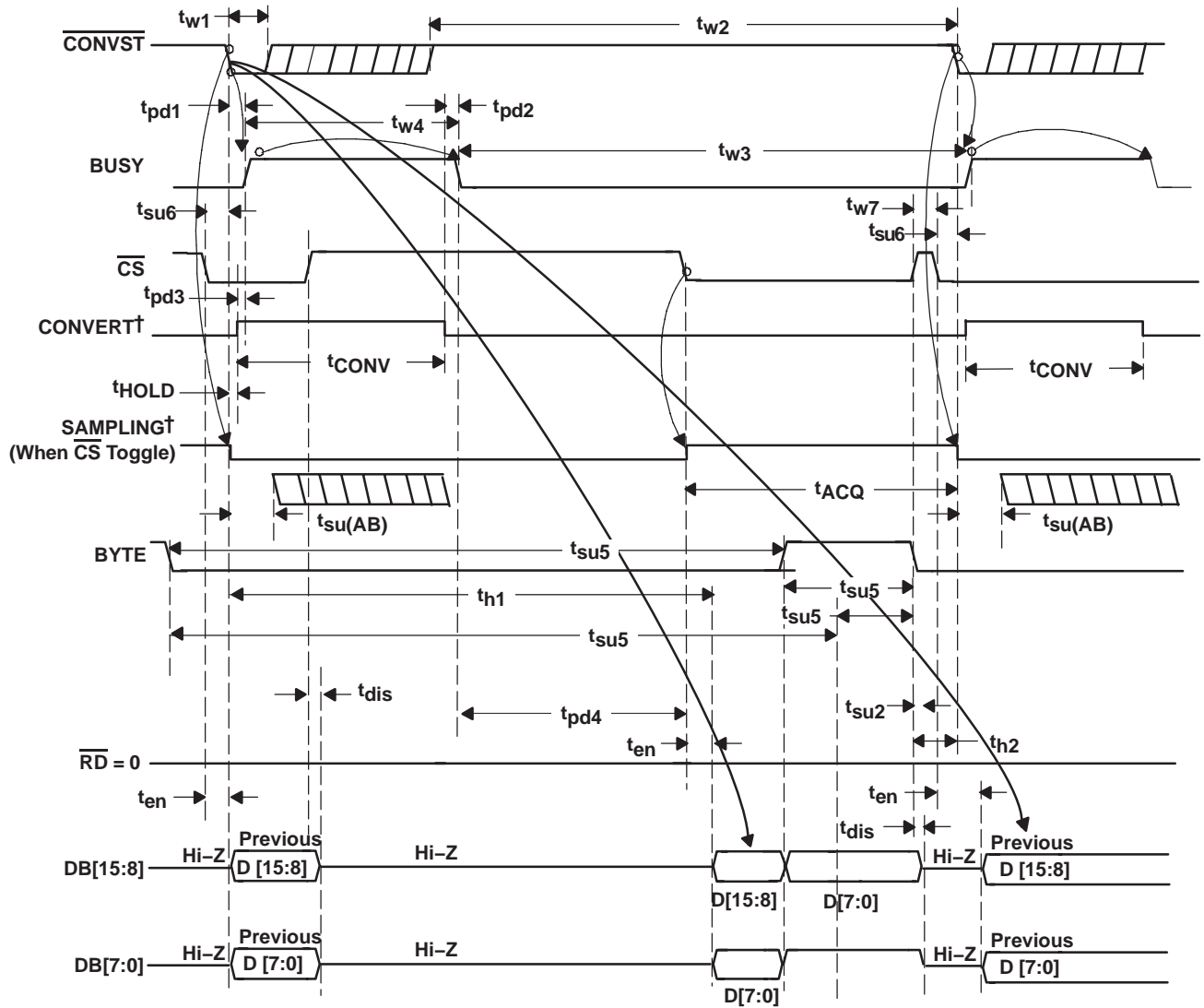
SLAS390B – JUNE 2003 – REVISED FEBRUARY 2005

TIMING DIAGRAMS



†Signal internal to device

Figure 1. Timing for Conversion and Acquisition Cycles With \overline{CS} and \overline{RD} Toggling

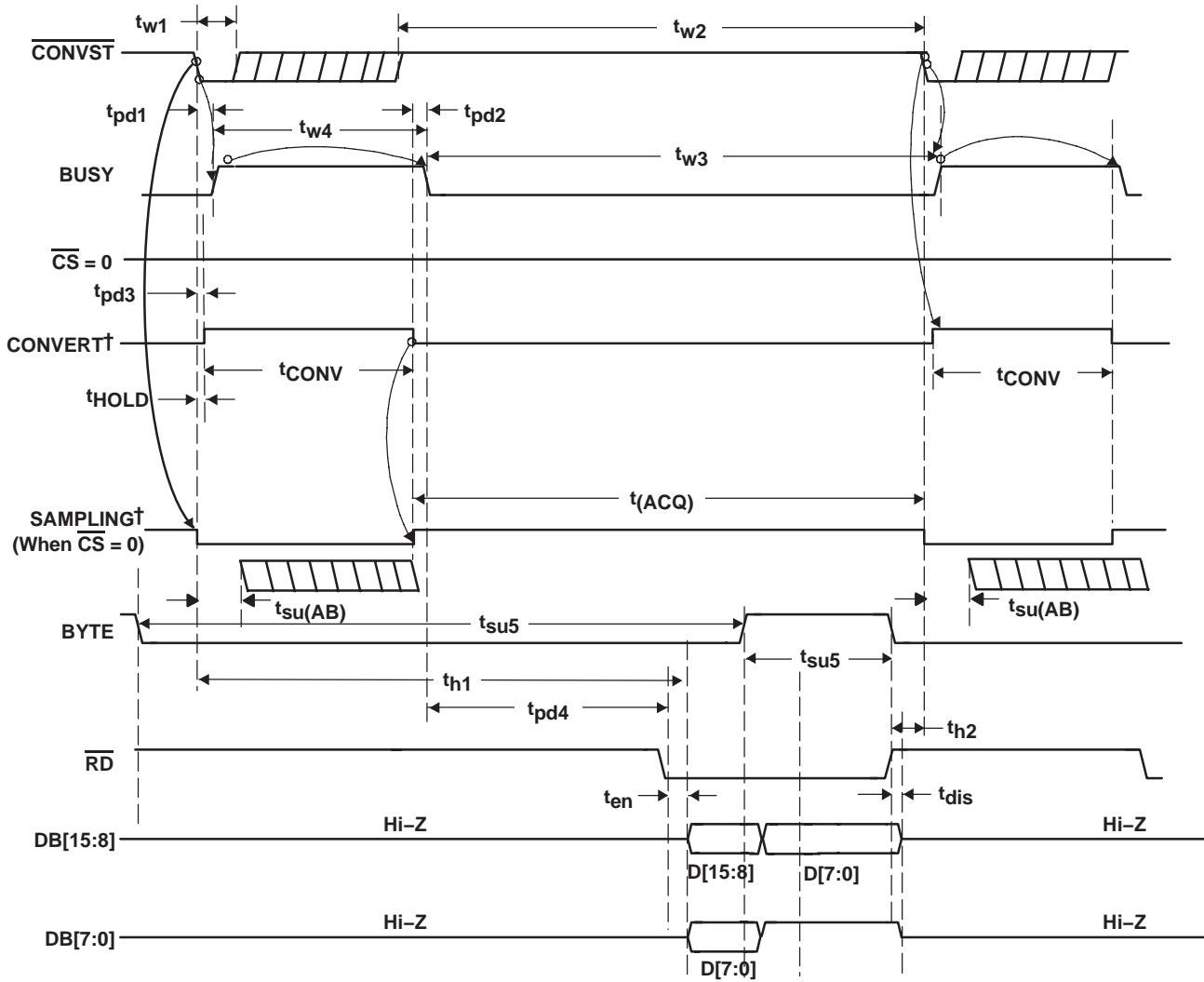


†Signal internal to device

Figure 2. Timing for Conversion and Acquisition Cycles With \overline{CS} Toggling, \overline{RD} Tied to BDGND

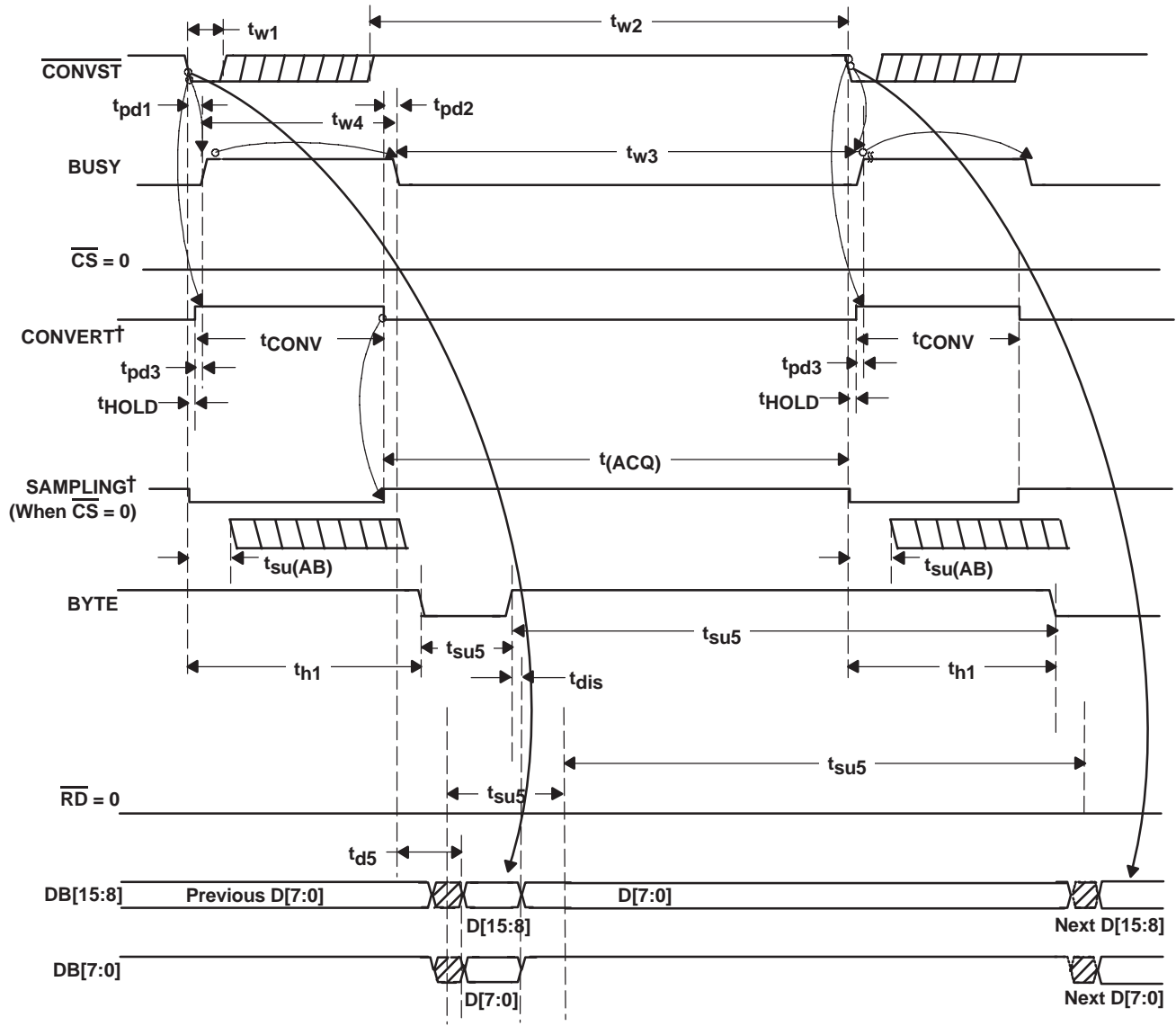
ADS8371

SLAS390B – JUNE 2003 – REVISED FEBRUARY 2005



†Signal internal to device

Figure 3. Timing for Conversion and Acquisition Cycles With \overline{CS} Tied to BDGND, \overline{RD} Toggling



†Signal internal to device

Figure 4. Timing for Conversion and Acquisition Cycles With \overline{CS} and \overline{RD} Tied to BDGND—Auto Read

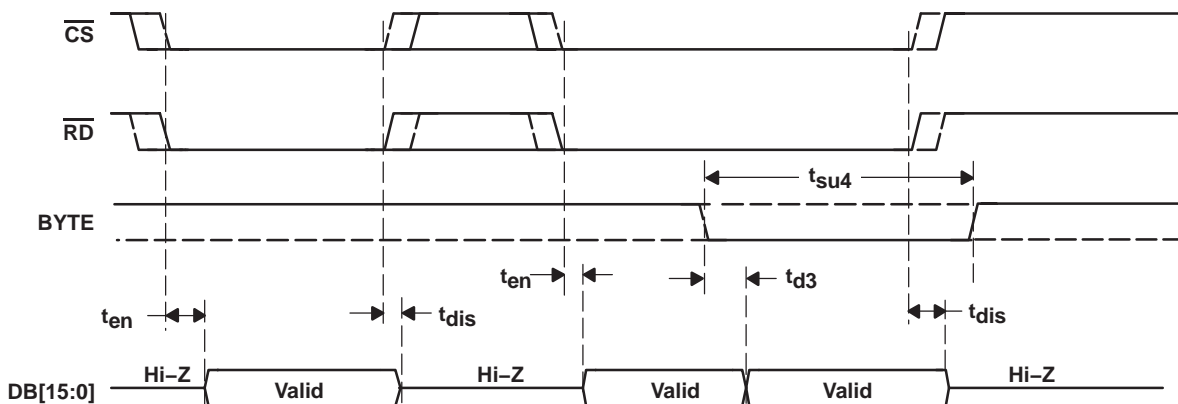


Figure 5. Detailed Timing for Read Cycles

TYPICAL CHARACTERISTICS(1)

HISTOGRAM (DC CODE SPREAD)
HALF SCALE 4096 CONVERSIONS

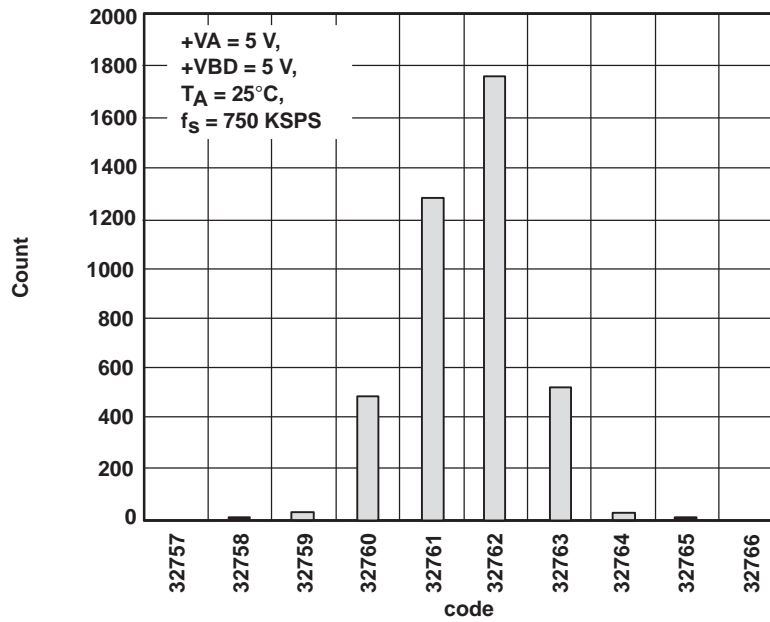


Figure 6

GAIN ERROR
vs
FREE-AIR TEMPERATURE

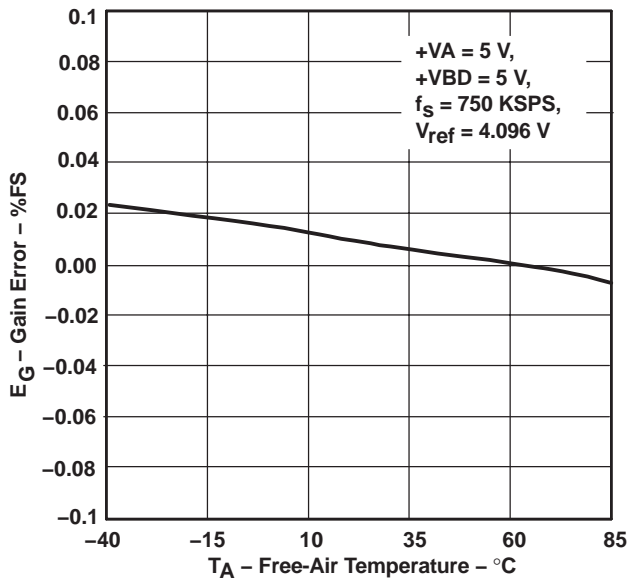


Figure 7

GAIN ERROR
vs
FREE-AIR TEMPERATURE

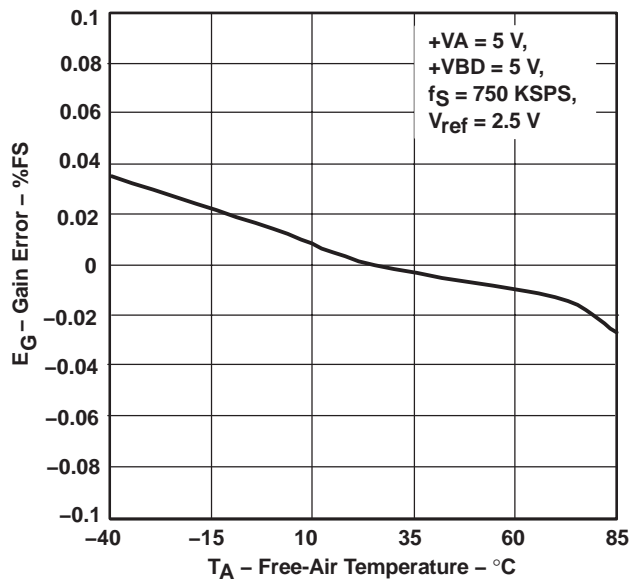
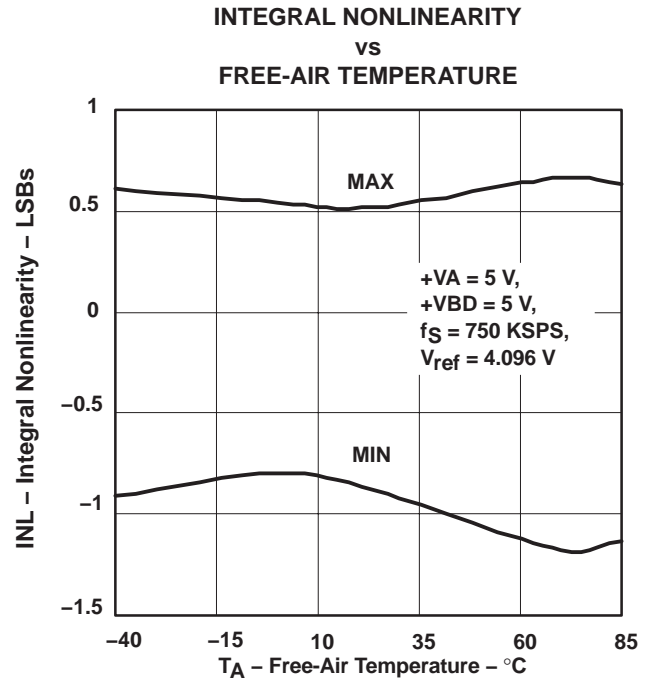
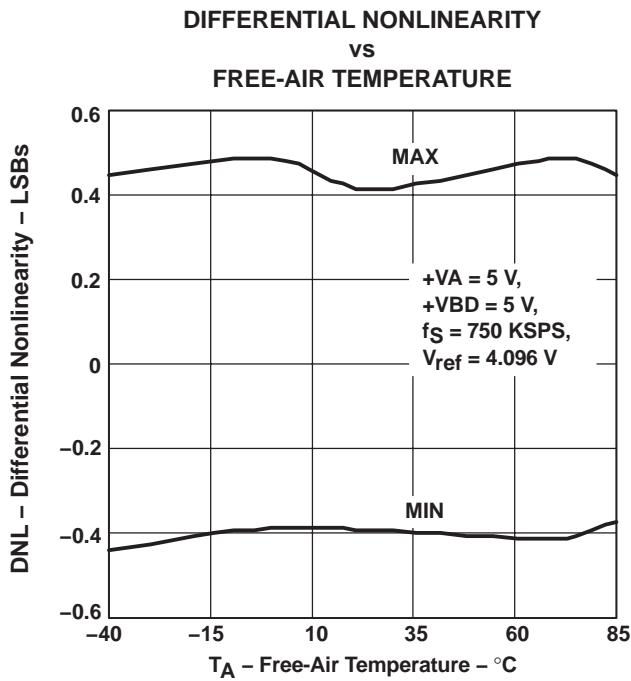
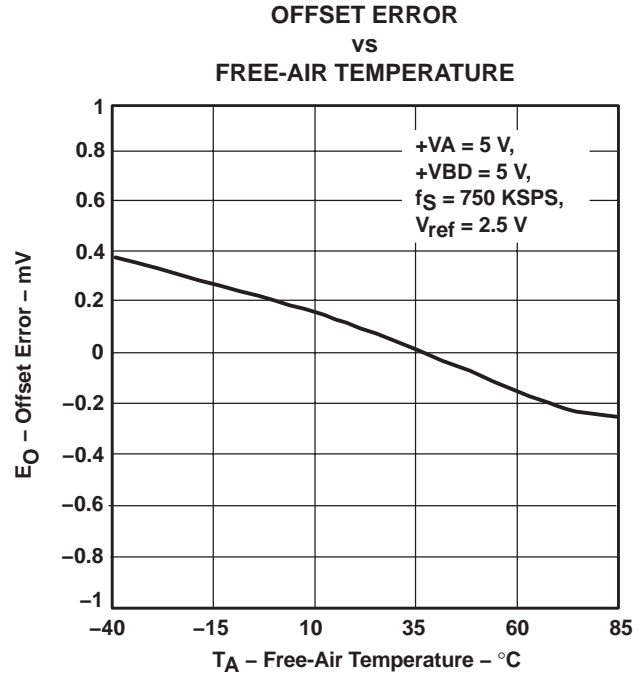
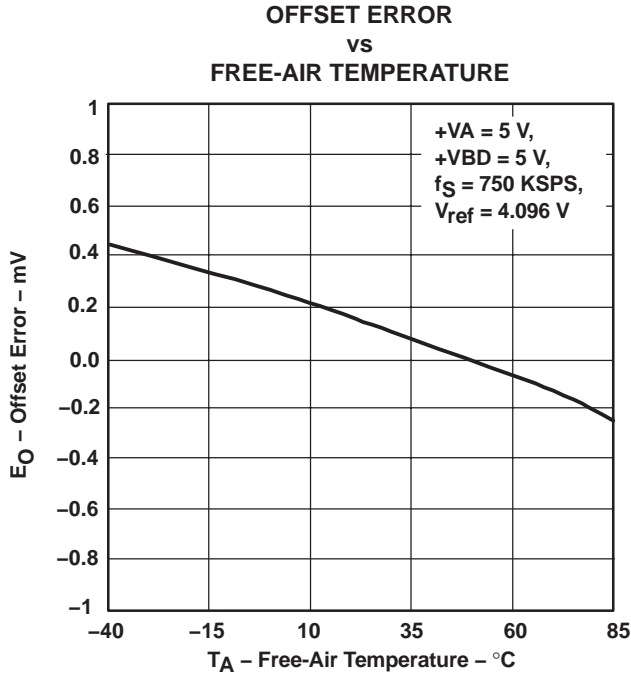


Figure 8



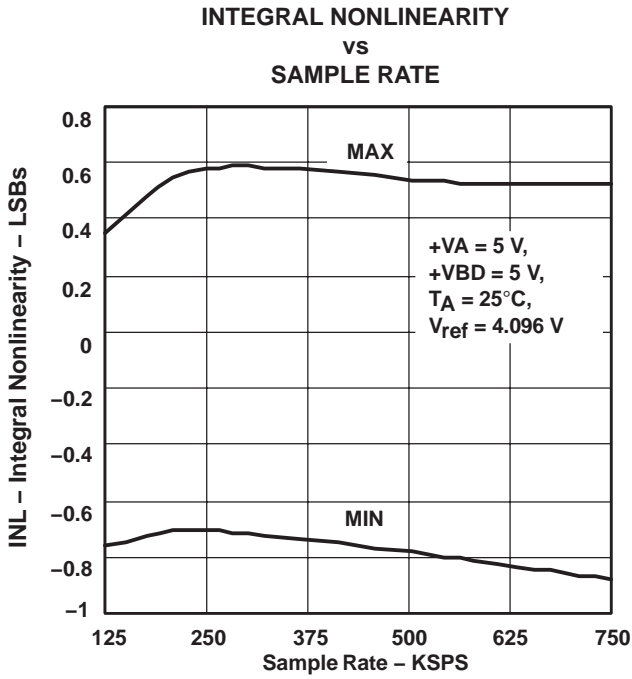


Figure 13

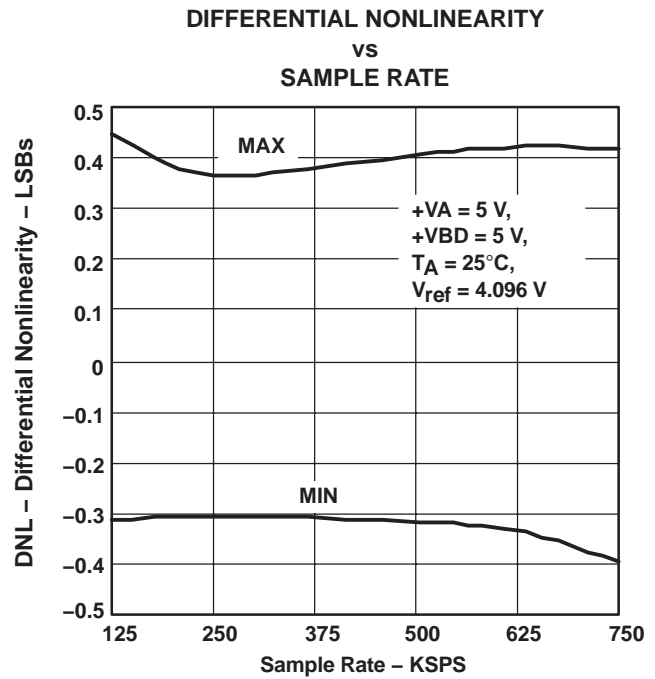


Figure 14

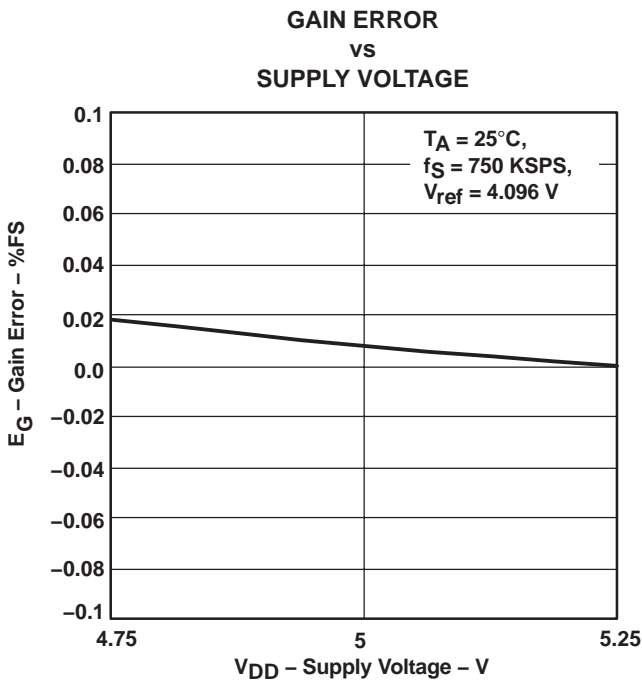


Figure 15

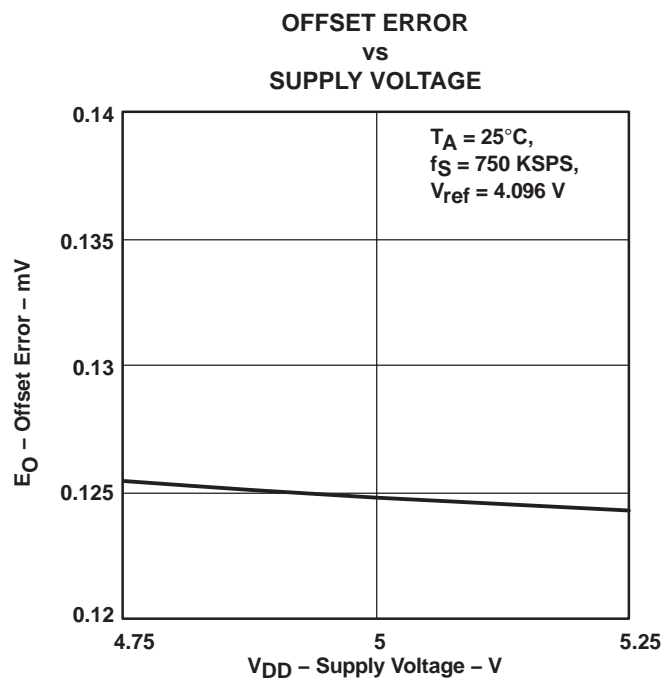
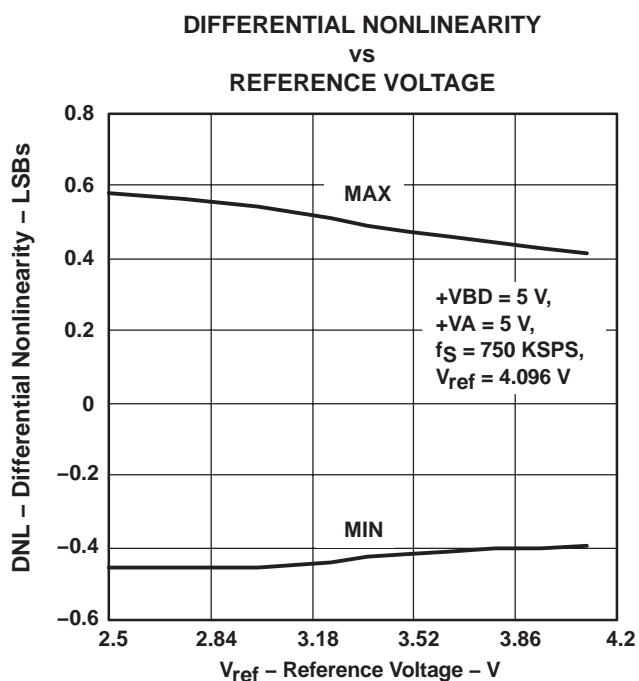
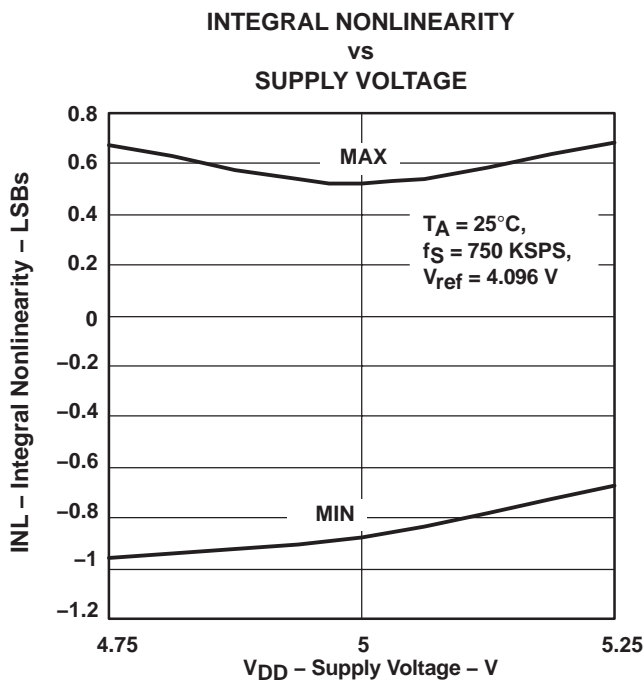
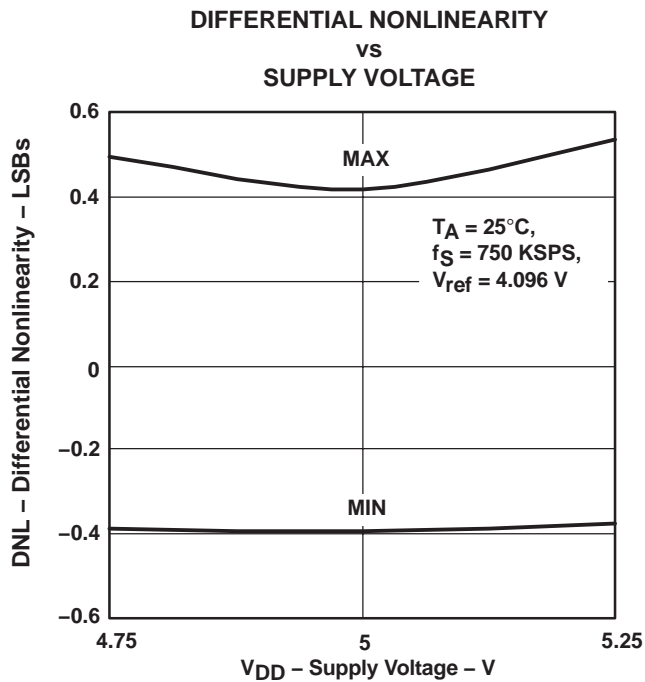
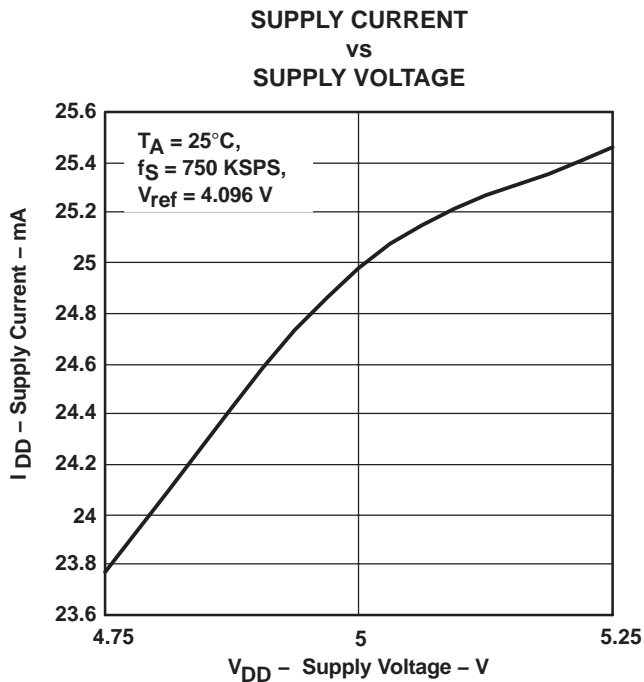
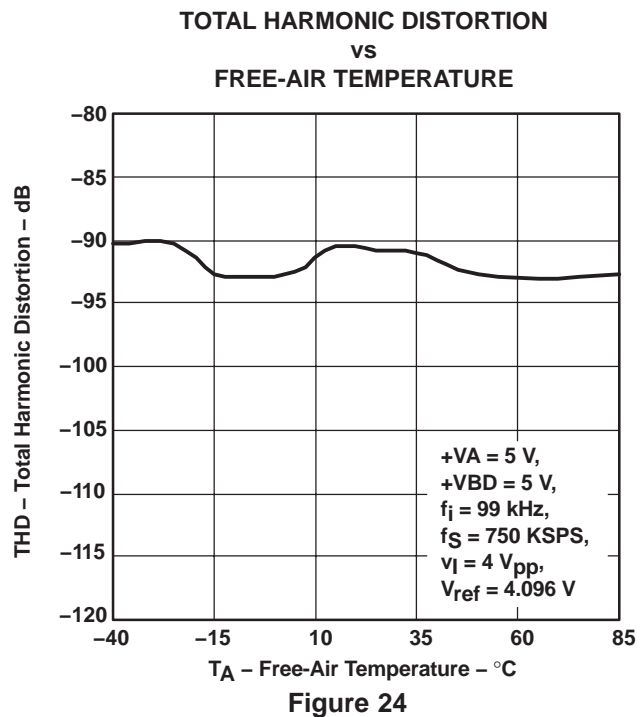
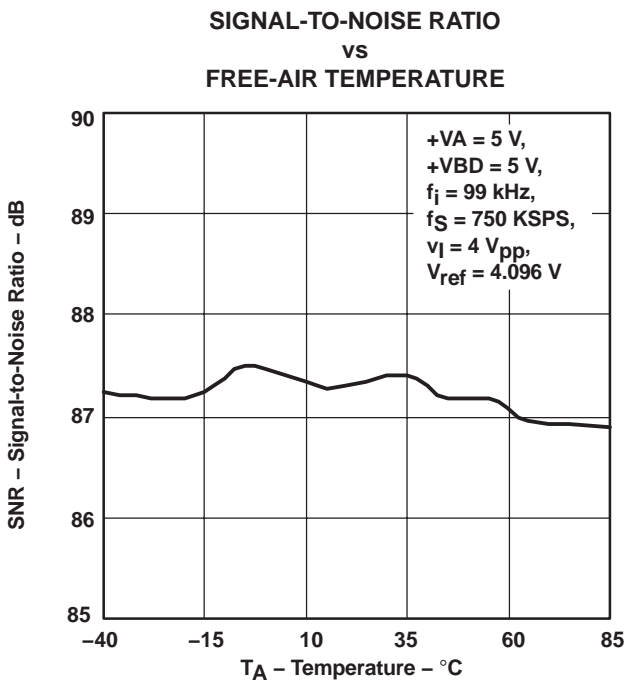
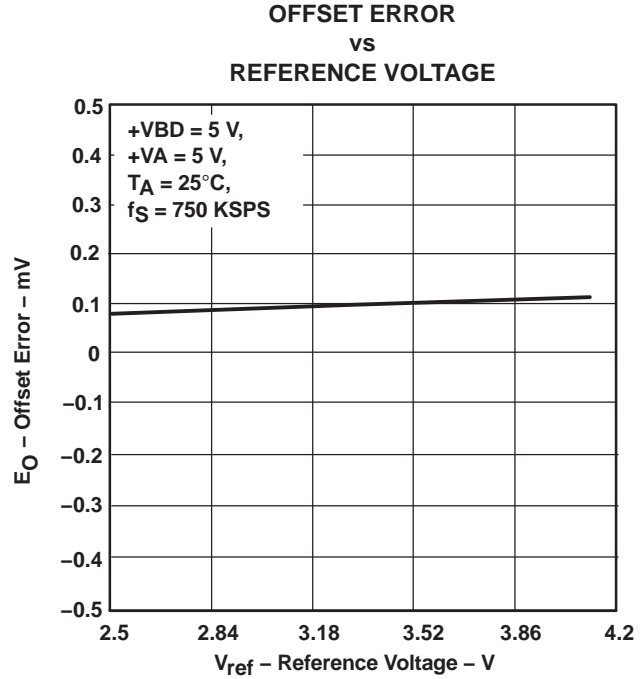
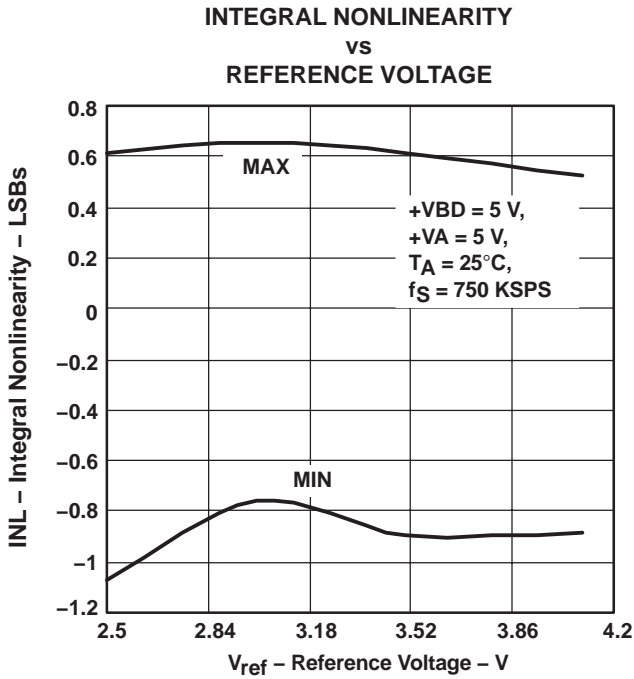
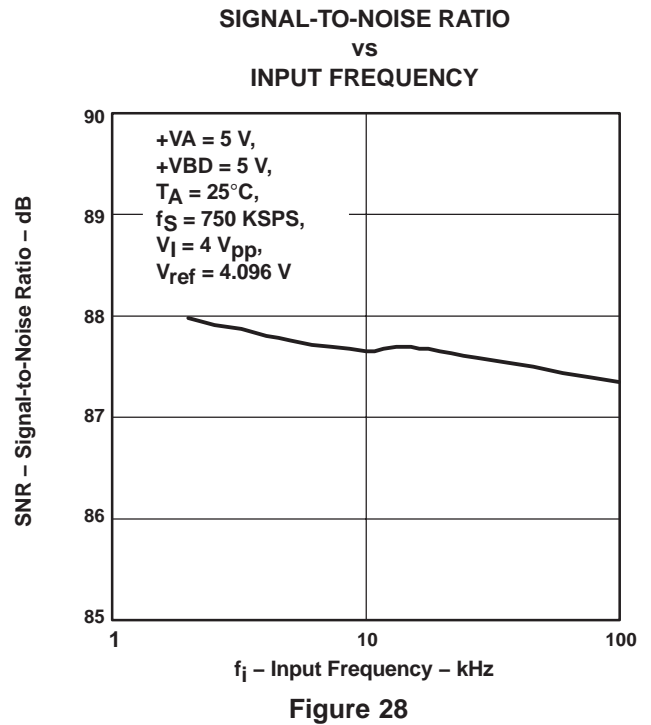
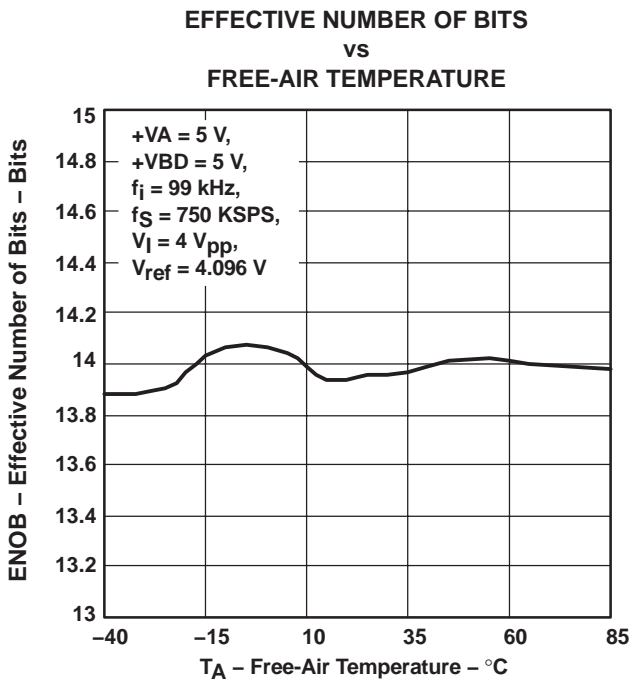
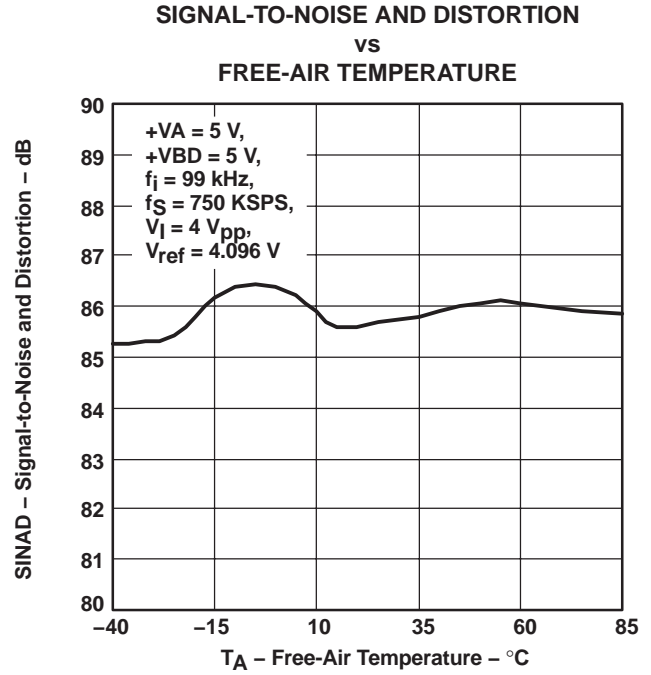
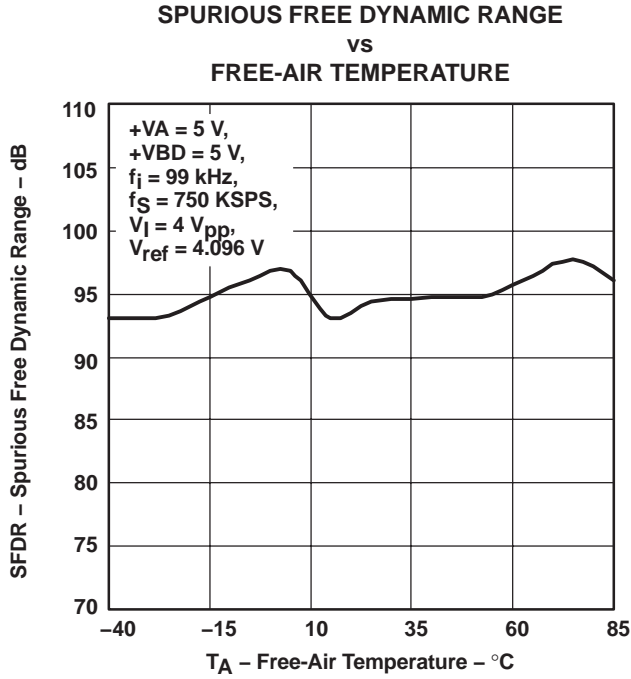


Figure 16







TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

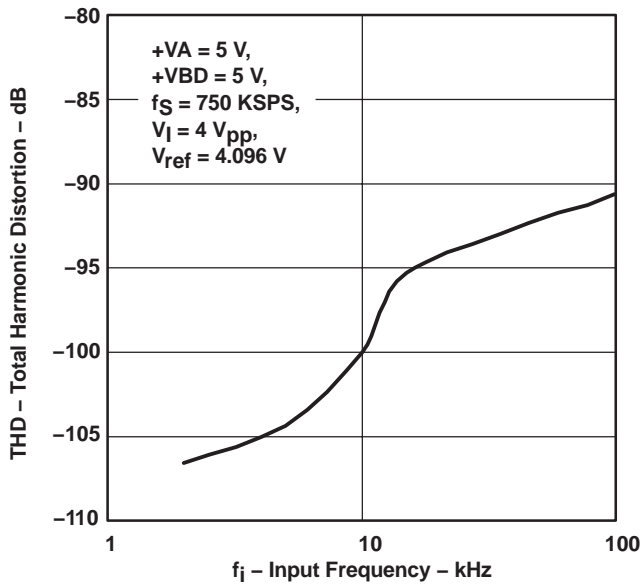


Figure 29

SIGNAL-TO-NOISE AND DISTORTION
vs
INPUT FREQUENCY

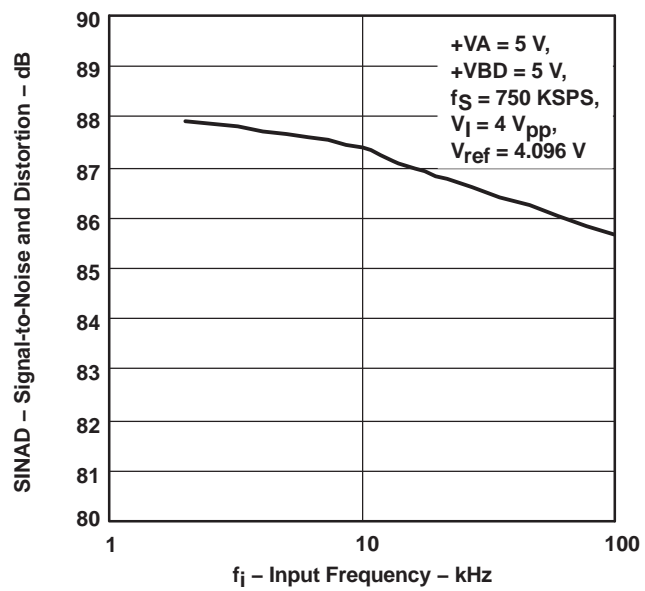


Figure 30

EFFECTIVE NUMBER OF BITS
vs
INPUT FREQUENCY

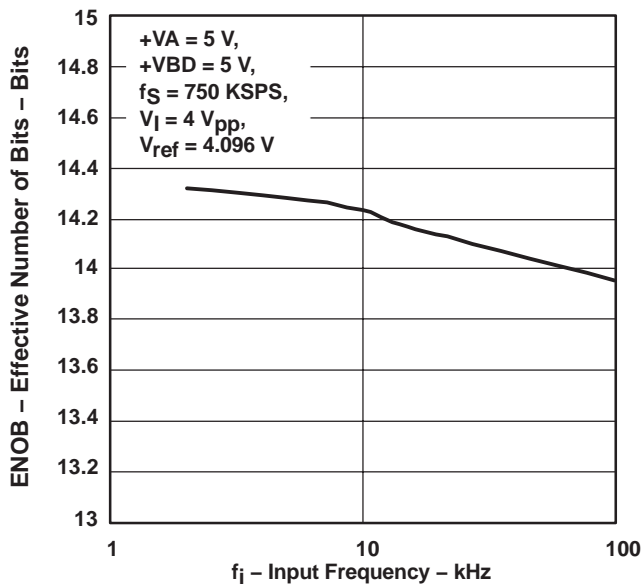


Figure 31

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY

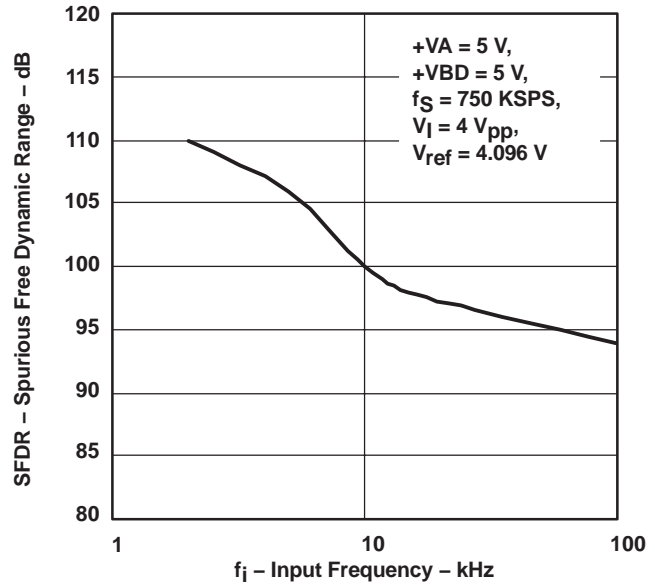
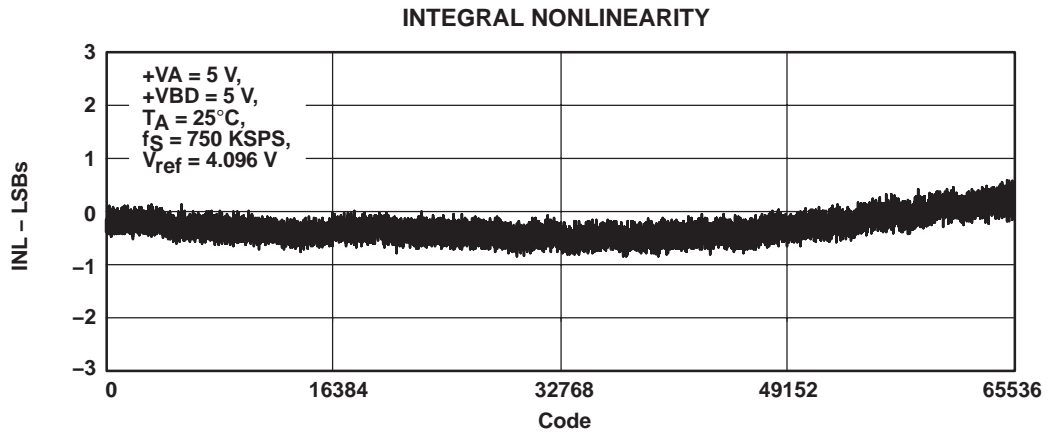
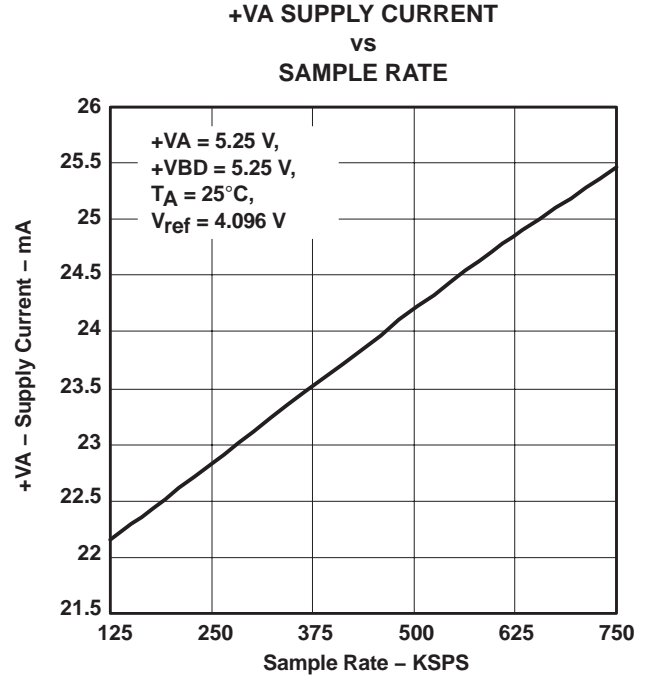
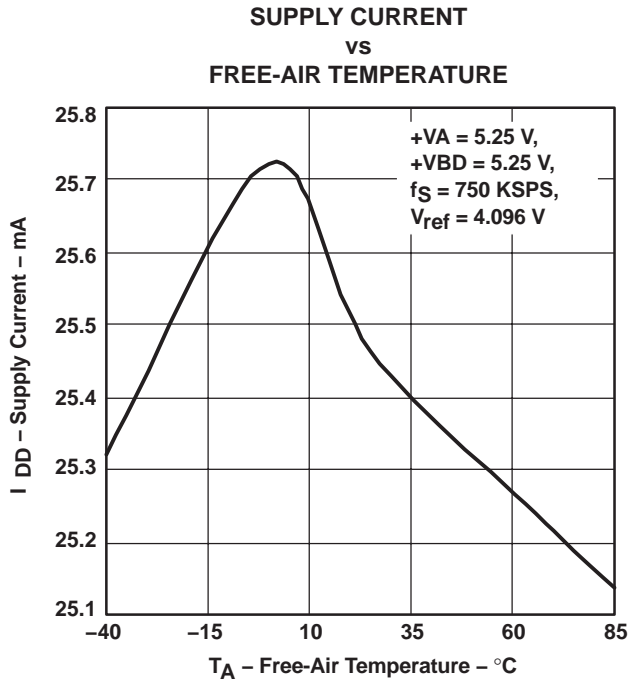


Figure 32



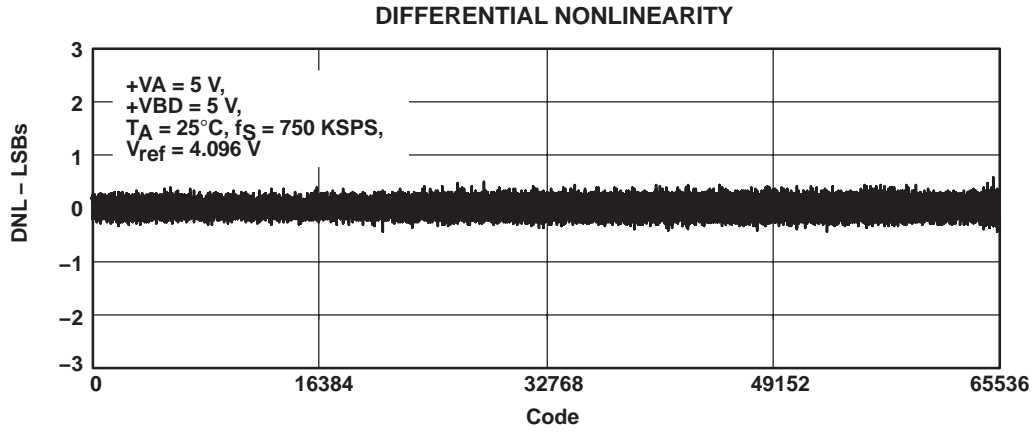


Figure 36

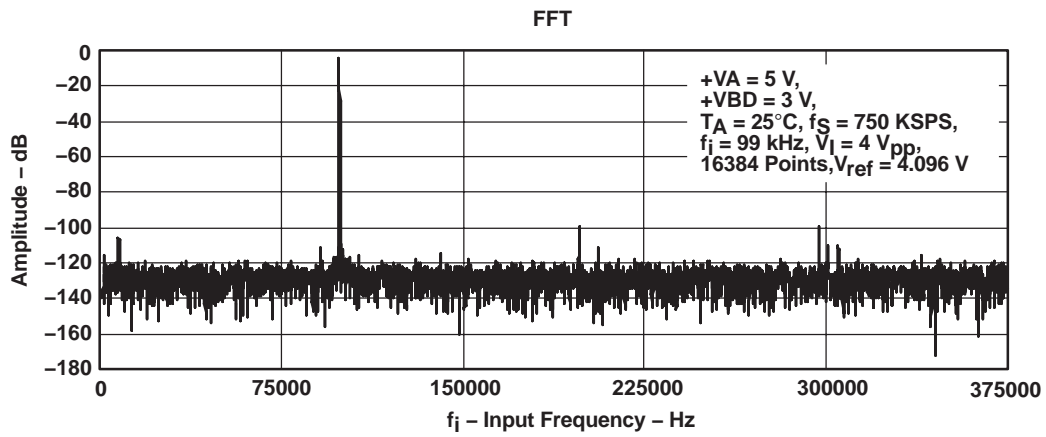


Figure 37

APPLICATION INFORMATION

MICROCONTROLLER INTERFACING

ADS8371 to 8-Bit Microcontroller Interface

Figure 38 shows a parallel interface between the ADS8371 and a typical microcontroller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microcontroller.

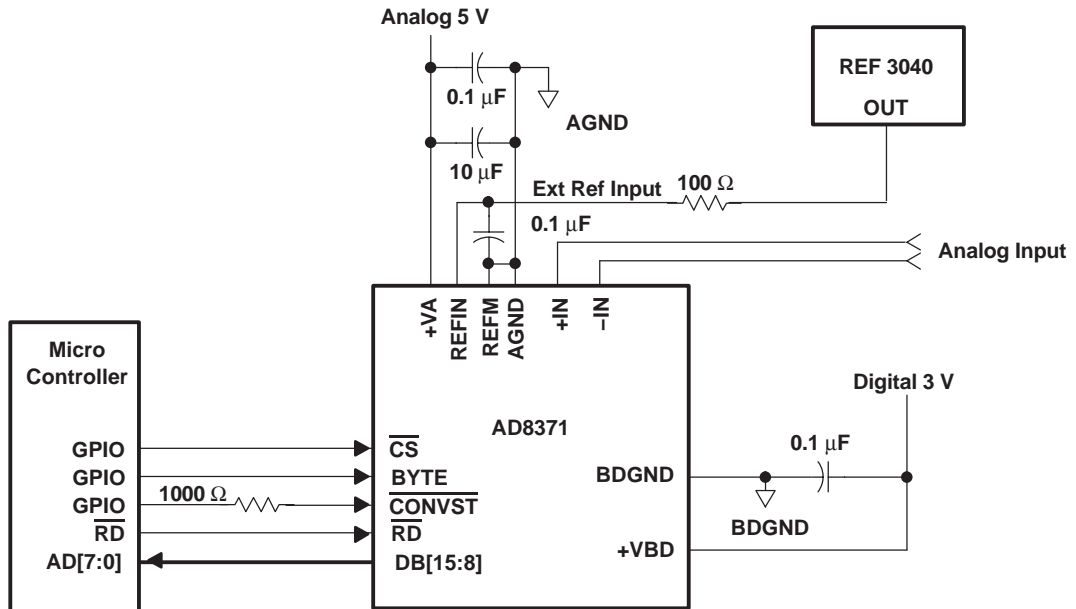


Figure 38. ADS8371 Application Circuitry

PRINCIPLES OF OPERATION

The ADS8371 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 38 for the application circuit for the ADS8371.

The conversion clock is generated internally. The conversion time of 1.13 μs is capable of sustaining a 750-kHz throughput.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8371 can operate with an external reference with a range from 2.5 V to 4.2 V. The reference voltage on the input pin 1 (REFIN) of the converter is internally buffered. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF3040 can be used to drive this pin. A 0.1- μF decoupling capacitor is required between pin 1 and pin 48 of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the terminals of the capacitor to the pins of the converter. An RC network can also be used to filter the reference voltage. A 100- Ω series resistor and a 0.1- μF capacitor, which can also serve as the decoupling capacitor, can be used to filter the reference voltage.

ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between -0.2 V and 0.2 V , allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of -0.2 V to $V_{\text{ref}} + 0.2\text{ V}$. The input span (+IN – (–IN)) is limited to 0 V to V_{ref} .

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8371 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to an 16-bit settling level within the acquisition time (200 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 G Ω .

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and –IN inputs and the span (+IN – (–IN)) should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

Care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in offset error, gain error, and linearity error which changes with temperature and input voltage.

The analog input to the converter needs to be driven with a low noise, high-speed op-amp like the THS4031. An RC filter is recommended at the input pins to low-pass filter the noise from the source. A series resistor of 15 Ω and a decoupling capacitor of 200 pF is recommended.

The input to the converter is a unipolar input voltage in the range 0 V to V_{ref} . The THS4031 can be used in the source follower configuration to drive the converter.

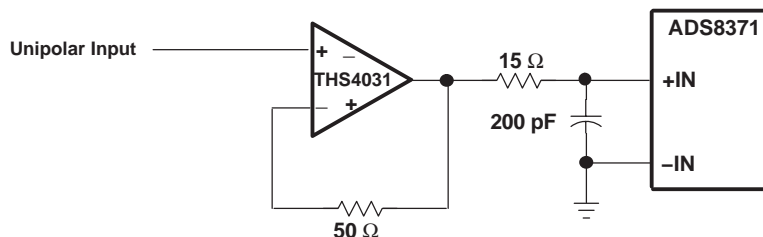


Figure 39. Unipolar Input to Converter

In systems where the input is bipolar, the THS4031 can be used in the inverting configuration with an additional DC bias applied to its + input so as to keep the input to the ADS8371 within its rated operating voltage range. This configuration is also recommended when the ADS8371 is used in signal processing applications where good SNR and THD performance is required. The DC bias can be derived from the REF3020 or the REF3040 reference voltage ICs. The input configuration shown below is capable of delivering better than 87-dB SNR and –90-dB THD at an input frequency of 100 kHz. In case bandpass filters are used to filter the input, care should be taken to ensure that the signal swing at the input of the bandpass filter is small so as to keep the distortion introduced by the filter minimal. In such cases, the gain of the circuit shown in Figure 40 can be increased to keep the input to the ADS8371 large to keep the SNR of the system high. Note that the gain of the system from the + input to the output of the THS4031 in such a configuration is a function of the gain of the AC signal. A resistor divider can be used to scale the output of the REF3020 or REF3040 to reduce the voltage at the DC input to THS4031 to keep the voltage at the input of the converter within its rated operating range.

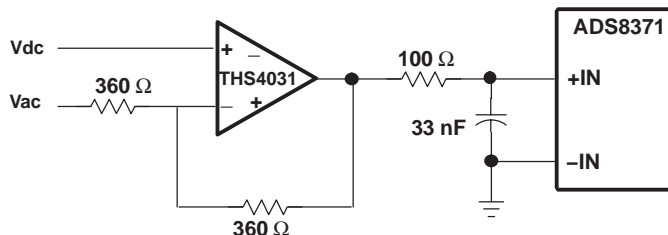


Figure 40. Bipolar Input to Converter

DIGITAL INTERFACE

Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8371 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 40 ns (after the 40 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high), while $\overline{\text{CS}}$ is low. The BUSY output is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high throughout the conversion process and returns low when the conversion has ended. Sampling starts with the falling edge of the BUSY signal when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the RD and CS pins are brought low in order to enable the parallel output bus with the conversion.

ADS8371

SLAS390B – JUNE 2003 – REVISED FEBRUARY 2005

Digital Inputs

The converter switches from sample to hold mode at the falling edge of the $\overline{\text{CONVST}}$ input pin. A clean and low jitter falling edge is important to the performance of the converter. A sharp falling transition on this pin can affect the voltage that is acquired by the converter. A falling transition time in the range of 10 ns to 30 ns is required to achieve the rated performance of the converter. A resistor of approximately 1000 Ω (10% tolerance) can be placed in series with the $\overline{\text{CONVST}}$ input pin to satisfy this requirement.

The other digital inputs to the ADS8371 do not require any resistors in series with them. However, certain precautions are necessary to ensure that transitions on these inputs do not affect converter performance. It is recommended that all activity on the input pins happen during the first 400 ns of the conversion period. This allows the error correction circuits inside the device to correct for any errors that these activities cause on the converter output. For example, when the converter is operated with $\overline{\text{CS}}$ and $\overline{\text{RD}}$ tied to ground, the signal $\overline{\text{CONVST}}$ can be brought low to initiate a conversion and brought high after a duration not exceeding 400 ns. Figure 41 shows the recommended timing for the $\overline{\text{CONVST}}$ input with $\overline{\text{RD}}$ and $\overline{\text{CS}}$ tied low.

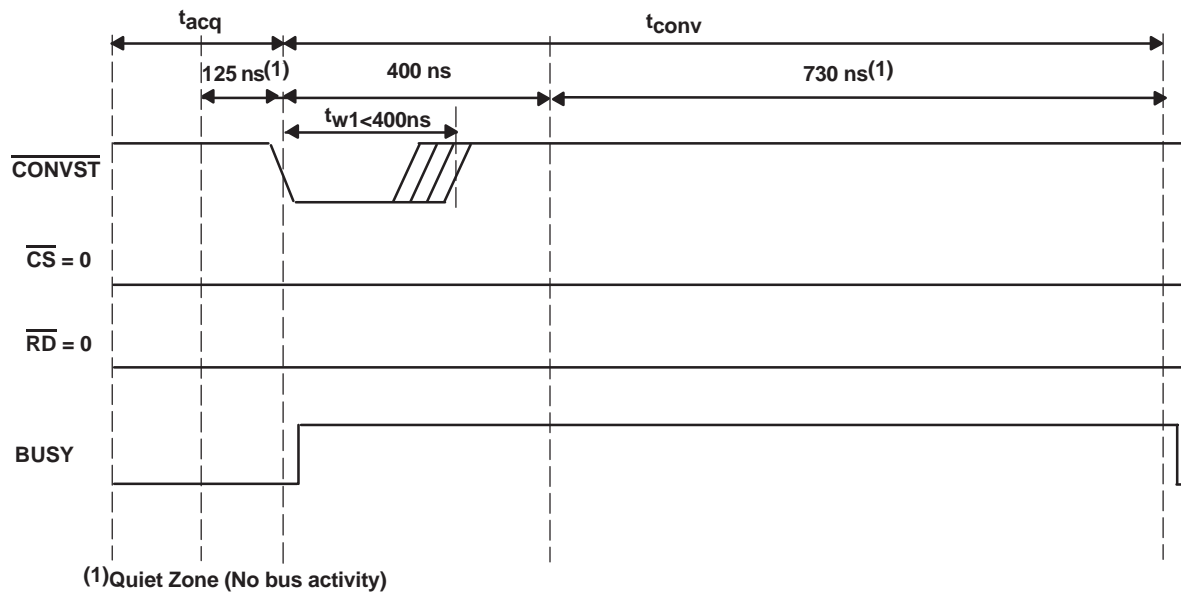


Figure 41. Timing for $\overline{\text{CONVST}}$ When $\overline{\text{CS}} = \overline{\text{RD}} = \text{BDGND}$

A similar precaution applies when \overline{RD} is used to three-state the output buffers after a data-read operation. A minimum quiet period of 125 ns is also required from the instant the data is changed on the bus (such as the falling or rising edge of \overline{RD} , the falling or rising edge of \overline{BYTE} , and the falling or rising edge of \overline{CONVST}). Figure 42 shows the timing of the input control signals that allow these conditions to be satisfied.

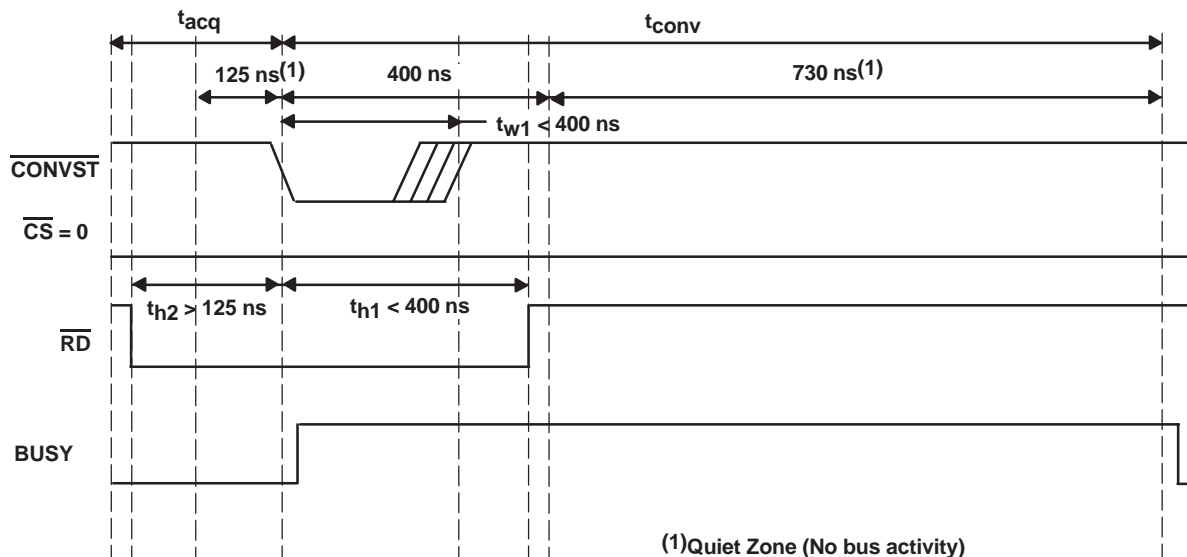


Figure 42. Bus Activity Split to Avoid Quiet Zone

If the \overline{RD} pin is brought high to three-state the data buses, the three-stating operation should occur 125 ns before the end of the acquisition phase. Figure 43 shows the recommended timing for using the ADS8381 in this mode of operation. The same principle applies to other bus activities such as \overline{BYTE} .

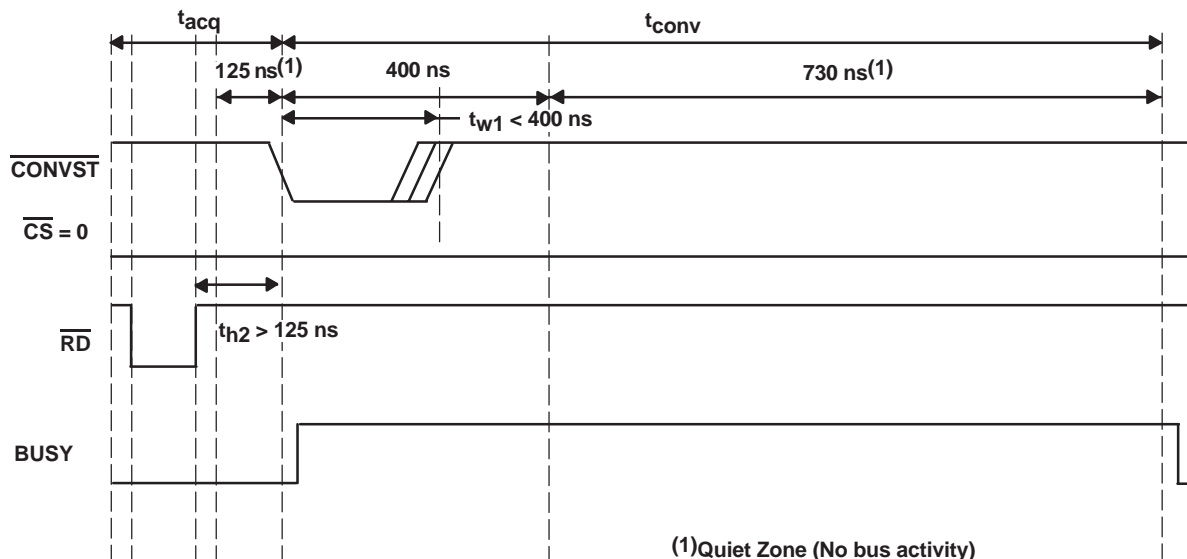


Figure 43. Read Timing if the Bus Needs to be Three-Stated

Reading Data

The ADS8371 outputs full parallel data in straight binary format as shown in Table 1. The parallel output is active when \overline{CS} and \overline{RD} are both low. Any other combination of \overline{CS} and \overline{RD} sets the parallel output to 3-state. BYTE is used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. Refer to Table 1 for ideal output codes.

Table 1. Ideal Input Voltages and Output Codes

| DESCRIPTION | ANALOG VALUE | DIGITAL OUTPUT STRAIGHT BINARY | |
|-----------------------------|--------------------------------|-----------------------------------|----------|
| | | BINARY CODE | HEX CODE |
| Full scale range | $(+V_{ref})$ | | |
| Least significant bit (LSB) | $(+V_{ref})/65536$ | | |
| +Full scale | $(+V_{ref}) - 1 \text{ LSB}$ | 1111 1111 1111 1111 | FFFF |
| Midscale | $(+V_{ref})/2$ | 1000 0000 0000 0000 | 8000 |
| Midscale – 1 LSB | $(+V_{ref})/2 - 1 \text{ LSB}$ | 0111 1111 1111 1111 | 7FFF |
| Zero | 0 V | 0000 0000 0000 0000 | 0000 |

The output data is a full 16-bit word (D15–D0) on DB15–DB0 pins (MSB–LSB) if BYTE is low.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB15–DB8. In this case two reads are necessary: the first as before, leaving BYTE low and reading the 8 most significant bits on pins DB15–DB8, then bringing BYTE high. When BYTE is high, the low bits (D7–D0) appear on pins DB15–D8.

These multiword read operations can be done with multiple active \overline{RD} (toggling) or with \overline{RD} tied low for simplicity.

Table 2. Conversion Data Readout

| BYTE | DATA READ OUT | |
|------|---------------|--------------|
| | DB15–DB8 PINS | DB7–DB0 PINS |
| High | D7–D0 | All one's |
| Low | D15–D8 | D7–D0 |

RESET

The device can be reset through the use of the combination of \overline{CS} and \overline{CONVST} . Since the BUSY signal is held at high during the conversion, either one of these conditions triggers an internal self-clear reset to the converter.

- Issue a \overline{CONVST} when \overline{CS} is low and internal CONVERT state is high. The falling edge of \overline{CONVST} starts a reset.
- Issue a \overline{CS} (select the device) while internal CONVERT state is high. The falling edge of \overline{CS} causes a reset.

Once the device is reset, all output latches are cleared (set to zeroes) and the BUSY signal is brought low. A new sampling period is started at the falling edge of the BUSY signal immediately after the instant of the internal reset.

INITIALIZATION

At first power on there are three read cycles required (\overline{RD} must be toggled three times). If conversion cycle is attempted before these initialization read cycles, the first three conversion cycles will not produce valid results. This is used to load factory trimming data for a specific device to assure high accuracy of the converter. Because of this requirement, the \overline{RD} pin cannot be tied permanently to BDGND. System designers can still achieve the AUTO READ function if the power-on requirement is satisfied.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8371 circuitry.

As the ADS8371 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8371 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1- μ F bypass capacitor is recommended from pin 1 (REFIN) directly to pin 48 (REFM). REFM and AGND should be shorted on the same ground plane under the device.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8371 should be clean and well bypassed. A 0.1- μ F ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of the capacitor. In addition, a 1- μ F to 10- μ F capacitor is recommended. In some situations, additional bypassing may be required, such as a 100- μ F electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

Table 3. Power Supply Decoupling Capacitor Placement

| POWER SUPPLY PLANE SUPPLY PINS | CONVERTER ANALOG SIDE | CONVERTER DIGITAL SIDE |
|---|---|------------------------|
| Pin pairs that require shortest path to decoupling capacitors | (4,5), (8,9), (10,11), (13,15), (43,44), (45,46) | (24,25) |
| Pins that require no decoupling | 12, 14 | 37, 38 |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|--------------------------------------|
| ADS8371IBPFBR | ACTIVE | TQFP | PFB | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |
| ADS8371IBPFBRG4 | ACTIVE | TQFP | PFB | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |
| ADS8371IBPFBT | ACTIVE | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |
| ADS8371IBPFBTG4 | ACTIVE | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |
| ADS8371IPFBT | ACTIVE | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |
| ADS8371IPFBTG4 | ACTIVE | TQFP | PFB | 48 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Request Free Samples |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS8371IBPFBR | TQFP | PFB | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS8371IBPFBT | TQFP | PFB | 48 | 250 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS8371IPFBT | TQFP | PFB | 48 | 250 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS8371IBPFBR | TQFP | PFB | 48 | 1000 | 367.0 | 367.0 | 38.0 |
| ADS8371IBPFBT | TQFP | PFB | 48 | 250 | 367.0 | 367.0 | 38.0 |
| ADS8371IPFBT | TQFP | PFB | 48 | 250 | 367.0 | 367.0 | 38.0 |

PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PFB (S-PQFP-G48)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

| | |
|------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Mobile Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |

TI E2E Community e2e.ti.com