



# 16-Bit 10 $\mu$ s Serial CMOS Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

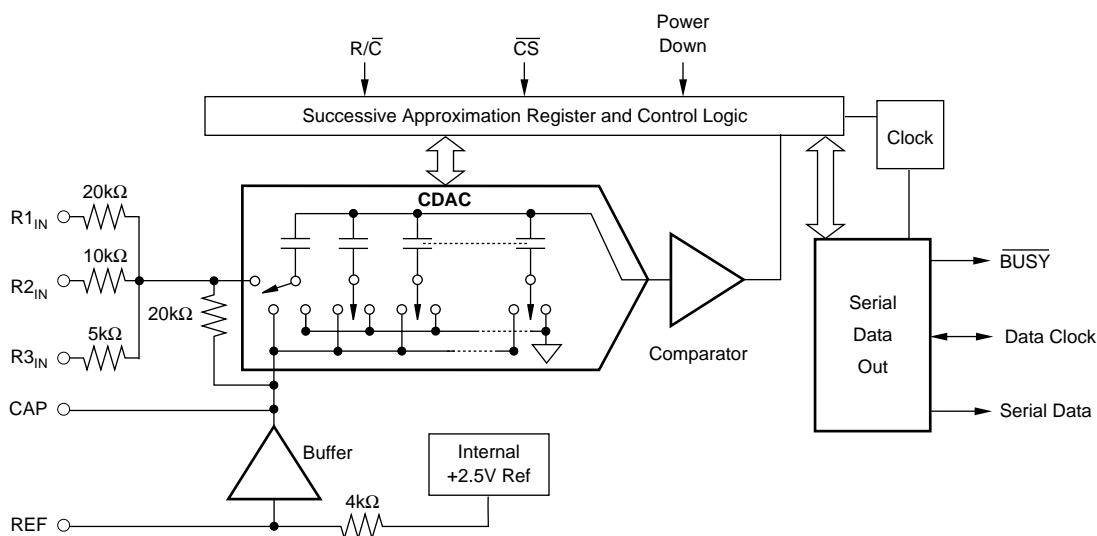
- 100kHz SAMPLING RATE
- 86dB SINAD WITH 20kHz INPUT
- $\pm 2$ LSB INL
- DNL: 16 Bits No Missing Codes
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7808
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 0.3" SO-20
- SIMPLE DSP INTERFACE

## DESCRIPTION

The ADS7809 is a complete 16-bit sampling Analog-to-Digital (A/D) converter using state-of-the-art CMOS structures. It contains a 16-bit capacitor-based Successive Approximation Register (SAR) A/D converter with sample-and-hold, reference, clock, and a serial data interface. Data can be outputted using the internal clock, or can be synchronized to an external data clock. The ADS7809 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7809 is specified at a 100kHz sampling rate, and specified over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including  $\pm 10$ V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The ADS7809 is available in a 0.3" SO-20, and is fully specified for operation over the industrial  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  range.



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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Analog Inputs: R1 <sub>IN</sub> .....	±25V
R2 <sub>IN</sub> .....	±25V
R3 <sub>IN</sub> .....	±25V
REF .....	V <sub>ANA</sub> + 0.3V to AGND2 – 0.3V
CAP .....	Indefinite Short to AGND2, Momentary Short to V <sub>ANA</sub>
Ground Voltage Differences: DGND, AGND2 .....	±0.3V
V <sub>ANA</sub> .....	7V
V <sub>DIG</sub> to V <sub>ANA</sub> .....	+0.3
V <sub>DIG</sub> .....	7V
Digital Inputs .....	–0.3V to V <sub>DIG</sub> + 0.3V
Maximum Junction Temperature .....	+165°C
Internal Power Dissipation .....	700mW
Lead Temperature (soldering, 10s) .....	+300°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7809U	±3	15	83	SO-20	DW	–40°C to +85°C	ADS7809U	ADS7809U	Rail, 38
"	"	"	"	"	"	"	"	ADS7809U/1K	Tape and Reel, 1000
ADS7809UB	±2	16	86	"	"	"	ADS7809UB	ADS7809UB	Rail, 38
"	"	"	"	"	"	"	"	ADS7809UB/1K	Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

# ELECTRICAL CHARACTERISTICS

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $f_S = 100\text{kHz}$ ,  $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$ , using internal reference and fixed resistors (see Figure 4), unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809U			ADS7809UB			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
<b>RESOLUTION</b>				16			*	Bits	
<b>ANALOG INPUT</b> Voltage Ranges Impedance Capacitance				±10, 0V to 5V, etc. (See Table I) See Table I			*	pF	
<b>THROUGHPUT SPEED</b> Complete Cycle Throughput Rate	Acquire and Convert	100		10	*		*	μs kHz	
<b>DC ACCURACY</b> Integral Linearity Error Differential Linearity Error No Missing Codes Transition Noise <sup>(2)</sup> Full-Scale Error <sup>(3,4)</sup> Full-Scale Error Drift Full-Scale Error <sup>(3,4)</sup> Full-Scale Error Drift Bipolar Zero Error <sup>(3)</sup> Bipolar Zero Error Drift Unipolar Zero Error <sup>(3)</sup> Unipolar Zero Error <sup>(3)</sup> Unipolar Zero Error Drift Recovery to Rated Accuracy after Power-Down Power-Supply Sensitivity ( $V_{\text{DIG}} = V_{\text{ANA}} = V_{\text{D}}$ )	Ext. 2.5000V Ref Ext. 2.5000V Ref Bipolar Ranges Bipolar Ranges 0V to 10V Ranges 0V to 4V, 0V to 5V Ranges Unipolar Ranges 1μF Capacitor to CAP  +4.75V < $V_{\text{D}}$ < +5.25V	15	1.3	±3 +3, -2  ±0.5  ±0.5  ±10  ±5 ±3  ±8	16	*	±2 ±1  *	LSB <sup>(1)</sup> LSB Bits LSB % ppm/°C % ppm/°C mV ppm/°C mV mV ppm/°C ms LSB	
<b>AC ACCURACY</b> Spurious-Free Dynamic Range Total Harmonic Distortion Signal-to-(Noise + Distortion)  Signal-to-Noise Full-Power Bandwidth <sup>(6)</sup>	$f_{\text{IN}} = 20\text{kHz}$ $f_{\text{IN}} = 20\text{kHz}$ $f_{\text{IN}} = 20\text{kHz}$ -60dB Input $f_{\text{IN}} = 20\text{kHz}$	90	100	-100	96	*	*	-94	dB <sup>(5)</sup> dB dB dB dB kHz
<b>SAMPLING DYNAMICS</b> Aperture Delay Transient Response Overvoltage Recovery <sup>(7)</sup>	FS Step		40	2		*	*		ns μs ns
<b>REFERENCE</b> Internal Reference Voltage Internal Reference Source Current (Must use external buffer) External Reference Voltage Range For Specified Linearity External Reference Current Drain	No Load   Ext. 2.5000V Ref	2.48	2.5	2.52	*	*	*	*	V μA V μA
<b>DIGITAL INPUTS</b> Logic Levels $V_{\text{IL}}$ $V_{\text{IH}}^{(8)}$ $I_{\text{IL}}$ $I_{\text{IH}}$	$V_{\text{IL}} = 0\text{V}$ $V_{\text{IH}} = 5\text{V}$	-0.3	2.0	+0.8 $V_{\text{D}} + 0.3\text{V}$ ±10 ±10	*	*	*	*	V V μA μA

# ELECTRICAL CHARACTERISTICS (Cont.)

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $f_S = 100\text{kHz}$ ,  $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$ , using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809U			ADS7809UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>DIGITAL OUTPUTS</b> Data Format Data Co Pipeline Delay Data Clock								
Internal (Output Only When Transmitting Data)	EXT/ $\overline{\text{INT}}$ LOW		2.3			*		MHz
External (Can Run Continually)	EXT/ $\overline{\text{INT}}$ HIGH	0.1		10	*		*	MHz
$V_{\text{OL}}$	$I_{\text{SINK}} = 1.6\text{mA}$			+0.4			*	V
$V_{\text{OH}}$	$I_{\text{SOURCE}} = 500\mu\text{A}$	+4			*		*	V
Leakage Current	High-Z State, $V_{\text{OUT}} = 0\text{V}$ to $V_{\text{DIG}}$			$\pm 5$			*	$\mu\text{A}$
Output Capacitance	High-Z State			15			*	pF
<b>POWER SUPPLIES</b> Specified Performance	Must be $\leq V_{\text{ANA}}$	+4.75	+5	+5.25	*	*	*	V
$V_{\text{DIG}}$		+4.75	+5	+5.25	*	*	*	V
$V_{\text{ANA}}$			0.3			*		mA
$I_{\text{DIG}}$			16			*		mA
$I_{\text{ANA}}$				100		*	*	mW
Power Dissipation: PWRD LOW PWRD HIGH	$V_{\text{ANA}} = V_{\text{DIG}} = 5\text{V}$ , $f_S = 100\text{kHz}$		50			*	*	$\mu\text{W}$
<b>TEMPERATURE RANGE</b> Specified Performance		-40		+85	*		*	$^\circ\text{C}$
Derated Performance		-55		+125	*		*	$^\circ\text{C}$
Storage		-65		+150	*		*	$^\circ\text{C}$
Thermal Resistance ( $\theta_{\text{JA}}$ ) SO			75			*		$^\circ\text{C/W}$

\* Same as specification for ADS7809U.

NOTES: (1) LSB means Least Significant Bit. For the  $\pm 10\text{V}$  input range, one LSB is  $305\mu\text{V}$ .

(2) Typical rms noise at worst case transitions and temperatures.

(3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer.

(4) For bipolar input ranges, full-scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full-scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.

(5) All specifications in dB are referred to a full-scale  $\pm 10\text{V}$  input.

(6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB.

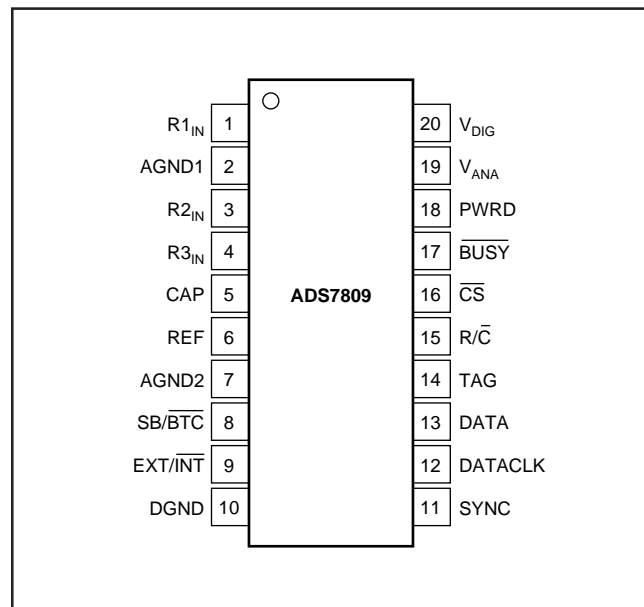
(7) Recovers to specified performance after  $2 \cdot \text{FS}$  input overvoltage.

(8) The minimum  $V_{\text{IH}}$  level for the DATACLK signal is 3V.

## PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	R1 <sub>IN</sub>	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	R2 <sub>IN</sub>	Analog Input. See Table I and Figure 4 for input range connections.
4	R3 <sub>IN</sub>	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2μF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2μF Tantalum capacitor.
7	AGND2	Analog Ground
8	SB/BTC	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.
9	EXT/INT	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground
11	SYNC	Synch Output. If EXT/INT is HIGH, either a rising edge on R/C with CS LOW or a falling edge on CS with R/C HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/INT level. Output data will be synchronized to this clock. If EXT/INT is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/BTC. In the external clock mode, after 16 bits of data, the ADS7809 will output the level input on TAG as long as CS is LOW and R/C is HIGH (see Figure 3). If EXT/INT is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/INT is HIGH, digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as CS is LOW and R/C is HIGH. See Figure 3.
15	R/C	Read/Convert Input. With CS LOW, a falling edge on R/C puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/INT is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/INT is HIGH, a rising edge on R/C with CS LOW, or a falling edge on CS with R/C HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	CS	Chip Select. Internally OR'ed with R/C.
17	BUSY	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. CS or R/C must be HIGH when BUSY rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V <sub>ANA</sub>	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1μF ceramic and 10μF tantalum capacitors.
20	V <sub>DIG</sub>	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V <sub>ANA</sub> .

## PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT R1 <sub>IN</sub> VIA 200Ω TO	CONNECT R2 <sub>IN</sub> VIA 100Ω TO	CONNECT R3 <sub>IN</sub> TO	IMPEDANCE
±10V	V <sub>IN</sub>	AGND	CAP	22.9kΩ
±5V	AGND	V <sub>IN</sub>	CAP	13.3kΩ
±3.33V	V <sub>IN</sub>	V <sub>IN</sub>	CAP	10.7kΩ
0V to 10V	AGND	V <sub>IN</sub>	AGND	13.3kΩ
0V to 5V	AGND	AGND	V <sub>IN</sub>	10.0kΩ
0V to 4V	V <sub>IN</sub>	AGND	V <sub>IN</sub>	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

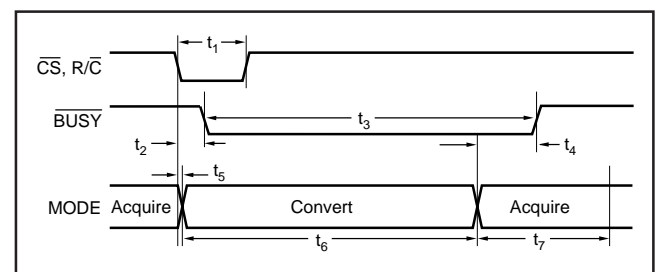


FIGURE 1. Basic Conversion Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_1$	Convert Pulse Width	40		6000	ns
$t_2$	$\overline{\text{BUSY}}$ Delay			65	ns
$t_3$	$\overline{\text{BUSY}}$ LOW			8	$\mu\text{s}$
$t_4$	$\overline{\text{BUSY}}$ Delay After End of Conversion		220		ns
$t_5$	Aperture Delay		40		ns
$t_6$	Conversion Time		7.6	8	$\mu\text{s}$
$t_7$	Acquisition Time			2	$\mu\text{s}$
$t_6 + t_7$	Throughput Time		9	10	$\mu\text{s}$
$t_8$	$\text{R}/\overline{\text{C}}$ LOW to DATACLK Delay		450		ns
$t_9$	DATACLK Period		440		ns
$t_{10}$	Data Valid to DATACLK HIGH Delay	20	75		ns
$t_{11}$	Data Valid After DATACLK LOW Delay	100	125		ns
$t_{12}$	External DATACLK	100			ns
$t_{13}$	External DATACLK HIGH	20			ns
$t_{14}$	External DATACLK LOW	30			ns
$t_{15}$	DATACLK HIGH Setup Time	20		$t_{12} + 5$	ns
$t_{16}$	$\text{R}/\overline{\text{C}}$ to $\overline{\text{CS}}$ Setup Time	10			ns
$t_{17}$	SYNC Delay After DATACLK HIGH	15		35	ns
$t_{18}$	Data Valid Delay	25		55	ns
$t_{19}$	$\overline{\text{CS}}$ to Rising Edge Delay	25			ns
$t_{20}$	Data Available after $\overline{\text{CS}}$ LOW	6			$\mu\text{s}$

TABLE II. Conversion and Data Timing.  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

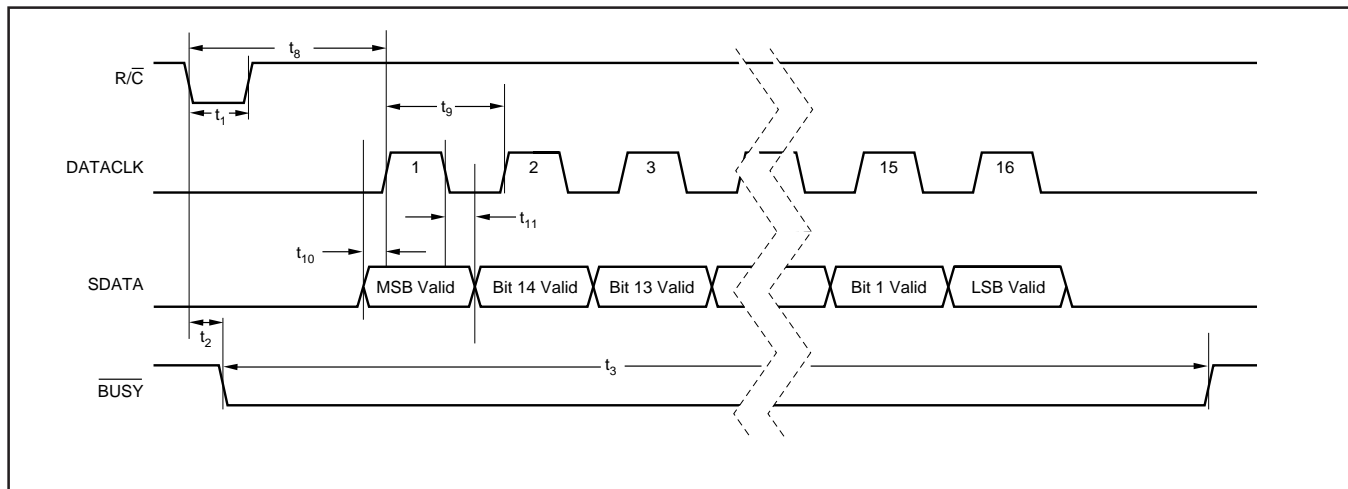


FIGURE 2. Serial Data Timing Using Internal Clock. ( $\overline{\text{CS}}$ ,  $\text{EXT}/\overline{\text{INT}}$  and TAG Tied LOW.)

SPECIFIC FUNCTION	$\overline{CS}$	$R/\overline{C}$	$\overline{BUSY}$	$\overline{EXT}/\overline{INT}$	DATACLK	PWRD	SB/ $\overline{BTC}$	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1 > 0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n - 1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
	0	1 > 0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n - 1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1 > 0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1 > 0	1	1	Input	0	x	Initiates conversion "n".
	1 > 0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1 > 0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n - 1" clocked out synchronized to external DATACLK. <sup>(1)</sup> Conversion "n" in process.
Incorrect Conversions	0	0	0 > 1	x	x	0	x	$\overline{CS}$ or $R/\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition.
	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
Power-Down	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
	x	x	x	x	x	x	1	
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

TABLE III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/ $\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/ $\overline{BTC}$ HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	$\pm 10$	$\pm 5$	$\pm 3.33V$	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305 $\mu V$	153 $\mu V$	102 $\mu V$	153 $\mu V$	76 $\mu V$	61 $\mu V$				
+Full Scale (FS - 1LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	-305 $\mu V$	-153 $\mu V$	-102 $\mu V$	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
-Full Scale	-10V	-5V	-3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

TABLE IV. Output Codes and Ideal Input Voltages.

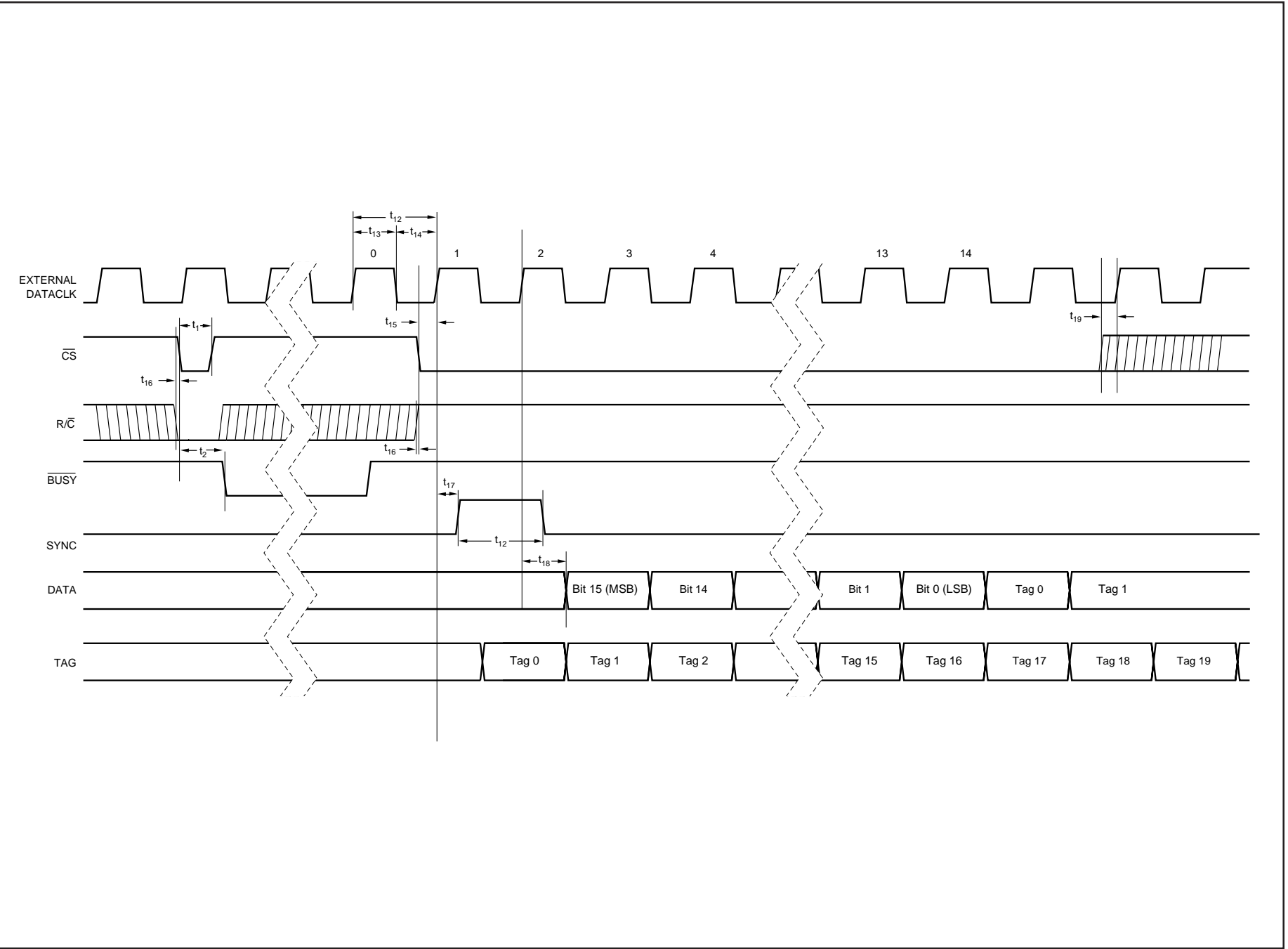


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/INT Tied High.) Read After Conversion.



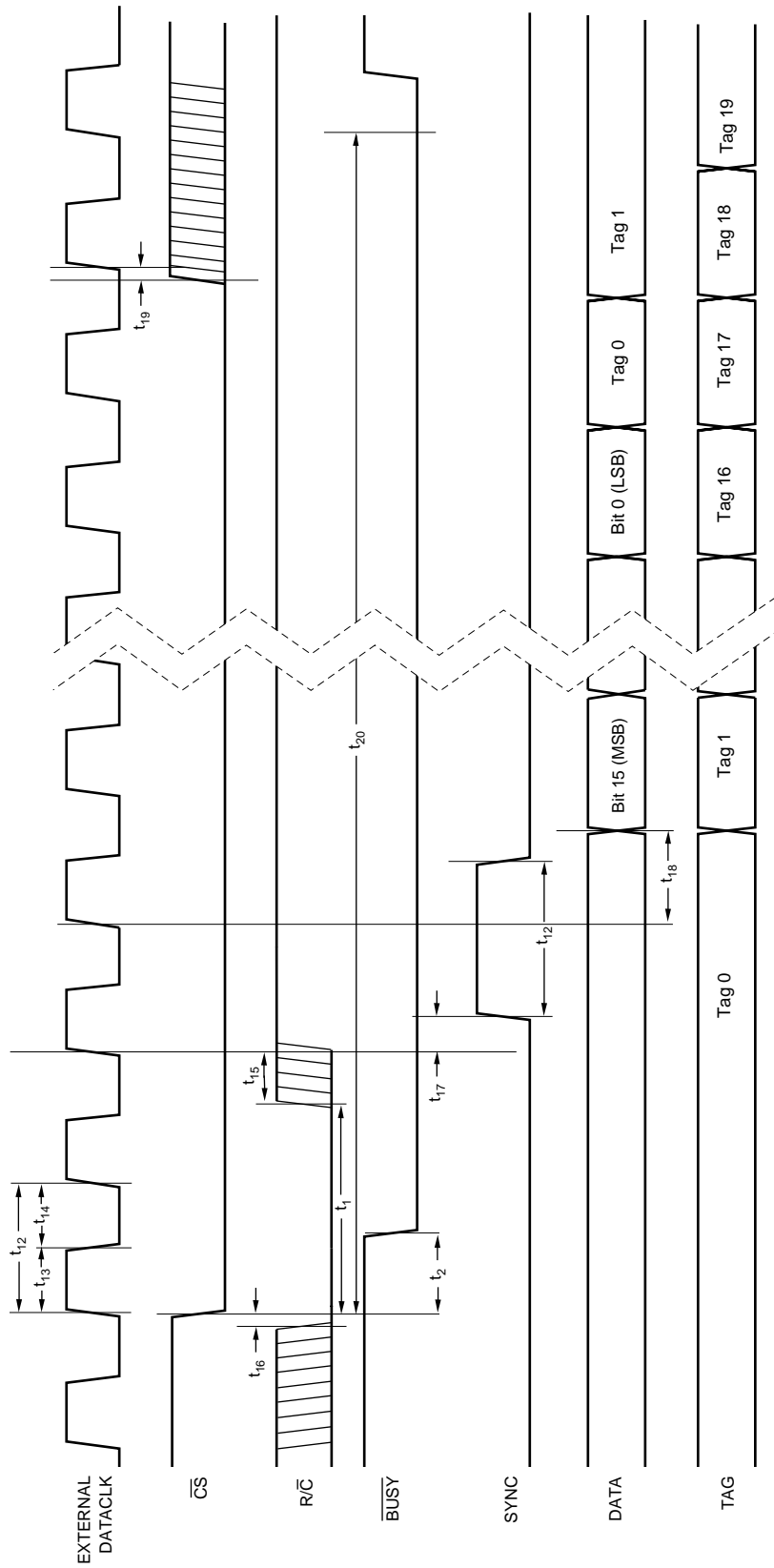


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/INT Tied High.) Read During Conversion (Previous Conversion Results).

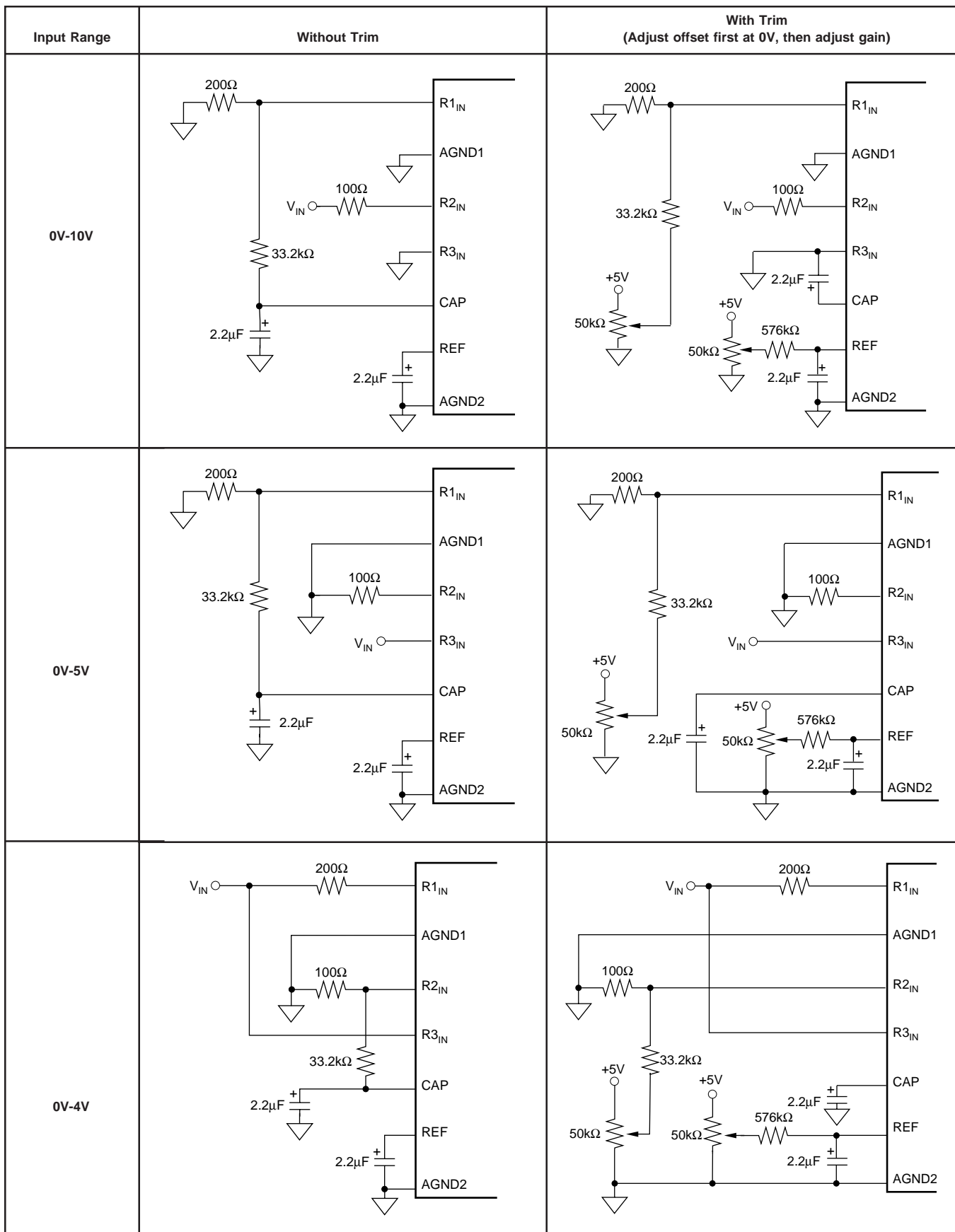


FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

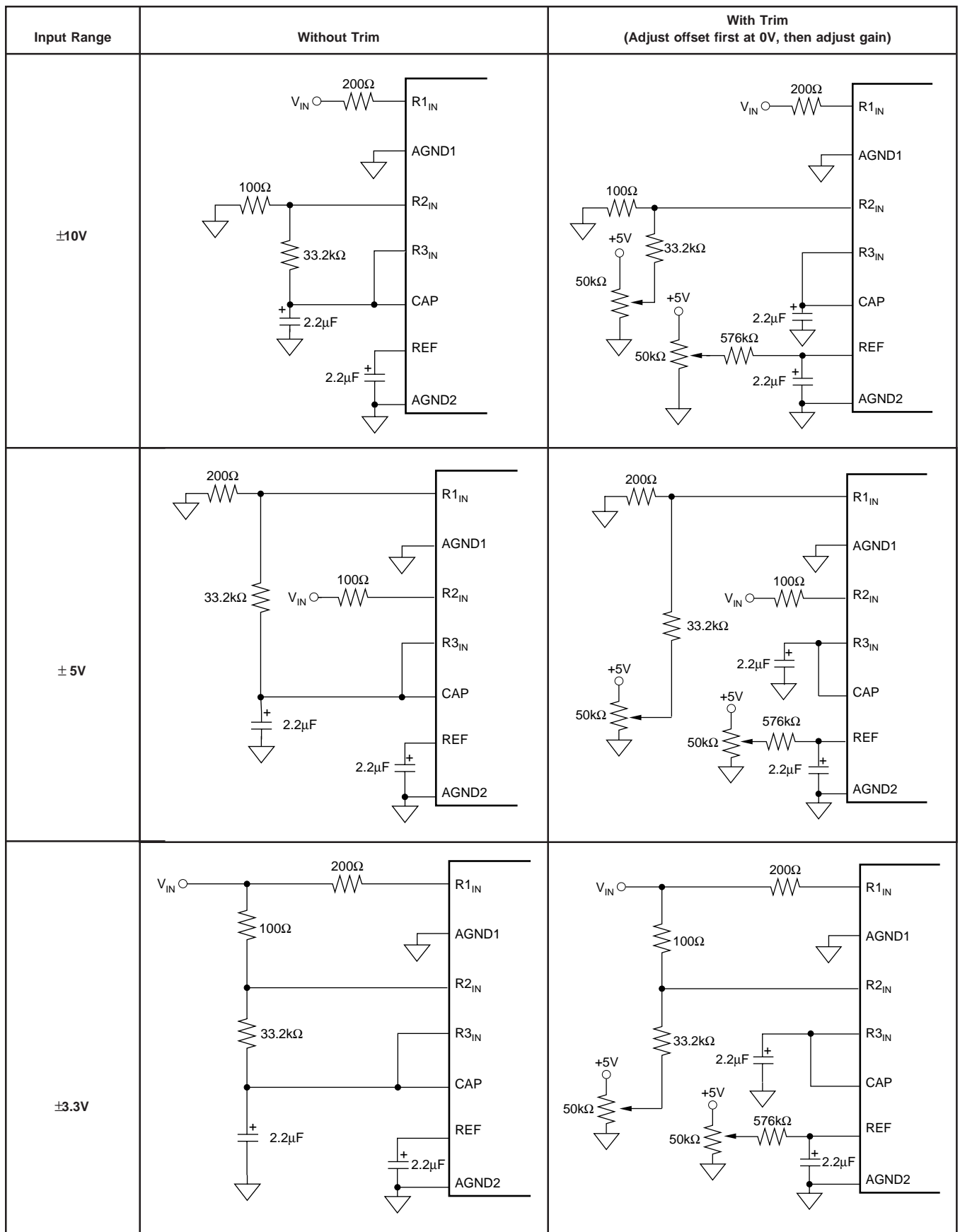


FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

## Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
10/06	C	3	Absolute Maximum Ratings	CAP and REF were switched.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS7809P	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI			
ADS7809PB	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI			
ADS7809U	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U	
ADS7809U/1K	NRND	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U	
ADS7809U/1KE4	NRND	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U	
ADS7809UB	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U B	
ADS7809UB/1K	NRND	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U B	
ADS7809UB/1KE4	NRND	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U B	
ADS7809UBE4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U B	
ADS7809UBG4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U B	
ADS7809UE4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U	
ADS7809UG4	NRND	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7809U	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7809U/1K	SOIC	DW	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
ADS7809UB/1K	SOIC	DW	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7809U/1K	SOIC	DW	20	1000	367.0	367.0	45.0
ADS7809UB/1K	SOIC	DW	20	1000	367.0	367.0	45.0



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



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- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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