| 0ARAMI | " 6ERS n # # TO # | 9 6ER n # # TO # | 5N | 4EST #ONDITIONS |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | $V_{SS}$ to $V_{DD}$ | V | $V_{DD}$ = +4.5 V, $V_{SS}$ = –4.5 V |
| On Resistance ($R_{ON}$) | 45 | | Ω typ | $V_S$ = ±4.5 V, $I_S$ = 1 mA; |
| | 75 90 | 100 | Ω max | Test Circuit 1 |
| On Resistance Match between | 1.3 | | Ω typ | |
| Channels ($\Delta R_{ON}$) | 3 3.2 | 3.5 | Ω max | $V_S$ = 3.5 V, $I_S$ = 1 mA |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 10 | | Ω typ | $V_{DD}$ = +5 V, $V_{SS}$ = –5 V; |
| | 16 17 | 18 | Ω max | $V_S$ = ±3 V, $I_S$ = 1 mA |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = +5.5 V, $V_{SS}$ = –5.5 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.005 | | nA typ | $V_D$ = ±4.5 V, $V_S$ = ∓4.5 V; |
| | ±0.2 | ±5 | nA max | Test Circuit 2 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.005 | | nA typ | $V_D$ = ±4.5 V, $V_S$ = ∓4.5 V; |
| ADG658 | ±0.2 | ±5 | nA max | Test Circuit 3 |
| ADG659 | ±0.1 | ±2.5 | nA max | |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.005 | | nA typ | $V_D$ = $V_S$ = ±4.5 V; Test Circuit 4 |
| ADG658 | ±0.2 | ±5 | nA max | |
| ADG659 | ±0.1 | ±2.5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | µA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±1 | µA max | |
| $C_{IN}$, Digital Input Capacitance | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{TRANS}$ | 80 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 115 140 | 165 | ns max | $V_S$ = 3 V; Test Circuit 5 |
| $t_{ON}$ ($\overline{EN}$) | 80 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 115 140 | 165 | ns max | $V_S$ = 3 V; Test Circuit 7 |
| $t_{OFF}$ ($\overline{EN}$) | 30 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 45 50 | 55 | ns max | $V_S$ = 3 V; Test Circuit 7 |
| Break-Before-Make Time Delay, $t_{BBM}$ | 50 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 10 | ns min | $V_{S1}$ = $V_{S2}$ = 3 V; Test Circuit 6 |
| Charge Injection | 2 | | pC typ | $V_S$ = 0 V, $R_S$ = 0 Ω, |
| | 4 | | pC max | $C_L$ = 1 nF; Test Circuit 8 |
| Off Isolation | –90 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 9 |
| Total Harmonic Distortion, THD + N | 0.025 | | % typ | $R_L$ = 600 Ω, 2 V p-p, f = 20 Hz to 20 kHz |
| Channel-to-Channel Crosstalk (ADG659) | –90 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 11 |
| –3 dB Bandwidth | | | | |
| ADG658 | 210 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; |
| ADG659 | 400 | | MHz typ | Test Circuit 10 |
| $C_S$ (OFF) | 4 | | pF typ | f = 1 MHz |
| $C_D$ (OFF) | | | | |
| ADG658 | 23 | | pF typ | f = 1 MHz |
| ADG659 | 12 | | pF typ | f = 1 MHz |
| $C_D$, $C_S$ (ON) | | | | |
| ADG658 | 28 | | pF typ | f = 1 MHz |
| ADG659 | 16 | | pF typ | f = 1 MHz |
| POWER REQUIREMENTS | | | | $V_{DD}$ = +5.5 V, $V_{SS}$ = –5.5 V |
| $I_{DD}$ | 0.01 | | µA typ | Digital Inputs = 0 V or 5.5 V |
| | | 1 | µA max | |
| $I_{SS}$ | 0.01 | | µA typ | Digital Inputs = 0 V or 5.5 V |
| | | 1 | µA max | |

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C. Y Version: –40°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

3).'.% 3 $ 6 › 3 6 '.$ 6 UNLE!

| 0ARAM! | # | " 6ERS n # TO # | 9 6ER! n # TO # | 5N | 4EST #ONDITIONS |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 to $V_{DD}$ | V | $V_{DD}$ = 4.5 V, $V_{SS}$ = 0 V |
| On Resistance ($R_{ON}$) | 85 | | | Ω typ | $V_S$ = 0 V to 4.5 V, $I_S$ = 1 mA; |
| | 150 | 160 | 200 | Ω max | Test Circuit 1 |
| On Resistance Match between | 4.5 | | | Ω typ | $V_S$ = 3.5 V, $I_S$ = 1 mA |
| Channels ($\Delta R_{ON}$) | 8 | 9 | 10 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 13 | 14 | 16 | Ω typ | $V_{DD}$= 5 V, $V_{SS}$ = 0 V |
| | | | | | $V_S$ = 1.5 V to 4 V, $I_S$ = 1 mA |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = 5.5 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.005 | | | nA typ | $V_S$ = 1 V/4.5 V, $V_D$ = 4.5 V/1 V; |
| | ±0.2 | | ±5 | nA max | Test Circuit 2 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.005 | | | nA typ | $V_S$ = 1 V/4.5 V, $V_D$ = 4.5 V/1 V; |
| ADG658 | ±0.2 | | ±5 | nA max | Test Circuit 3 |
| ADG659 | ±0.1 | | ±2.5 | nA max | |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.005 | | | nA typ | $V_S$ = $V_D$ = 1 V or 4.5 V, Test Circuit 4 |
| ADG658 | ±0.2 | | ±5 | nA max | |
| ADG659 | ±0.1 | | ±2.5 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V max | |
| Input Current | | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | | µA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | | ±1 | µA max | |
| $C_{IN}$, Digital Input Capacitance | 2 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | | |
| $t_{TRANS}$ | 120 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 200 | 270 | 300 | ns max | $V_S$ = 3 V; Test Circuit 5 |
| $t_{ON}$ ($\overline{EN}$) | 120 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 190 | 245 | 280 | ns max | $V_S$ = 3 V; Test Circuit 7 |
| $t_{OFF}$ ($\overline{EN}$) | 35 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 50 | 60 | 70 | ns max | $V_S$ = 3 V; Test Circuit 7 |
| Break-Before-Make Time Delay, $t_{BBM}$ | 100 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | | 10 | ns min | $V_{S1}$ = $V_{S2}$ = 3 V; Test Circuit 6 |
| Charge Injection | 0.5 | | | pC typ | $V_S$ = 2.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; |
| | 1 | | | pC max | Test Circuit 8 |
| Off Isolation | –90 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | | Test Circuit 9 |
| Channel-to-Channel Crosstalk | –90 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; f = 1 MHz; |
| (ADG659) | | | | | Test Circuit 11 |
| –3 dB Bandwidth | | | | | |
| ADG658 | 180 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; |
| ADG659 | 330 | | | MHz typ | Test Circuit 10 |
| $C_S$ (OFF) | 5 | | | pF typ | f = 1 MHz |
| $C_D$ (OFF) | | | | | |
| ADG658 | 29 | | | pF typ | f = 1 MHz |
| ADG659 | 15 | | | pF typ | f = 1 MHz |
| $C_D$, $C_S$ (ON) | | | | | |
| ADG658 | 30 | | | pF typ | f = 1 MHz |
| ADG659 | 16 | | | pF typ | f = 1 MHz |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 5.5 V |
| $I_{DD}$ | 0.01 | | | µA typ | Digital Inputs = 0 V or 5.5 V |
| | | | 1 | µA max | |

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C. Y Version: –40°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifcations subject to change without notice.

# !$'  !$'  n30%#

## 3).'.% 3 $ 6 T( 3 6 '.$ 6 UNLE!

| 0ARAMI | " 6ERS n # # TO # | 9 6ER! n # TO # | 5N | 4EST #ONDITIONS |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 to $V_{DD}$ | V | $V_{DD}$ = 2.7 V, $V_{SS}$ = 0 V |
| On Resistance ($R_{ON}$) | 185 | | Ω typ | $V_S$ = 0 V to 2.7 V, $I_S$ = 0.1 mA; |
| | 300 350 | 400 | Ω max | Test Circuit 1 |
| On Resistance Match between | 2 | | Ω typ | $V_S$ = 1.5 V, $I_S$ = 0.1 mA |
| Channels ($\Delta R_{ON}$) | 4.5 6 | 7 | Ω max | |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = 3.3 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.005 | | nA typ | $V_S$ = 1 V/3 V, $V_D$ = 3 V/1 V; |
| | ±0.2 | ±5 | nA max | Test Circuit 2 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.005 | | nA typ | $V_S$ = 1 V/3 V, $V_D$ = 3 V/1 V; |
| ADG658 | ±0.2 | ±5 | nA max | Test Circuit 3 |
| ADG659 | ±0.1 | ±2.5 | nA max | |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.005 | | nA typ | $V_S$ = $V_D$ = 1 V or 3 V; Test Circuit 4 |
| ADG658 | ±0.2 | ±5 | nA max | |
| ADG659 | ±0.1 | ±2.5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.5 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | µA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±1 | µA max | |
| $C_{IN}$, Digital Input Capacitance | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{TRANS}$ | 200 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 370 440 | 490 | ns max | $V_S$ = 1.5 V; Test Circuit 7 |
| $t_{ON}$ ($\overline{EN}$) | 230 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 370 440 | 490 | ns max | $V_S$ = 1.5 V; Test Circuit 7 |
| $t_{OFF}$ ($\overline{EN}$) | 50 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 80 90 | 110 | ns max | $V_S$ = 1.5 V; Test Circuit 7 |
| Break-Before-Make Time Delay, $t_{BBM}$ | 200 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | | 10 | ns min | $V_{S1}$ = $V_{S2}$ = 1.5 V; Test Circuit 6 |
| Charge Injection | 1 | | pC typ | $V_S$ = 1.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; |
| | 2 | | pC max | Test Circuit 8 |
| Off Isolation | –90 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 9 |
| Channel-to-Channel Crosstalk (ADG659) | –90 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 11 |
| –3 dB Bandwidth | | | | |
| ADG658 | 160 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; |
| ADG659 | 300 | | MHz typ | Test Circuit 10 |
| $C_S$ (OFF) | 5 | | pF typ | f = 1 MHz |
| $C_D$ (OFF) | | | | |
| ADG658 | 29 | | pF typ | f = 1 MHz |
| ADG659 | 15 | | pF typ | f = 1 MHz |
| $C_D$, $C_S$ (ON) | | | | |
| ADG658 | 30 | | pF typ | f = 1 MHz |
| ADG659 | 16 | | pF typ | f = 1 MHz |
| POWER REQUIREMENTS | | | | $V_{DD}$ = 3.6 V |
| $I_{DD}$ | 0.01 | | µA typ | Digital Inputs = 0 V or 3.6 V |
| | | 1 | µA max | |

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C. Y Version: –40°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

## !"3/.54% -!8)-5- 2!4).'3

($T_A$ = 25°C, unless otherwise noted.)

$V_{DD}$ to $V_{SS}$ . . . . . 13 V
$V_{DD}$ to GND . . . . . –0.3 V to +13 V
$V_{SS}$ to GND . . . . . +0.3 V to –6.5 V
Analog Inputs[2] . . . . . $V_{SS}$ – 0.3 V to $V_{DD}$ + 0.3 V
Digital Inputs[2] . . . . . GND – 0.3 V to $V_{DD}$ + 0.3 V
or 10 mA, whichever occurs frst
Peak Current, S or D . . . . . 40 mA
(Pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D . . . . . 20 mA
Operating Temperature Range
Automotive (Y Version) . . . . . –40°C to +125°C
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
$\theta_{JA}$ Thermal Impedance, 16-Lead TSSOP . . . . . 150.4°C/W
$\theta_{JA}$ Thermal Impedance (4-Layer Board),
16-Lead LFCSP . . . . . 70°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C
ESD . . . . . 5.5 kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specif cation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at $A_X$, $\overline{EN}$, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## #!54)/.

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG658/ADG659 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


## /2$%2).' '5)$%

| -ODEL | 4EMPERATURE | 0ACKAGE $ESCRIPTION | 0ACKAGE /PTION |
|---|---|---|---|
| ADG658YRU | –40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG658BCP | –40°C to +85°C | Lead Frame Chip Scale Package (LFCSP) | CP-16 |
| ADG659YRU | –40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG659BCP | –40°C to +85°C | Lead Frame Chip Scale Package (LFCSP) | CP-16 |

### 4ABLE ) !$' 4RUTH

| ! | ! | ! | <E | 3WITCH #ONDITION |
|---|---|---|---|---|
| X | X | X | 1 | NONE |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 0 | 3 |
| 0 | 1 | 1 | 0 | 4 |
| 1 | 0 | 0 | 0 | 5 |
| 1 | 0 | 1 | 0 | 6 |
| 1 | 1 | 0 | 0 | 7 |
| 1 | 1 | 1 | 0 | 8 |

X = Don't Care

### 4ABLE )) !$' 4RUTH

| ! | ! | <E | /N 3WITCH |
|---|---|---|---|
| X | X | 1 | NONE |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 2 |
| 1 | 0 | 0 | 3 |
| 1 | 1 | 0 | 4 |

X = Don't Care

### 0). #/.&)'52!4)/.3

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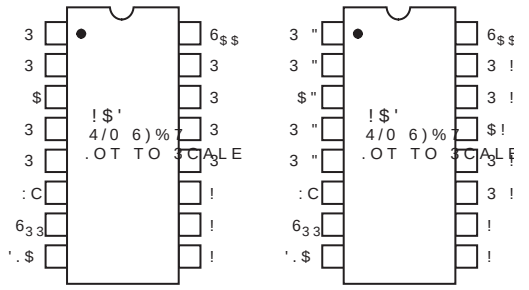


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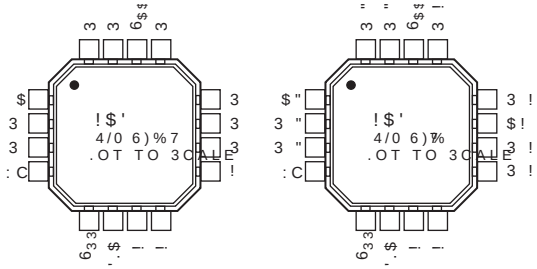

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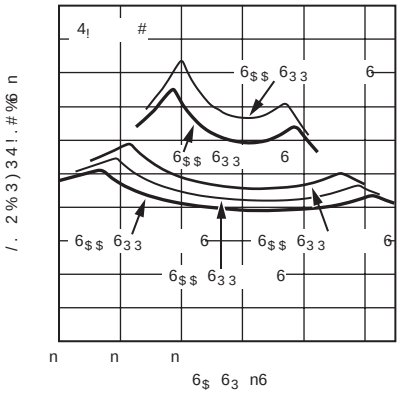
| 0ARAM | $ESCRI |
|---|---|
| $V_{DD}$ | Most Positive Power Supply Potential. |
| $V_{SS}$ | Most Negative Power Supply Potential. |
| $I_{DD}$ | Positive Supply Current. |
| $I_{SS}$ | Negative Supply Current. |
| GND | Ground (0 V) Reference. |
| S | Source Terminal. May be an input or output. |
| D | Drain Terminal. May be an input or output. |
| $A_X$ | Logic Control Input. |
| $\overline{EN}$ | Active Low Digital Input. When high, device is disabled and all switches are OFF. When low, $A_X$ logic inputs determine ON switch. |
| $V_D$ ($V_S$) | Analog Voltage on Terminals D, S. |
| $R_{ON}$ | Ohmic Resistance between D and S. |
| $\Delta R_{ON}$ | On Resistance Match between Any Two Channels, i.e., $R_{ON}$ max – $R_{ON}$ min. |
| $R_{FLAT(ON)}$ | Flatness is defined as the difference between the maximum and minimum value of ON Resistance as measured over the specified analog signal range. |
| $I_S$ (OFF) | Source Leakage Current with the Switch OFF. |
| $I_D$ (OFF) | Drain Leakage Current with the Switch OFF. |
| $I_D$, $I_S$ (ON) | Channel Leakage Current with the Switch ON. |
| $V_{INL}$ | Maximum Input Voltage for Logic 0. |
| $V_{INH}$ | Minimum Input Voltage for Logic 1. |
| $I_{INL}$($I_{INH}$) | Input Current of the Digital Input. |
| $C_S$ (OFF) | OFF Switch Source Capacitance. Measured with reference to ground. |
| $C_D$ (OFF) | OFF Switch Drain Capacitance. Measured with reference to ground. |
| $C_D$, $C_S$ (ON) | ON Switch Capacitance. Measured with reference to ground. |
| $C_{IN}$ | Digital Input Capacitance. |
| $t_{ON}$ | Delay between Applying the Digital Control Input and the Output Switching ON. See Test Circuit 7. |
| $t_{OFF}$ | Delay between Applying the Digital Control Input and the Output Switching OFF. |
| $t_{BBM}$ | ON Time. Measured between 80% points of both switches when switching from one address state to another. |
| Charge Injection | Measure of the Glitch Impulse Transferred from the Digital Input to the Analog Output during Switching. |
| Off Isolation | Measure of Unwanted Signal Coupling through an OFF Switch. |
| Crosstalk | Measure of Unwanted Signal Coupled through from One Channel to Another as a Result of Parasitic Capacitance. |
| Bandwidth | The Frequency at which the Output is Attenuated by 3 dB. |
| On Response | The Frequency Response of the ON Switch. |
| Insertion Loss | The Loss Due to the ON Resistance of the Switch. |

# 4YPICAL 0ERFORMANCE #H



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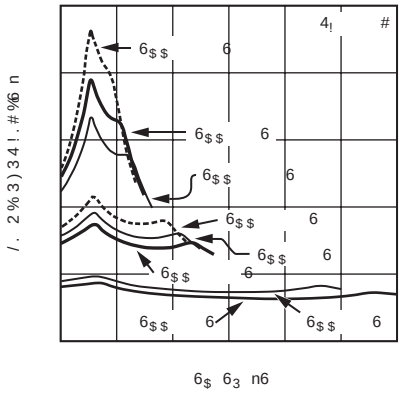

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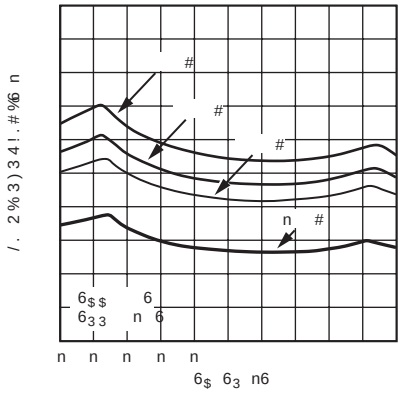

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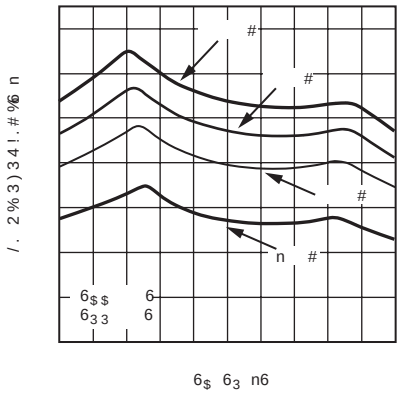

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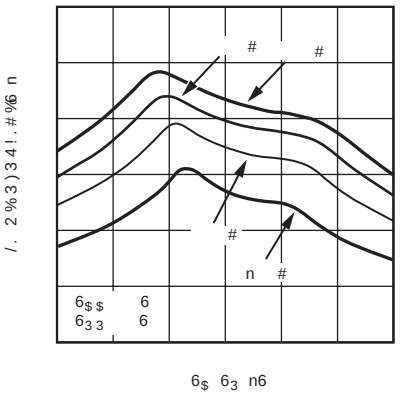

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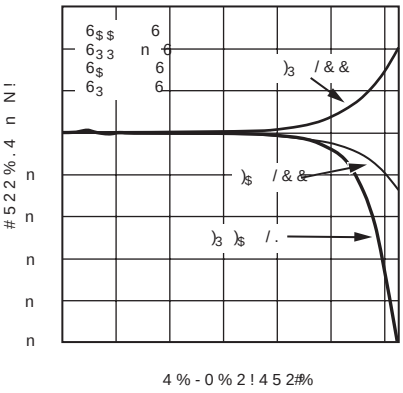
FOR $IFFERENT 4
3INGLE 3



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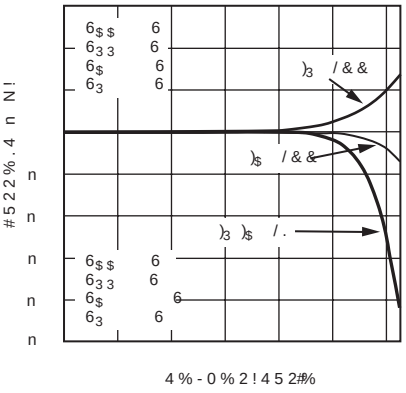

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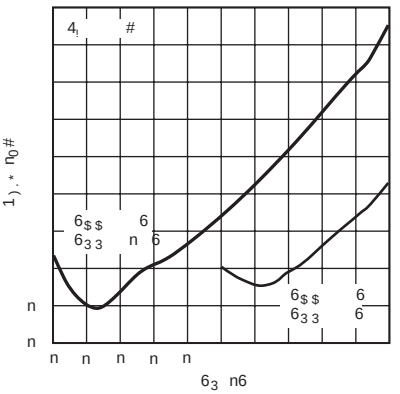
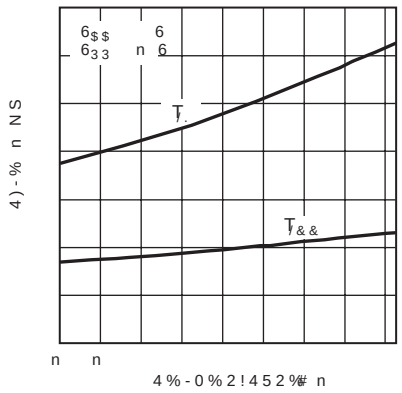


40# #HARGE )N
3OURCE 6



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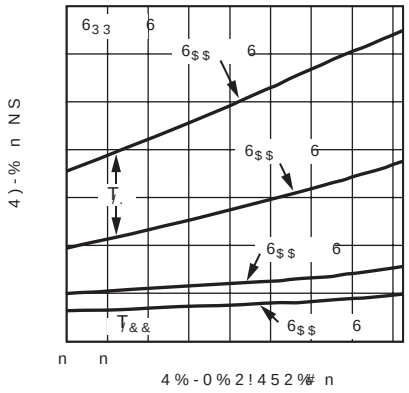


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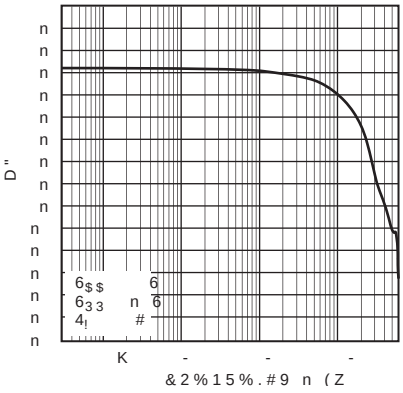
4EMPERATURE 3IN

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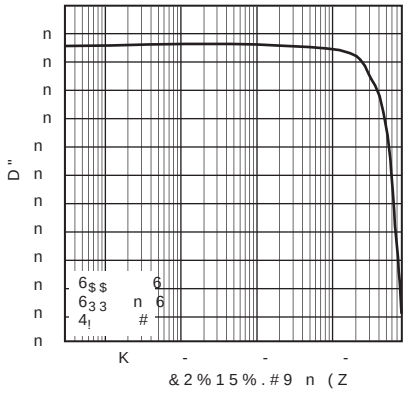


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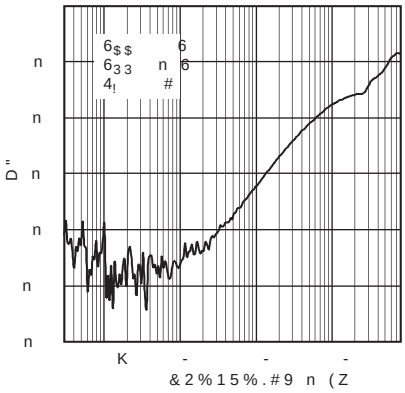
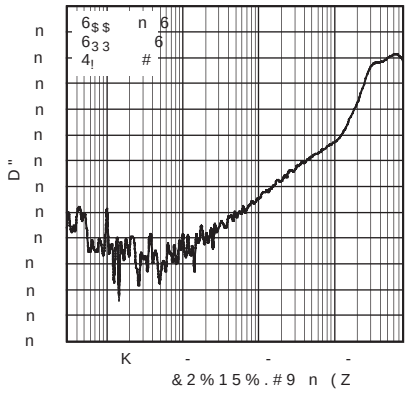
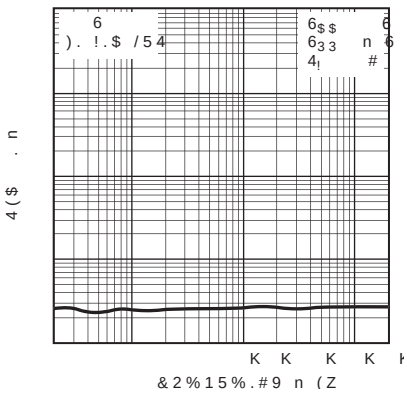


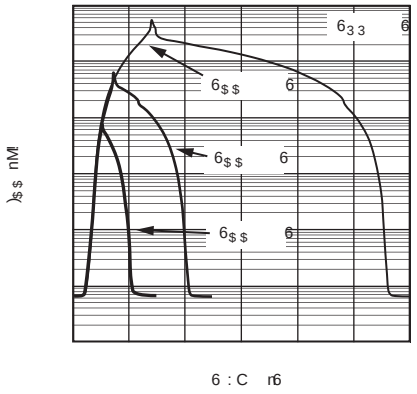

40# /&& )SOLATION VS



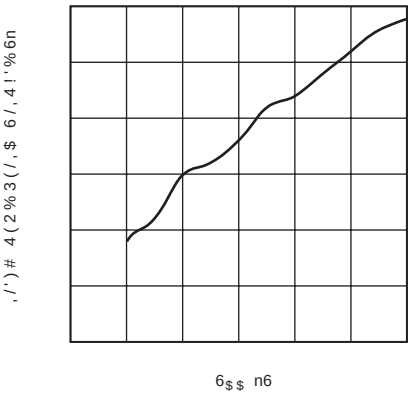

40# #ROSSTARLEKQVS




40# 4($ .O

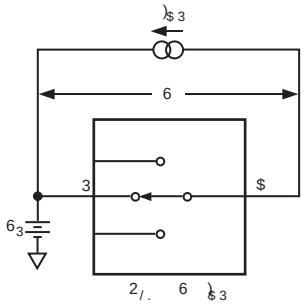



40# $$ #URRENT VS

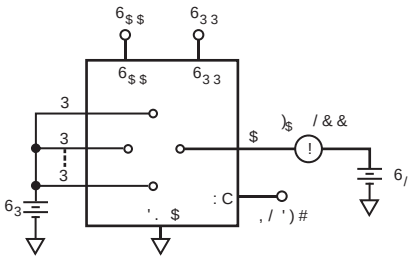



40# ,OGIC 4H
6OLTAGE VS 3UP

# 4EST :




4EST #IRCUIT /N

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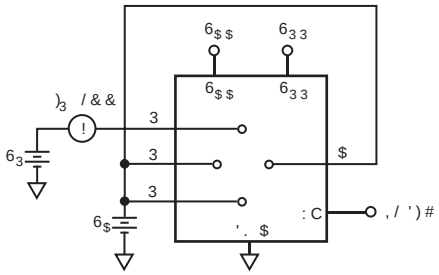


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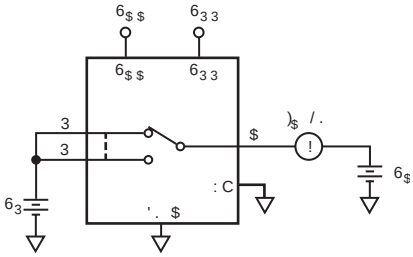


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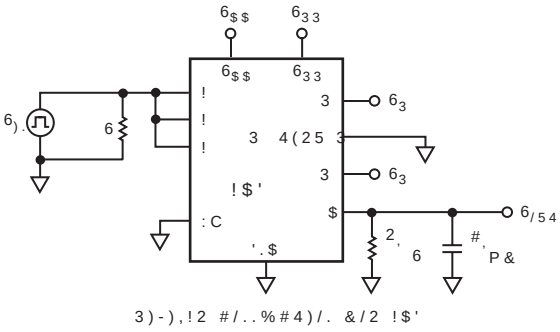


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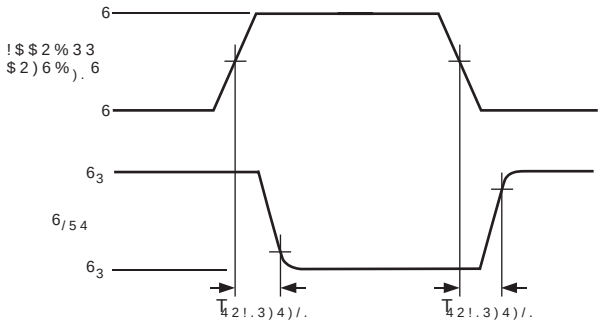
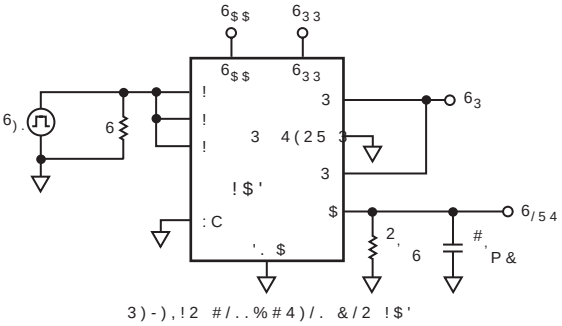
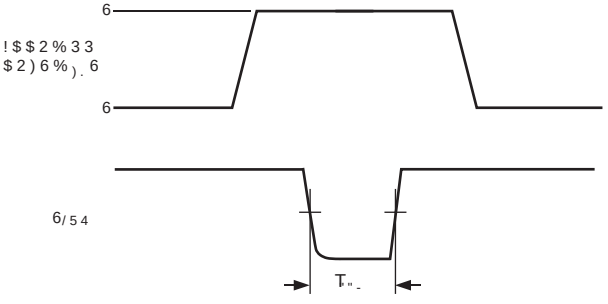



3WITCHING 4 42!.3)4)/

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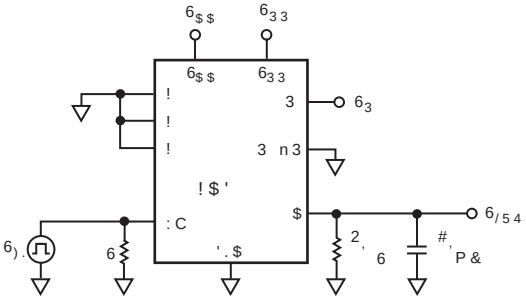
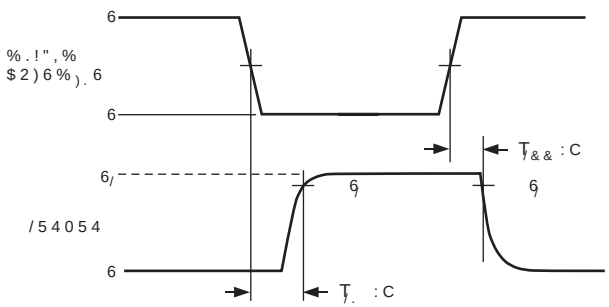
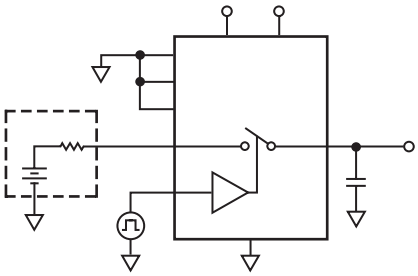
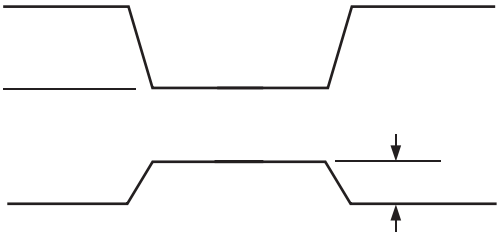



4EST #IRCUIT %l/. <E /&& <E





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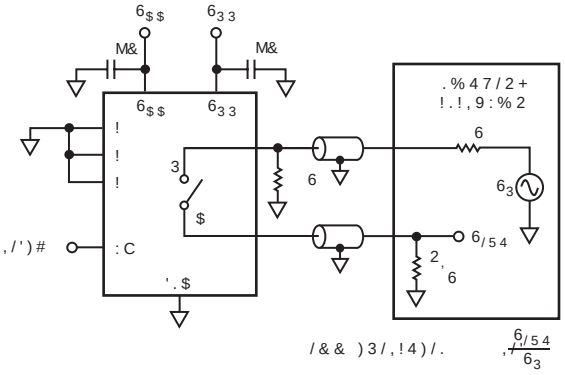


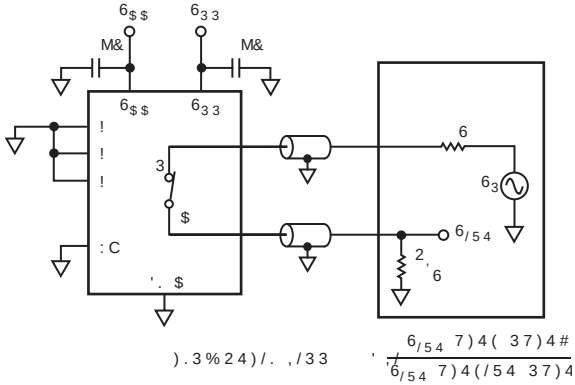


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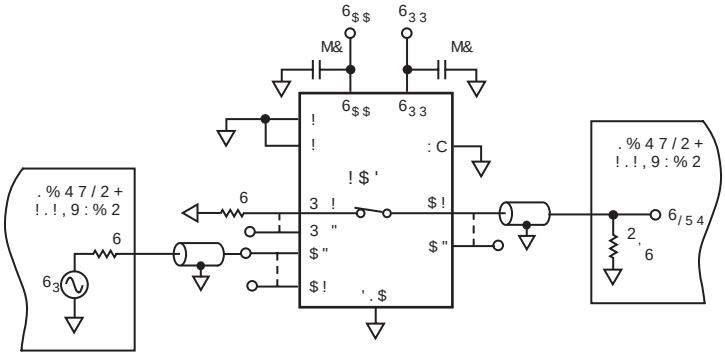
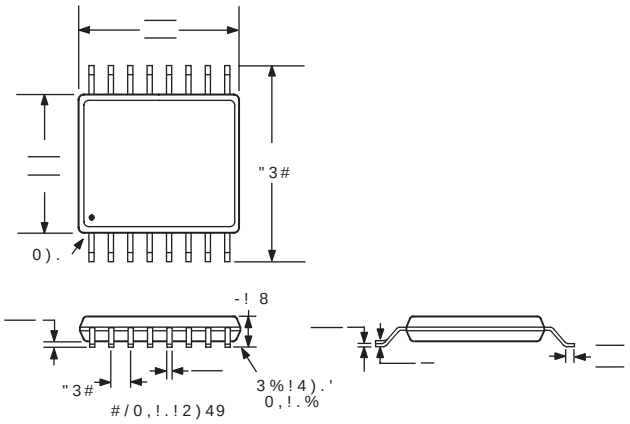



4EST #IRCUIT #HANNEL TC

/54.).% $)-%.3)/.3

,EAD 4HIN 3HRINK 3MALL /UTLINE
25

Dimensions shown in millimeters




#/-0,)!.4 4/ *%$%# 34!.$!2$3 -/  !"

,EAD ,EAD &RAME #HIP 3CALE
MM  MM "C
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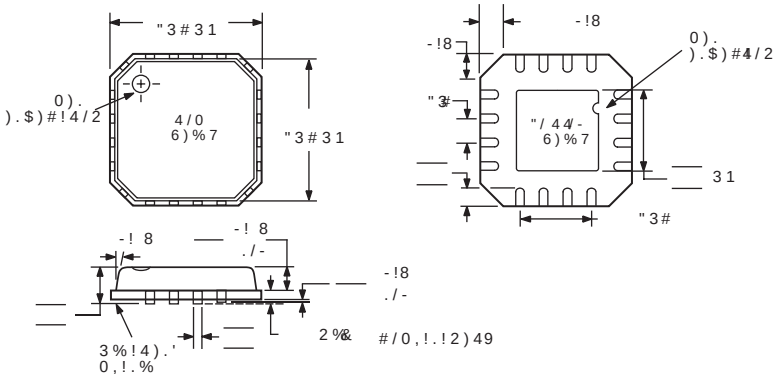
Dimensions shown in millimeters




#/-0,)!.4 4/ *%$%# 34!.$!2$3 -/  6''#

n n

02).4%$ ). 5

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