ADCS7476 ADCS7477 ADCS7478 1MSPS, 12-/10-/8-Bit A/D Converters in SOT-23 & WSON

Check for Samples: ADCS7476, ADCS7477, ADCS7478

FEATURES

- **Variable Power Management**
- **Packaged in 6-Lead, SOT-23 and WSON**
- **Power Supply used as Reference**
- **Single +2.7V to +5.25V Supply Operation**
- **SPI™/QSPI™/MICROWIRE™/DSP Compatible**

APPLICATIONS

- **Automotive Navigation**
- **FA/ATM Equipment**
- **Portable Systems**
- **Medical Instruments**
- **Mobile Communications**
- **Instrumentation and Control Systems**

KEY SPECIFICATIONS

- **Resolution with no Missing Codes 12/10/8 bits**
- **Conversion Rate 1 MSPS**
- **DNL +0.5, -0.3 LSB (typ)**
- **INL ± 0.4 LSB (typ)**
- **Power Consumption**
  - **3V Supply 2 mW (typ)**
  - **5V Supply 10 mW (typ)**

DESCRIPTION

The ADCS7476, ADCS7477, and ADCS7478 are low power, monolithic CMOS 12-, 10- and 8-bit analog-to-digital converters that operate at 1 MSPS. The ADCS7476/77/78 are drop-in replacements for Analog Devices' AD7476/77/78. Each device is based on a successive approximation register architecture with internal track-and-hold. The serial interface is compatible with several standards, such as SPI™, QSPI™, MICROWIRE™, and many common DSP serial interfaces.

The ADCS7476/77/78 uses the supply voltage as a reference, enabling the devices to operate with a full-scale input range of 0 to V_{DD}. The conversion rate is determined from the serial clock (SCLK) speed. These converters offer a shutdown mode, which can be used to trade throughput for power consumption. The ADCS7476/77/78 is operated with a single supply that can range from +2.7V to +5.25V. Normal power consumption during continuous conversion, using a +3V or +5V supply, is 2 mW or 10 mW respectively. The power down feature, which is enabled by a chip select ($\overline{CS}$) pin, reduces the power consumption to under 5 µW using a +5V supply. All three converters are available in a 6-lead, SOT-23 package and in a 6-lead WSON, both of which provide an extremely small footprint for applications where space is a critical consideration. These products are designed for operation over the automotive/extended industrial temperature range of −40°C to +125°C.

Connection Diagram

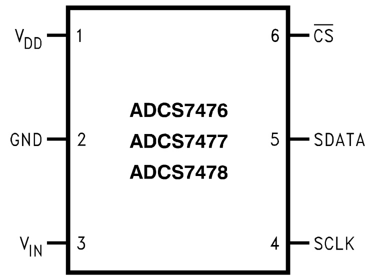
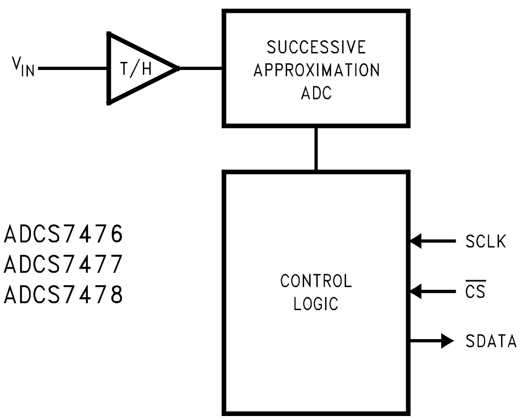


Figure 1. 6-Lead SOT-23 or WSON
See DBV or NGF Package

PIN DESCRIPTIONS

Pin No.	Symbol	Description
ANALOG I/O		
3	V_{IN}	Analog input. This signal can range from 0V to V_{DD}.
DIGITAL I/O		
4	SCLK	Digital clock input. The range of frequencies for this input is 10 kHz to 20 MHz, with guaranteed performance at 20 MHz. This clock directly controls the conversion and readout processes.
5	SDATA	Digital data output. The output words are clocked out of this pin by the SCLK pin.
6	$\overline{CS}$	Chip select. A conversion process begins on the falling edge of $\overline{CS}$.
POWER SUPPLY		
1	V_{DD}	Positive supply pin. These pins should be connected to a quiet +2.7V to +5.25V source and bypassed to GND with 0.1 µF and 1 µF monolithic capacitors located within 1 cm of the power pin. The ADCS7476/77/78 uses this power supply as a reference, so it should be thoroughly bypassed.
2	GND	The ground return for the supply.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage V_{DD}	−0.3V to +6.5V
Voltage on Any Analog Pin to GND	−0.3V to V_{DD} +0.3V
Voltage on Any Digital Pin to GND	-0.3V to 6.5V
Input Current at Any Pin (3)	±10 mA
ESD Susceptibility Human Body Model Machine Model	 3500V 200V
Soldering Temperature, Infrared, 10 seconds	 215°C
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C

(1) Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not implied. Exposure to maximum ratings for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Except power supply pins.

Operating Ratings

Operating Temperature Range	T_{MIN} = −40°C ≤ T_A ≤ T_{MAX} = +125°C
V_{DD} Supply Voltage	+2.7V to +5.25V
Digital Input Pins Voltage Range (1)	+2.7V to +5.25V

(1) Independent of supply voltage.

Package Thermal Resistance

Package	θ_{JA}
6-Lead SOT-23	265°C / W
6-Lead WSON	78°C / W

ADCS7476/ADCS7477/ADCS7478 Specifications(1)
ADCS7476 Converter Electrical Characteristics

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes	V_{DD} = 2.7V to 3.6V, −40°C ≤ T_A ≤ 125°C		**12**	Bits
INL	Integral Non-Linearity	V_{DD} = 2.7V to 3.6V, −40°C ≤ T_A ≤ 85°C	±0.4	**±1**	LSB (max)
		V_{DD} = 2.7V to 3.6V, T_A = 125°C		+1 -1.1	LSB (max) LSB (min)
DNL	Differential Non-Linearity	V_{DD} = 2.7V to 3.6V, −40°C ≤ T_A ≤ 85°C	+0.5 -0.3	**+1** **-0.9**	LSB (max) LSB (min)
		V_{DD} = 2.7V to 3.6V, T_A = 125°C		±1	LSB (max)
V_{OFF}	Offset Error	V_{DD} = 2.7V to 3.6V, −40°C ≤ T_A ≤ 125°C	±0.1	**±1.2**	LSB (max)
GE	Gain Error	V_{DD} = 2.7V to 3.6V, −40°C ≤ T_A ≤ 125°C	±0.2	**±1.2**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 100 kHz, −40°C ≤ T_A ≤ 125°C	72	**70**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 100 kHz, −40°C ≤ T_A ≤ 85°C	72.5	**70.8**	dB (min)
		f_{IN} = 100 kHz, T_A = 125°C		70.6	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 100 kHz	-80		dB
SFDR	Spurious-Free Dynamic Range	f_{IN} = 100 kHz	82		dB
IMD	Intermodulation Distortion, Second Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-78		dB
	Intermodulation Distortion, Third Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-78		dB
FPBW	-3 dB Full Power Bandwidth	+5V Supply	11		MHz
		+3V Supply	8		MHz
POWER SUPPLY CHARACTERISTICS					
V_{DD}	Supply Voltage	−40°C ≤ T_A ≤ 125°C		**2.7**	V (min)
				5.25	V (max)

(1) Data sheet min/max specification limits are guaranteed by design, test, or statistical analysis.

ADCS7476/ADCS7477/ADCS7478 Specifications[(1)]
ADCS7476 Converter Electrical Characteristics (continued)

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
I_{DD}	Normal Mode (Static)	V_{DD} = +4.75V to +5.25V, SCLK On or Off	2		mA
		V_{DD} = +2.7V to +3.6V, SCLK On or Off	1		mA
	Normal Mode (Operational)	V_{DD} = +4.75V to +5.25V, f_{SAMPLE} = 1 MSPS	2.0	**3.5**	mA (max)
		V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 1 MSPS	0.6	**1.6**	mA (max)
	Shutdown Mode	V_{DD} = +5V, SCLK Off	0.5		µA
		V_{DD} = +5V, SCLK On	60		µA
P_D	Power Consumption, Normal Mode (Operational)	V_{DD} = +5V, f_{SAMPLE} = 1 MSPS	10	**17.5**	mW (max)
		V_{DD} = +3V, f_{SAMPLE} = 1 MSPS	2	**4.8**	mW (max)
	Power Consumption, Shutdown Mode	V_{DD} = +5V, SCLK Off	2.5		µW
		V_{DD} = +3V, SCLK Off	1.5		µW
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to V_{DD}		V
I_{DCL}	DC Leakage Current			**±1**	µA (max)
C_{INA}	Analog Input Capacitance		30		pF
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Input High Voltage			**2.4**	V (min)
V_{IL}	Input Low Voltage	V_{DD} = +5V		**0.8**	V (max)
		V_{DD} = +3V		**0.4**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_{DD}	±10 nA	**±1**	µA (max)
C_{IND}	Digital Input Capacitance		2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, V_{DD} = +2.7V to +5.25V		**V_{DD} −0.2**	V (min)
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		**0.4**	V (max)
I_{OL}	TRI-STATE Leakage Current			**±10**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Clock Frequency	−40°C ≤ T_A ≤ 125°C		**20**	MHz (max)
DC	SCLK Duty Cycle			**40** **60**	% (min) % (max)
t_{TH}	Track/Hold Acquisition Time			**400**	ns (max)
f_{RATE}	Throughput Rate	See USING THE ADCS7476/77/78		**1**	MSPS (max)
t_{AD}	Aperture Delay		3		ns
t_{AJ}	Aperture Jitter		30		ps

ADCS7476/ADCS7477/ADCS7478 Specifications[(1)] ADCS7477 Converter Electrical Characteristics

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
STATIC CONVERTER CHARACTERISTICS					

(1) Data sheet min/max specification limits are guaranteed by design, test, or statistical analysis.

ADCS7476/ADCS7477/ADCS7478 Specifications[1] ADCS7477 Converter Electrical Characteristics (continued)

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
	Resolution with No Missing Codes			**10**	Bits
INL	Integral Non-Linearity		±0.2	**±0.7**	LSB (max)
DNL	Differential Non-Linearity		+0.3 -0.2	**±0.7**	LSB (max) LSB (min)
V_{OFF}	Offset Error		±0.1	**±0.7**	LSB (max)
GE	Gain Error		±0.2	**±1**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 100 kHz	61.7	**61**	dBFS (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 100 kHz	62		dB
THD	Total Harmonic Distortion	f_{IN} = 100 kHz	-77	**-73**	dB (max)
SFDR	Spurious-Free Dynamic Range	f_{IN} = 100 kHz	78	**74**	dB (min)
IMD	Intermodulation Distortion, Second Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-78		dB
	Intermodulation Distortion, Third Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-78		dB
FPBW	-3 dB Full Power Bandwidth	+5V Supply	11		MHz
		+3V Supply	8		MHz
POWER SUPPLY CHARACTERISTICS					
V_{DD}	Supply Voltage			**2.7** **5.25**	V (min) V (max)
I_{DD}	Normal Mode (Static)	V_{DD} = +4.75V to +5.25V, SCLK On or Off	2		mA
		V_{DD} = +2.7V to +3.6V, SCLK On or Off	1		mA
	Normal Mode (Operational)	V_{DD} = +4.75V to +5.25V, f_{SAMPLE} = 1 MSPS	2.0	**3.5**	mA (max)
		V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 1 MSPS	0.6	**1.6**	mA (max)
	Shutdown Mode	V_{DD} = +5V, SCLK Off	0.5		µA (max)
		V_{DD} = +5V, SCLK On	60		µA (max)
P_D	Power Consumption, Normal Mode (Operational)	V_{DD} = +5V, f_{SAMPLE} = 1 MSPS	10	**17.5**	mW (max)
		V_{DD} = +3V, f_{SAMPLE} = 1 MSPS	2	**4.8**	mW (max)
	Power Consumption, Shutdown Mode	V_{DD} = +5V, SCLK Off	2.5		µW (max)
		V_{DD} = +3V, SCLK Off	1.5		µW (max)
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to V_{DD}		V
I_{DCL}	DC Leakage Current			**±1**	µA (max)
C_{INA}	Analog Input Capacitance		30		pF
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Input High Voltage			**2.4**	V (min)
V_{IL}	Input Low Voltage	V_{DD} = +5V		**0.8**	V (max)
		V_{DD} = +3V		**0.4**	V (max)
I_{IN}	Input Current	V_{IN} = 0V or V_{DD}	±10 nA	**±1**	µA (max)
C_{IND}	Digital Input Capacitance		2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, V_{DD} = +2.7V to +5.25V		**V_{DD} −0.2**	V (min)

ADCS7476/ADCS7477/ADCS7478 Specifications[(1)] ADCS7477 Converter Electrical Characteristics (continued)

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		**0.4**	V (max)
I_{OL}	TRI-STATE Leakage Current			**±10**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Clock Frequency			**20**	MHz (max)
DC	SCLK Duty Cycle			**40** **60**	% (min) % (max)
t_{TH}	Track/Hold Acquisition Time			**400**	ns (max)
f_{RATE}	Throughput Rate	See USING THE ADCS7476/77/78		**1**	MSPS (max)
t_{AD}	Aperture Delay		3		ns
t_{AJ}	Aperture Jitter		30		ps

ADCS7476/ADCS7477/ADCS7478 Specifications[1]
ADCS7478 Converter Electrical Characteristics

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**8**	Bits
INL	Integral Non-Linearity		±0.05	**±0.3**	LSB (max)
DNL	Differential Non-Linearity		±0.07	**±0.3**	LSB (max)
V_{OFF}	Offset Error		±0.03	**±0.3**	LSB (max)
GE	Gain Error		±0.08	**±0.4**	LSB (max)
	Total Unadjusted Error		±0.07	**±0.3**	LSB (max)
DYNAMIC CONVERTER CHARACTERISTICS					
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 100 kHz	49.7	**49**	dB (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 100 kHz	49.7		dB
THD	Total Harmonic Distortion	f_{IN} = 100 kHz	-77	**-65**	dB (max)
SFDR	Spurious-Free Dynamic Range	f_{IN} = 100 kHz	69	**65**	dB (min)
IMD	Intermodulation Distortion, Second Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-68		dB
	Intermodulation Distortion, Third Order Terms	f_a = 103.5 kHz, f_b = 113.5 kHz	-68		dB
FPBW	-3 dB Full Power Bandwidth	+5V Supply	11		MHz
		+3V Supply	8		MHz
POWER SUPPLY CHARACTERISTICS					
V_{DD}	Supply Voltage			**2.7** **5.25**	V (min) V (max)
I_{DD}	Normal Mode (Static)	V_{DD} = +4.75V to +5.25V, SCLK On or Off	2		mA
		V_{DD} = +2.7V to +3.6V, SCLK On or Off	1		mA
	Normal Mode (Operational)	V_{DD} = +4.75V to +5.25V, f_{SAMPLE} = 1 MSPS	2.0	**3.5**	mA (max)
		V_{DD} = +2.7V to +3.6V, f_{SAMPLE} = 1 MSPS	0.6	**1.6**	mA (max)
	Shutdown Mode	V_{DD} = +5V, SCLK Off	0.5		µA (max)
		V_{DD} = +5V, SCLK On	60		µA (max)
P_D	Power Consumption, Normal Mode (Operational)	V_{DD} = +5V, f_{SAMPLE} = 1 MSPS	10	**17.5**	mW (max)
		V_{DD} = +3V, f_{SAMPLE} = 1 MSPS	2	**4.8**	mW (max)
	Power Consumption= Shutdown Mode	V_{DD} = +5V, SCLK Off	2.5		µW (max)
		V_{DD} = +3V, SCLK Off	1.5		µW (max)
ANALOG INPUT CHARACTERISTICS					
V_{IN}	Input Range		0 to V_{DD}		V
I_{DCL}	DC Leakage Current			**±1**	µA (max)
C_{INA}	Analog Input Capacitance		30		pF
DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Input High Voltage			**2.4**	V (min)
V_{IL}	Input Low Voltage	V_{DD} = +5V		**0.8**	V (max)
		V_{DD} = +3V		**0.4**	V (max)
I_{IN}	Digital Input Current	V_{IN} = 0V or V_{DD}	±10 nA	**±1**	µA (max)
C_{IND}	Input Capacitance		2	**4**	pF(max)
DIGITAL OUTPUT CHARACTERISTICS					

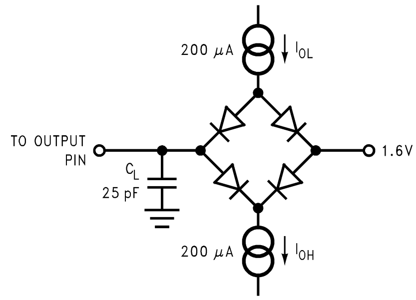
(1) Data sheet min/max specification limits are guaranteed by design, test, or statistical analysis.

ADCS7476/ADCS7477/ADCS7478 Specifications (1) ADCS7478 Converter Electrical Characteristics (continued)

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted. **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Typical	Limits	Units
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA, V_{DD} = +2.7V to +5.25V		**V_{DD} −0.2**	V (min)
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		**0.4**	V (max)
I_{OL}	TRI-STATE Leakage Current			**±10**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance		2	**4**	pF (max)
	Output Coding		Straight (Natural) Binary		
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Clock Frequency			**20**	MHz (max)
DC	SCLK Duty Cycle			**40** **60**	% (min) % (max)
t_{TH}	Track/Hold Acquisition Time			**400**	ns (max)
f_{RATE}	Throughput Rate	See Applications Information		**1**	MSPS (min)
t_{AD}	Aperture Delay		3		ns
t_{AJ}	Aperture Jitter		30		ps

Figure 2. Timing Test Circuit



Timing Test Circuit ADCS7476/ADCS7477/ADCS7478 Timing Specifications

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless otherwise noted. (1)

Symbol	Parameter	Conditions	Typical	Limits	Units
$t_{CONVERT}$			16 x t_{SCLK}		
t_{QUIET}	(2)			**50**	ns (min)
t_1	Minimum $\overline{CS}$ Pulse Width			**10**	ns (min)
t_2	$\overline{CS}$ to SCLK Setup Time			**10**	ns (min)
t_3	Delay from $\overline{CS}$ Until SDATA TRI-STATE Disabled (3)			**20**	ns (max)
t_4	Data Access Time after SCLK Falling Edge (4)	V_{DD} = +2.7 to +3.6		**40**	ns (max)
		V_{DD} = +4.75 to +5.25		**20**	ns (max)
t_5	SCLK Low Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_6	SCLK High Pulse Width			**0.4 x t_{SCLK}**	ns (min)
t_7	SCLK to Data Valid Hold Time	V_{DD} = +2.7 to +3.6		**7**	ns (min)
		V_{DD} = +4.75 to +5.25		**5**	ns (min)

(1) All input signals are specified as t_r = t_f = 5 ns (10% to 90% V_{DD}) and timed from 1.6V.
(2) Minimum Quiet Time Required Between Bus Relinquish and Start of Next Conversion
(3) Measured with the load circuit shown above, and defined as the time taken by the output to cross 1.0V.
(4) Measured with the load circuit shown above, and defined as the time taken by the output to cross 1.0V or 2.0V.

Timing Test Circuit ADCS7476/ADCS7477/ADCS7478 Timing Specifications (continued)

The following specifications apply for V_{DD} = +2.7V to 5.25V, f_{SCLK} = 20 MHz, **Boldface limits apply for T_A = −40°C to +85°C**: all other limits T_A = 25°C, unless noted otherwise. (1)

Symbol	Parameter	Conditions	Typical	Limits	Units
t_8	SCLK Falling Edge to SDATA High Impedance (5)	V_{DD} = +2.7 to +3.6		**25**	ns (max)
				6	ns (min)
		V_{DD} = +4.75 to +5.25		**25**	ns (max)
				5	ns (min)
$t_{POWER-UP}$	Power-Up Time from Full Power-Down		1		µs

(5) t_8 is derived from the time taken by the outputs to change by 0.5V with the loading circuit shown above. The measured number is then adjusted to remove the effects of charging or discharging the 25pF capacitor. This means t_8 is the true bus relinquish time, independent of the bus loading.

Specification Definitions

APERTURE DELAY is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation of the last code transition (111...110) to (111...111) from the ideal (V_{REF} - 1.5 LSB for ADCS7476 and ADCS7477, V_{REF} - 1 LSB for ADCS7478), after adjusting for offset error.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the either the two second order or all four third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dBFS.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADCS7476/77/78 is guaranteed not to have any missing codes.

OFFSET ERROR is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB for the ADCS7476 and ADCS7477, and GND + 1 LSB for the ADCS7478).

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first five harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_6^2}{f_1^2}}$$

where

- f_1 is the RMS power of the fundamental (output) frequency
- f_2 through f_6 are the RMS power in the first 5 harmonic frequencies (1)

TOTAL UNADJUSTED ERROR is the worst deviation found from the ideal transfer function. As such, it is a comprehensive specification which includes full scale error, linearity error, and offset error.

Timing Diagrams

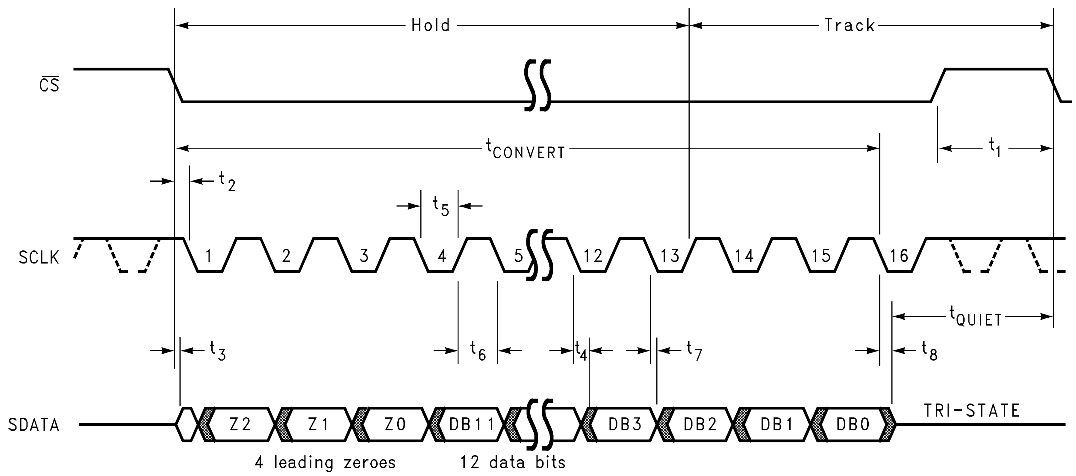


Figure 3. ADCS7476 Serial Interface Timing Diagram

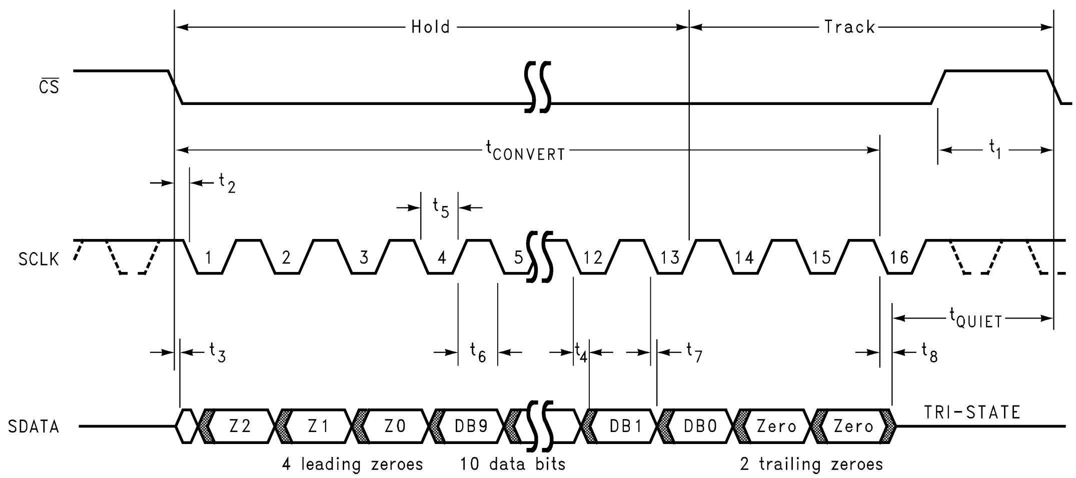


Figure 4. ADCS7477 Serial Interface Timing Diagram

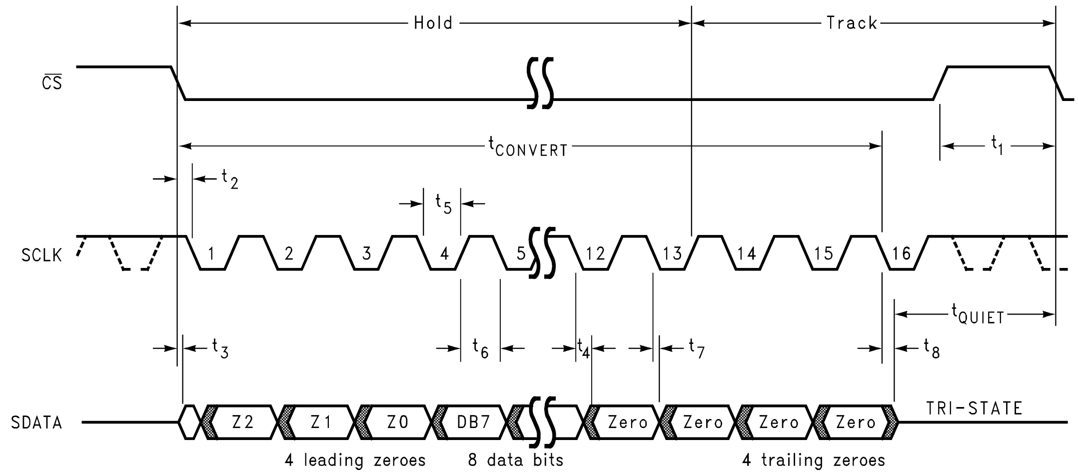


Figure 5. ADCS7478 Serial Interface Timing Diagram

Typical Performance Characteristics

T_A = +25°C, V_{DD} = 3V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, f_{IN} = 100 kHz unless otherwise stated.

ADCS7476

ADCS7476 DNL

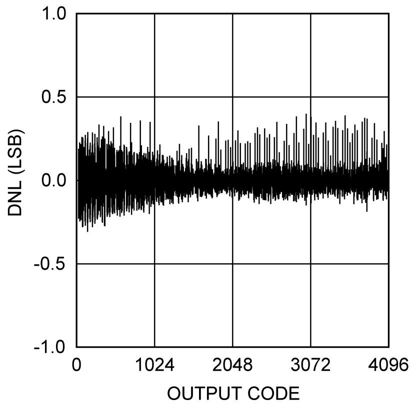


Figure 6.

ADCS7476 INL

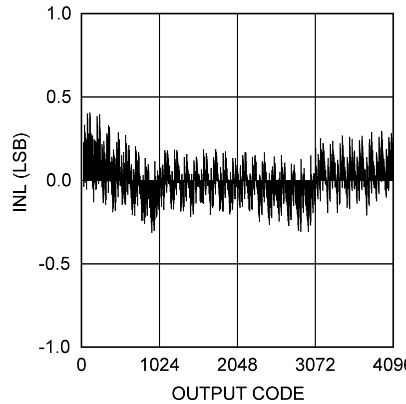


Figure 7.

ADCS7476 Spectral Response @ 100kHz Input

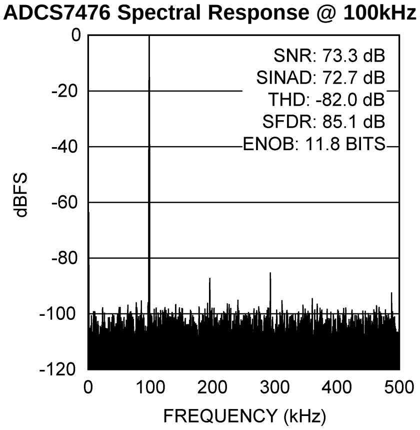


Figure 8.

ADCS7476 THD vs. Source Impedance

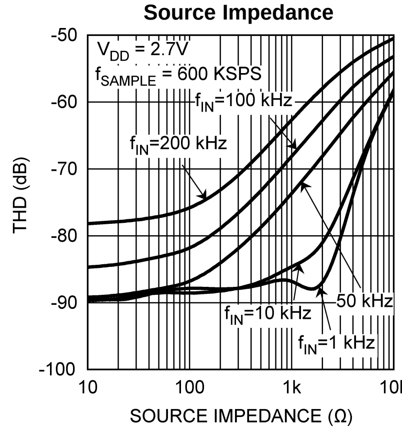


Figure 9.

ADCS7476 THD vs. Input Frequency, 600 kSPS

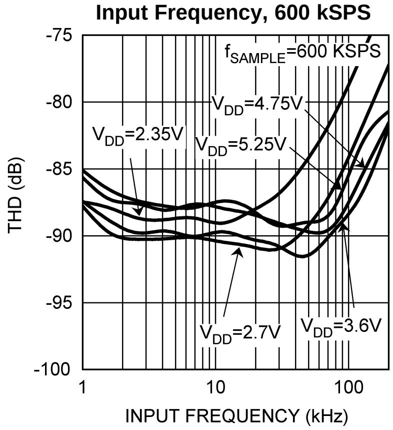


Figure 10.

ADCS7476 THD vs. Input Frequency, 1 MSPS

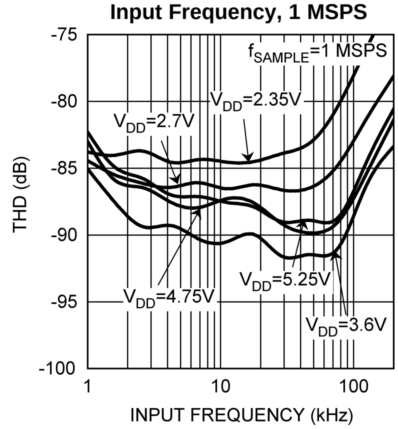


Figure 11.

Typical Performance Characteristics (continued)

T_A = +25°C, V_{DD} = 3V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, f_{IN} = 100 kHz unless otherwise stated.

ADCS7476

ADCS7476 SINAD vs. Input Frequency, 600 kSPS

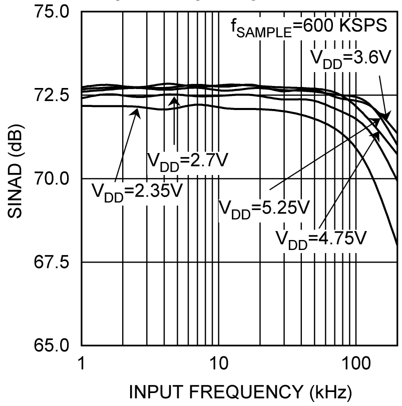


Figure 12.

ADCS7476 SINAD vs. Input Frequency, 1 MSPS

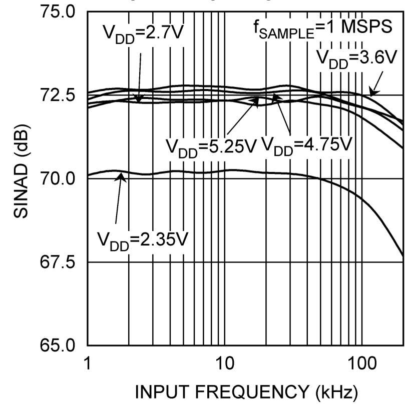


Figure 13.

ADCS7476 SNR vs. f_{SCLK}

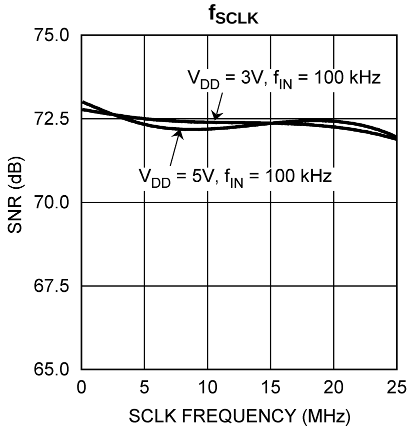


Figure 14.

ADCS7476 SINAD vs. f_{SCLK}

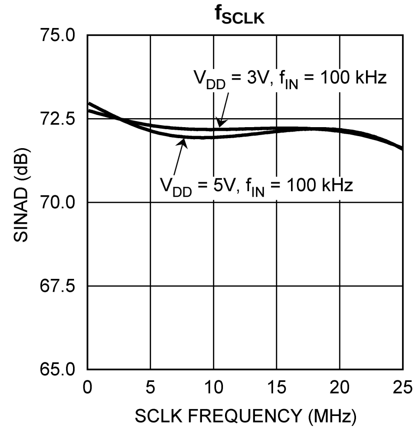


Figure 15.

ADCS7477 DNL

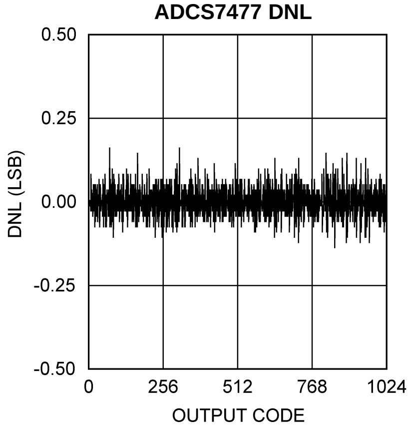


Figure 16.

ADCS7477 INL

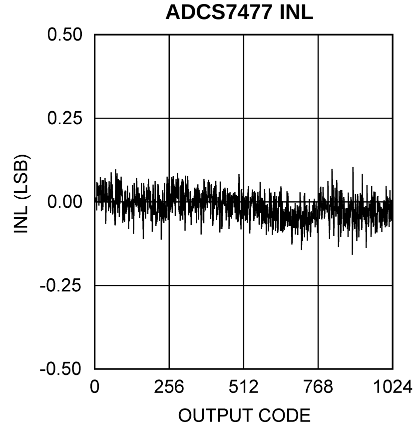


Figure 17.

Typical Performance Characteristics (continued)

T_A = +25°C, V_{DD} = 3V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, f_{IN} = 100 kHz unless otherwise stated.

ADCS7476

ADCS7477 Spectral Response @ 100kHz Input

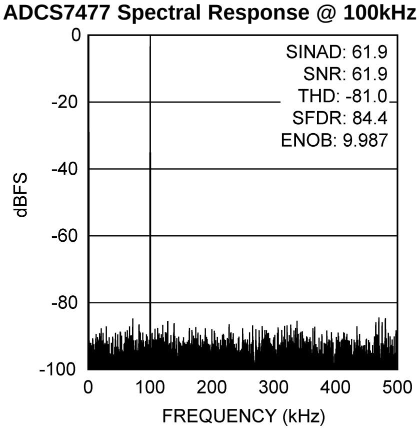


Figure 18.

ADCS7477 SNR vs. f_{SCLK}

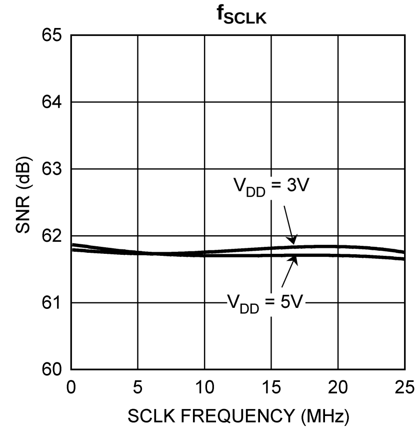


Figure 19.

ADCS7477 SINAD vs. f_{SCLK}

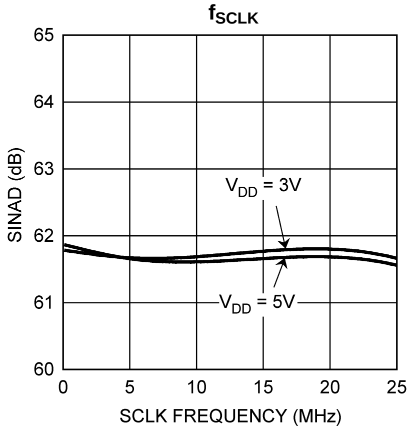


Figure 20.

ADCS7478 DNL

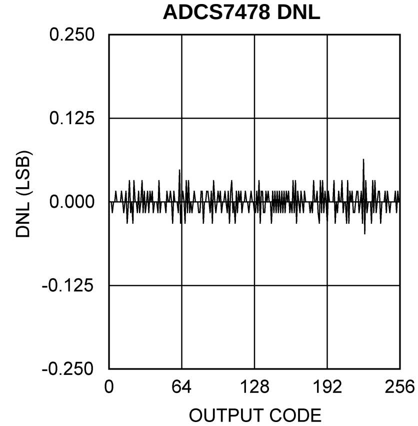


Figure 21.

ADCS7478 INL

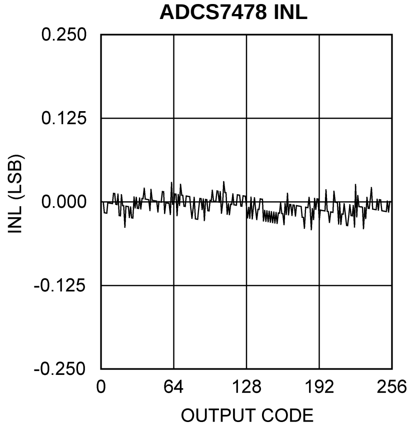


Figure 22.

ADCS7478 Spectral Response @ 100kHz Input

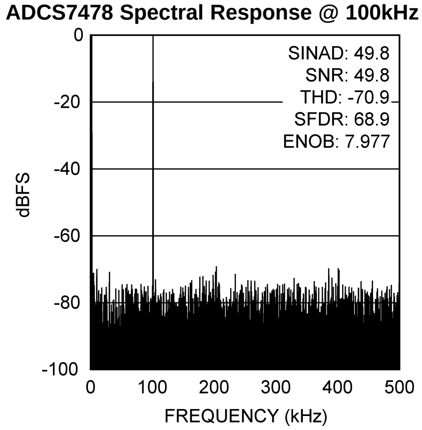


Figure 23.

Typical Performance Characteristics (continued)

T_A = +25°C, V_{DD} = 3V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, f_{IN} = 100 kHz unless otherwise stated.

ADCS7476

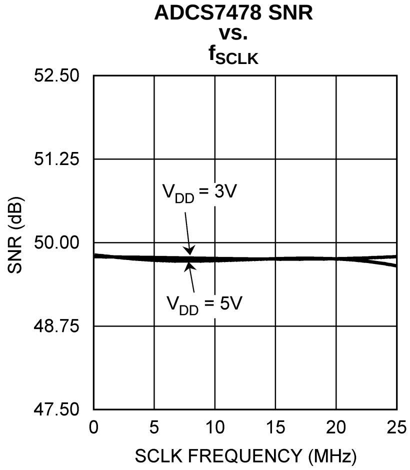


Figure 24.

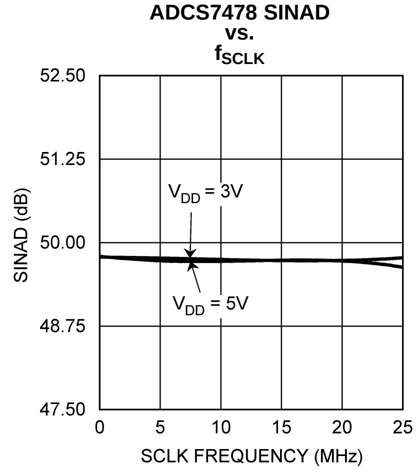


Figure 25.

APPLICATIONS INFORMATION

ADCS7476/77/78 OPERATION

The ADCS7476/77/78 are successive-approximation analog-to-digital converters designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the ADCS7476/77/78 in both track and hold operation are shown in Figure 26 and Figure 27, respectively. In Figure 26 the device is in track mode: switch SW1 connects the sampling capacitor to the input, and SW2 balances the comparator inputs. The device is in this state until $\overline{CS}$ is brought low, at which point the device moves to hold mode.

Figure 27 shows the device in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode on the 13th rising edge of SCLK.

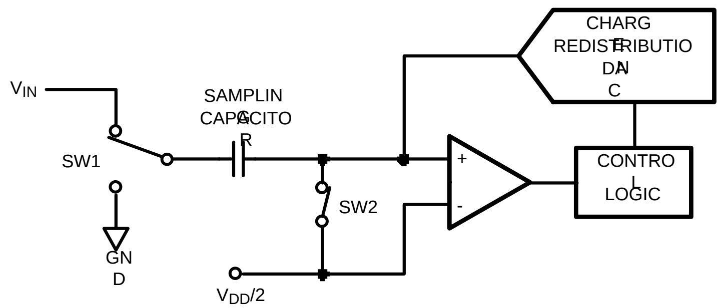


Figure 26. ADCS7476/77/78 in Track Mode

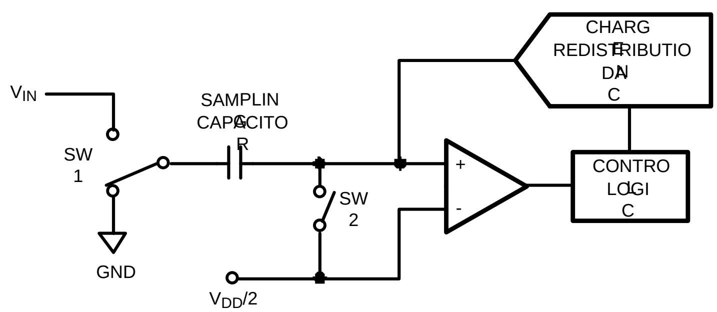


Figure 27. ADCS7476/77/78 in Hold Mode

USING THE ADCS7476/77/78

Serial interface timing diagrams for the ADCS7476/77/78 are shown in Figure 3, Figure 4, and Figure 5. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found.

Basic operation of the ADCS7476/77/78 begins with $\overline{CS}$ going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK will be labeled with reference to the falling edge of $\overline{CS}$; for example, "the third falling edge of SCLK" shall refer to the third falling edge of SCLK after $\overline{CS}$ goes low.

At the fall of $\overline{CS}$, the SDATA pin comes out of TRI-STATE, and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion at the falling edge of $\overline{CS}$. The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see Figure 3, Figure 4, or Figure 5). The SDATA pin will be placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of $\overline{CS}$, whichever occurs first. After a conversion is completed, the quiet time t_{QUIET} must be satisfied before bringing $\overline{CS}$ low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the ADCS7476/77/78. The sample bits (including any leading or trailing zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent falling edges of SCLK. The ADCS7476/77/78 will produce four leading zeroes on SDATA, followed by twelve, ten, or eight data bits, most significant first. After the data bits, the ADCS7477 will clock out two trailing zeros, and the ADCS7478 will clock out four trailing zeros. The ADCS7476 will not clock out any trailing zeros; the least significant data bit will be valid on the 16th falling edge of SCLK.

Depending upon the application, the first edge on SCLK after $\overline{CS}$ goes low may be either a falling edge or a rising edge. If the first SCLK edge after $\overline{CS}$ goes low is a rising edge, all four leading zeroes will be valid on the first four falling edges of SCLK. If instead the first SCLK edge after $\overline{CS}$ goes low is a falling edge, the first leading zero may not be set up in time for a microprocessor or DSP to read it correctly. The remaining data bits are still clocked out on the falling edges of SCLK.

ADCS7476/77/78 TRANSFER FUNCTION

The output format of the ADCS7476/77/78 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB widths for the ADCS7476 is V_{DD} / 4096; for the ADCS7477 the LSB width is V_{DD} / 1024; for the ADCS7478, the LSB width is V_{DD} / 256. The ideal transfer characteristic for the ADCS7476 and ADCS7477 is shown in Figure 28, while the ideal transfer characteristic for the ADCS7478 is shown in Figure 29.

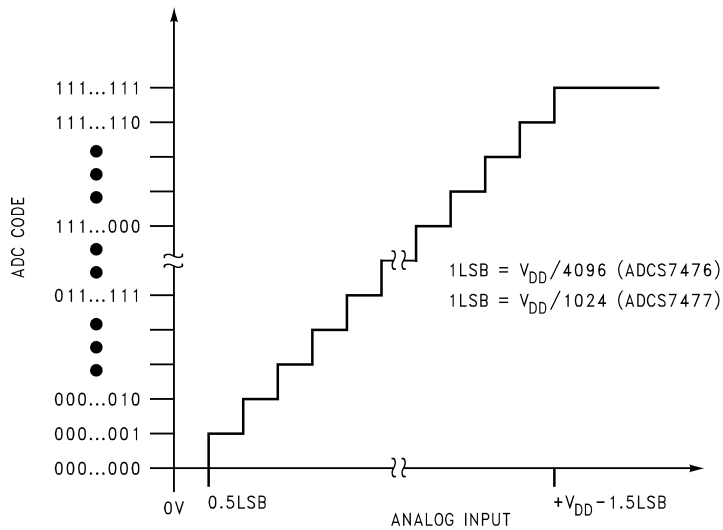


Figure 28. ADCS7476/77 Ideal Transfer Characteristic

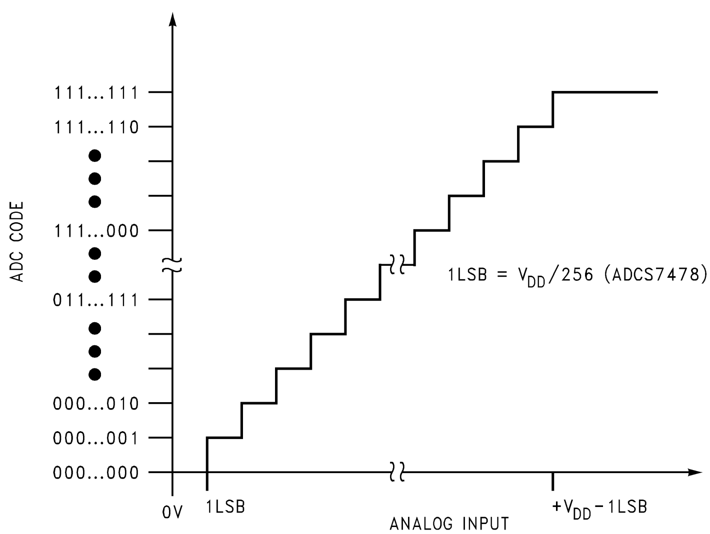


Figure 29. ADCS7478 Ideal Transfer Characteristic

TYPICAL APPLICATION CIRCUIT

A typical application of the ADCS7476/77/78 is shown in Figure 30. The combined analog and digital supplies are provided in this example by the National LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The supply is bypassed with a capacitor network located close to the device. The three-wire interface is also shown connected to a microprocessor or DSP.

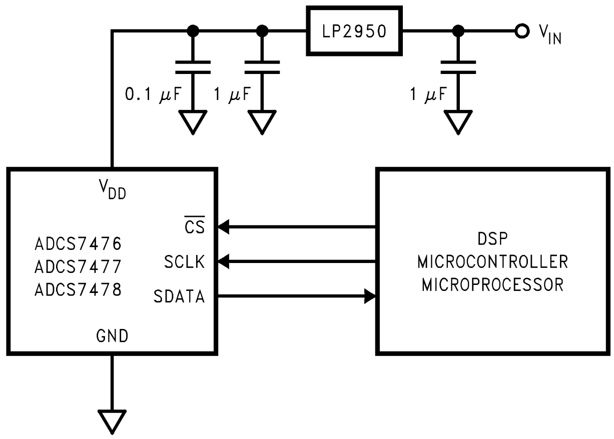


Figure 30. Typical Application Circuit

ANALOG INPUTS

An equivalent circuit for the ADCS7476/77/78 input channel is shown in Figure 31. The diodes D1 and D2 provide ESD protection for the analog inputs. At no time should an analog input exceed V_{DD} + 300 mV or GND - 300 mV, as these ESD diodes will begin conducting current into the substrate or supply line and affect ADC operation.

The capacitor C1 in Figure 31 typically has a value of 4 pF, and is mainly due to pin capacitance. The resistor R1 represents the on resistance of the multiplexer and track / hold switch, and is typically 100 ohms. The capacitor C2 is the ADCS7476/77/78 sampling capacitor, and is typically 26 pF.

The sampling nature of the analog input causes input current pulses that result in voltage spikes at the input. The ADCS7476/77/78 will deliver best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. In applications where dynamic performance is critical, the input might need to be driven with a low output-impedance amplifier. In addition, when using the ADCS7476/77/78 to sample AC signals, a band-pass or low-pass filter will reduce harmonics and noise and thus improve THD and SNR.

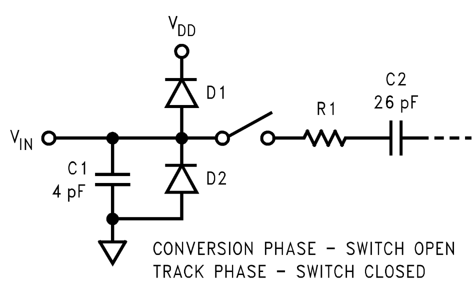


Figure 31. Equivalent Input Circuit

DIGITAL INPUTS AND OUTPUTS

The ADCS7476/77/78 digital inputs (SCLK and $\overline{CS}$) are not limited by the same absolute maximum ratings as the analog inputs. The digital input pins are instead limited to +6.5V with respect to GND, regardless of V_{DD}, the supply voltage. This allows the ADCS7476/77/78 to be interfaced with a wide range of logic levels, independent of the supply voltage.

Note that, even though the digital inputs are tolerant of up to +6.5V above GND, the digital outputs are only capable of driving V_{DD} out. In addition, the digital input pins are not prone to latch-up; SCLK and $\overline{CS}$ may be asserted before V_{DD} without any risk.

MODES OF OPERATION

The ADCS7476/77/78 has two possible modes of operation: NORMAL MODE, and SHUTDOWN MODE. The ADCS7476/77/78 enters normal mode (and a conversion process is begun) when $\overline{CS}$ is pulled low. The device will enter shutdown mode if $\overline{CS}$ is pulled high before the tenth falling edge of SCLK after $\overline{CS}$ is pulled low, or will stay in normal mode if $\overline{CS}$ remains low. Once in shutdown mode, the device will stay there until $\overline{CS}$ is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade-off throughput for power consumption.

NORMAL MODE

The best possible throughput is obtained by leaving the ADCS7476/77/78 in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

If $\overline{CS}$ is brought high after the 10th falling edge, but before the 16th falling edge, the device will remain in normal mode, but the current conversion will be aborted, and SDATA will return to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed, $\overline{CS}$ may be idled either high or low until the next conversion. If $\overline{CS}$ is idled low, it must be brought high again before the start of the next conversion, which begins when $\overline{CS}$ is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after t_{QUIET} has elapsed, by bringing $\overline{CS}$ low again.

SHUTDOWN MODE

Shutdown mode is appropriate for applications that either do not sample continuously, or are willing to trade throughput for power consumption. When the ADCS7476/77/78 is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing $\overline{CS}$ back high anytime between the second and tenth falling edges of SCLK, as shown in Figure 32. Once $\overline{CS}$ has been brought high in this manner, the device will enter shutdown mode; the current conversion will be aborted and SDATA will enter TRI-STATE. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the device will not change mode; this is to avoid accidentally changing mode as a result of noise on the $\overline{CS}$ line.

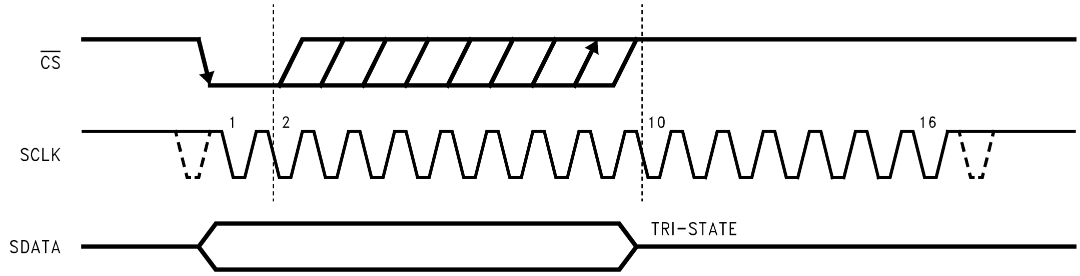


Figure 32. Entering Shutdown Mode

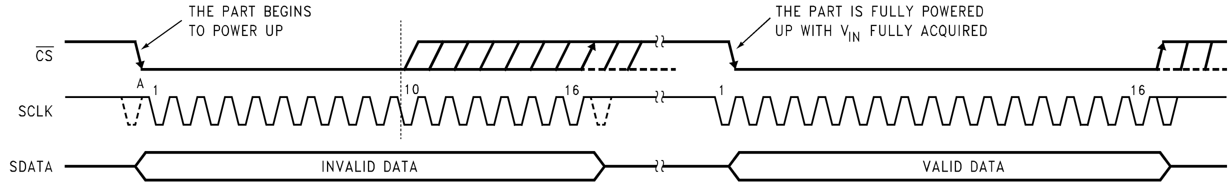


Figure 33. Entering Normal Mode

EXITING SHUTDOWN MODE

To exit shutdown mode, bring $\overline{CS}$ back low. Upon bringing $\overline{CS}$ low, the ADCS7476/77/78 will begin powering up. Power up typically takes 1 µs. This microsecond of power-up delay results in the first conversion result being unusable. The second conversion performed after power-up, however, is valid, as shown in Figure 33.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device will return to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit shutdown mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK. The ADCS7476/77/78 will be fully powered-up after 16 SCLK cycles.

POWER-UP TIMING

The ADCS7476/77/78 typically requires 1 µs to power up, either after first applying V_{DD}, or after returning to normal mode from shutdown mode. This corresponds to one "dummy" conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the ADCS7476/77/78 will perform conversions properly. Note that the t_{QUIET} time must still be included between the first dummy conversion and the second valid conversion.

STARTUP MODE

When the V_{DD} supply is first applied, the ADCS7476/77/78 may power up in either of the two modes: normal or shutdown. As such, one dummy conversion should be performed after start-up, exactly as described in POWER-UP TIMING. The part may then be placed into either normal mode or the shutdown mode, as described in NORMAL MODE and SHUTDOWN MODE.

POWER CONSIDERATIONS

There are three concerns relating to the power supply of these products: the effects of Power Supply Noise upon the conversion process, the Digital Output Effect Upon Noise upon the conversion process and Power Management of the product.

Power Supply Noise

Since the reference voltage of the ADCS7476/77/78 is the reference voltage, any noise greater than 1/2 LSB in amplitude will have some effect upon the converter noise performance. This effect is proportional to the input voltage level. The power supply should receive all the considerations of a reference voltage as far as stability and noise is concerned. Using the same supply voltage for these devices as is used for digital components will lead to degraded noise performance.

Digital Output Effect Upon Noise

The charging of any output load capacitance requires current from the digital supply, V_{DD}. The current pulses required from the supply to charge the output capacitance will cause voltage variations at the ADC supply line. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, causing "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the device power supply line and die substrate and the greater is the noise coupled into the analog path.

The first solution to keeping digital noise out of the power supply is to decouple the supply from any other components or use a separate supply for the ADC. To keep noise out of the supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100 Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve noise performance. Since the series resistor and the load capacitance form a low frequency pole, verify signal integrity once the series resistor has been added.

Power Management

When the ADCS7476/77/78 is operated continuously in normal mode, throughput up to 1 MSPS can be achieved. The user may trade throughput for power consumption by simply performing fewer conversions per unit time, and putting the ADCS7476/77/78 into shutdown mode between conversions. This method is not advantageous beyond 350 kSPS throughput.

A plot of maximum power consumption versus throughput is shown in Figure 34. To calculate the power consumption for a given throughput, remember that each time the part exits shutdown mode and enters normal mode, one dummy conversion is required. Generally, the user will put the part into normal mode, execute one dummy conversion followed by one valid conversion, and then put the part back into shutdown mode. When this is done, the fraction of time spent in normal mode may be calculated by multiplying the throughput (in samples per second) by 2 µs, the time taken to perform one dummy and one valid conversion. The power consumption can then be found by multiplying the fraction of time spent in normal mode by the normal mode power consumption figure. The power dissipated while the part is in shutdown mode is negligible.

For example, to calculate the power consumption at 300 kSPS with V_{DD} = 5V, begin by calculating the fraction of time spent in normal mode: 300,000 samples/second x 2 µs = 0.6, or 60%. The power consumption at 300 kSPS is then 60% of 17.5 mW (the maximum power consumption at V_{DD} = 5V) or 10.5 mW.

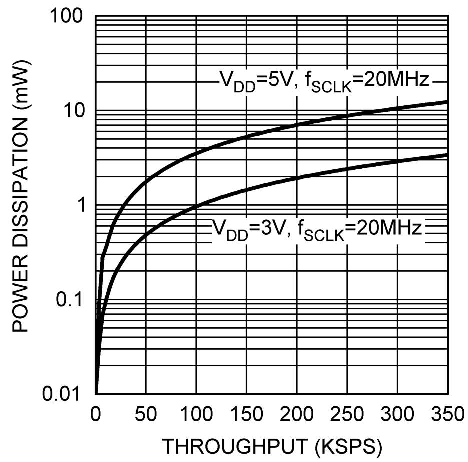


Figure 34. Maximum Power Consumption vs. Throughput

LAYOUT AND GROUNDING

Capacitive coupling between noisy digital circuitry and sensitive analog circuitry can lead to poor performance. The solution is to keep the analog and digital circuitry separated from each other and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. This digital noise could have significant impact upon system noise performance. To avoid performance degradation of the ADCS7476/77/78 due to supply noise, do not use the same supply for the ADCS7476/77/78 that is used for digital logic.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated.

The analog input should be isolated from noisy signal lines to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

We recommend the use of a single, uniform ground plane and the use of split power planes. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground should be connected together with short traces and enter the analog ground plane at a single, quiet point.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADCS7476AIMF	ACTIVE	SOT-23	DBV	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	X01A	Samples
ADCS7476AIMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X01A	Samples
ADCS7476AIMFE/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X01A	Samples
ADCS7476AIMFX	ACTIVE	SOT-23	DBV	6	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 125	X01A	Samples
ADCS7476AIMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X01A	Samples
ADCS7477AIMF	ACTIVE	SOT-23	DBV	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	X02A	Samples
ADCS7477AIMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	X02A	Samples
ADCS7477AIMFE/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	X02A	Samples
ADCS7477AIMFX	ACTIVE	SOT-23	DBV	6	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	X02A	Samples
ADCS7477AIMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	X02A	Samples
ADCS7478AIMF	ACTIVE	SOT-23	DBV	6	1000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	X03A	Samples
ADCS7478AIMF/NOPB	ACTIVE	SOT-23	DBV	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	X03A	Samples
ADCS7478AIMFE/NOPB	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	X03A	Samples
ADCS7478AIMFX	ACTIVE	SOT-23	DBV	6	3000	TBD	CU SNPB	Level-1-260C-UNLIM	-40 to 85	X03A	Samples
ADCS7478AIMFX/NOPB	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	X03A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Only one of markings shown within the brackets will appear on the physical device.

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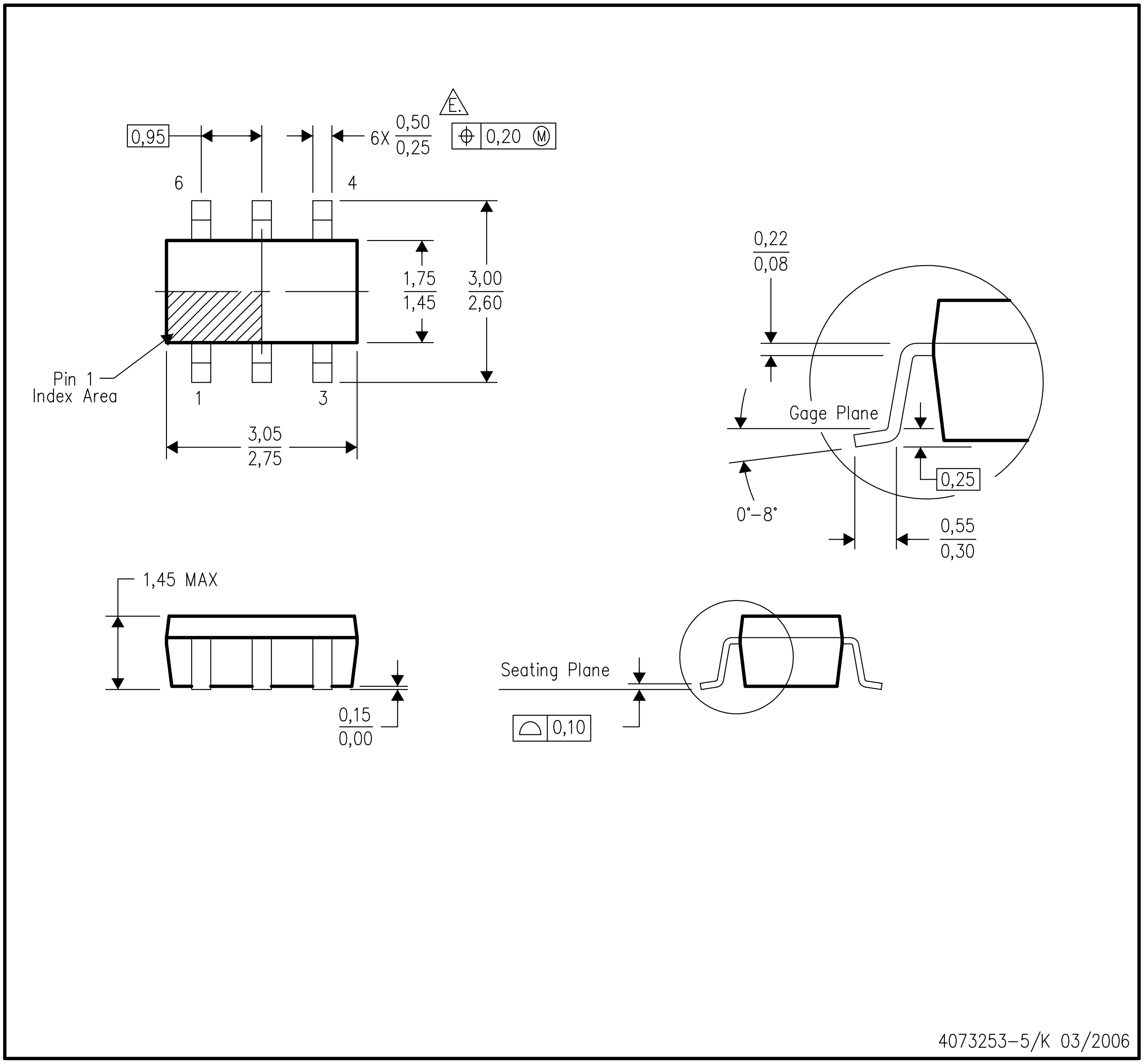
DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.