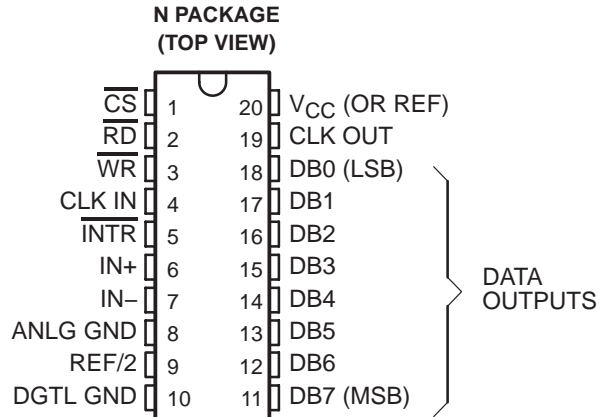


# ADC0804C, ADC0804I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH DIFFERENTIAL INPUTS

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- 8-Bit Resolution
- Ratiometric Conversion
- 100- $\mu$ s Conversion Time
- 135-ns Access Time
- No Zero Adjust Requirement
- On-Chip Clock Generator
- Single 5-V Power Supply
- Operates With Microprocessor or as Stand-Alone
- Designed to Be interchangeable With National Semiconductor and Signetics ADC0804



## description

The ADC0804 is a CMOS 8-bit successive-approximation analog-to-digital converter that uses a modified potentiometric (256R) ladder. The ADC0804 is designed to operate from common microprocessor control buses, with the 3-state output latches driving the data bus. The ADC0804 can be made to appear to the microprocessor as a memory location or an I/O port. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although REF/2 is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with REF/2 open. Without an external reference, the conversion takes place over a span from  $V_{CC}$  to ANLG GND. The ADC0804 can operate with an external clock signal or, with an additional resistor and capacitor, can operate using an on-chip clock generator.

The ADC0804C is characterized for operation from 0°C to 70°C. The ADC0804I is characterized for operation from -40°C to 85°C.

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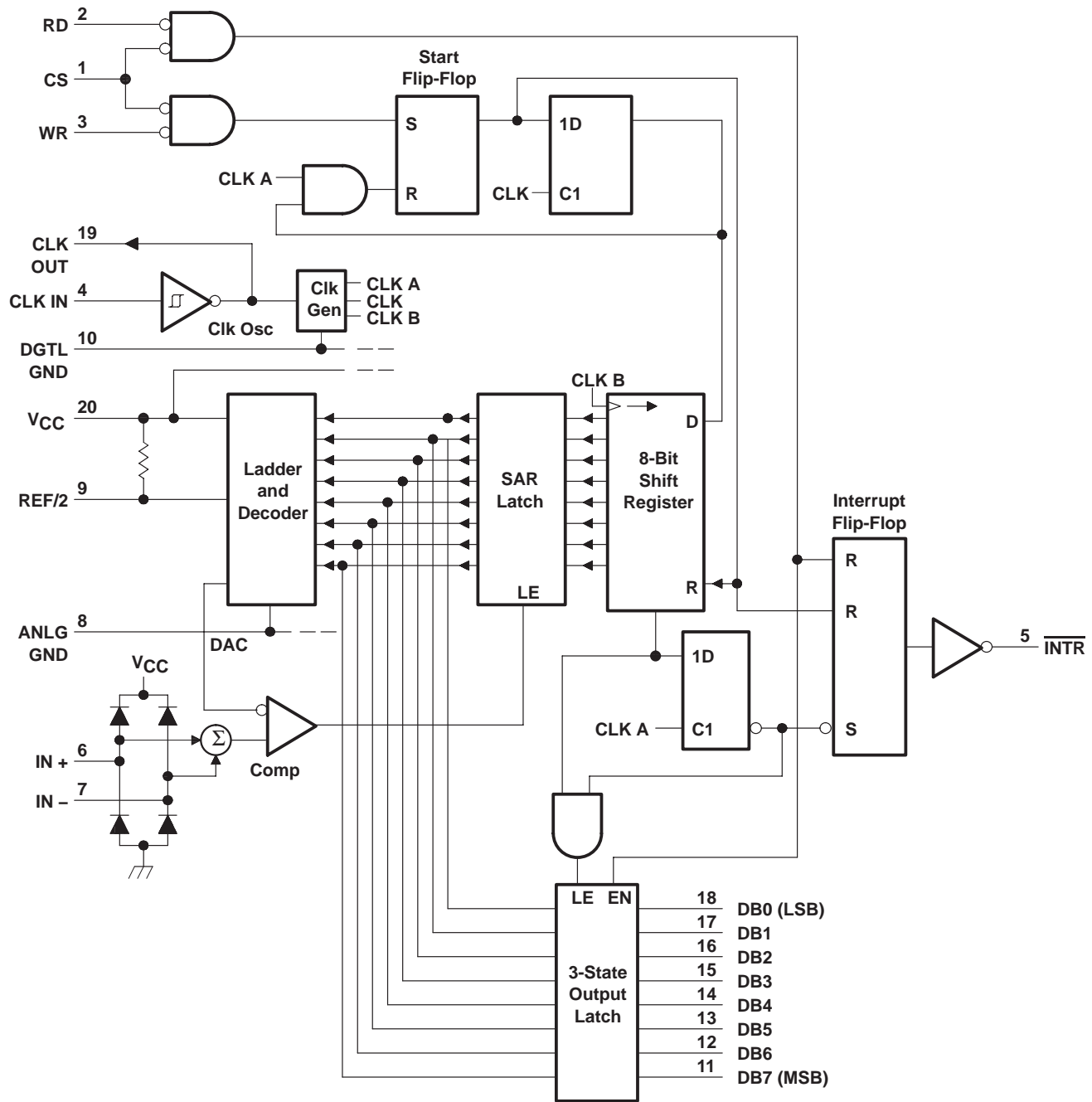
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# ADC0804C, ADC08041

## 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH DIFFERENTIAL INPUTS

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### functional block diagram (positive logic)



# ADC0804C, ADC0804I 8-BIT ANALOG-TO-DIGITAL CONVERTERS WITH DIFFERENTIAL INPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	6.5 V
Input voltage range: $\overline{CS}$ , $\overline{RD}$ , $\overline{WR}$	–0.3 V to 18 V
Other inputs	–0.3 V to $V_{CC} + 0.3$ V
Output voltage range	–0.3 V to $V_{CC} + 0.3$ V
Operating free-air temperature range: ADC0804C	0°C to 70°C
ADC0804I	–40°C to 85°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect DGTL GND with DGTL GND and ANLG GND connected together (unless otherwise noted.)

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.5	5	6.3	V
Voltage at REF/2, $V_{REF/2}$ (see Note 2),	0.25	2.5		V
High-level input voltage at $\overline{CS}$ , $\overline{RD}$ , or $\overline{WR}$ , $V_{IH}$	2		15	V
Low-level input voltage at $\overline{CS}$ , $\overline{RD}$ , or $\overline{WR}$ , $V_{IL}$			0.8	V
Analog ground voltage (see Note 3)	–0.05	0	1	V
Analog input voltage (see Note 4)	–0.05		$V_{CC} + 0.05$	V
Clock input frequency, $f_{clock}$ (see Note 5)	100	640	1460	kHz
Duty cycle for $f_{clock} \geq 640$ kHz (see Note 5)	40		60	%
Pulse duration, clock input (high or low) for $f_{clock} < 640$ kHz, $t_W(\text{CLK})$ (see Note 5)	275	781		ns
Pulse duration, $\overline{WR}$ input low, (start conversion), $t_W(\overline{WR})$	100			ns
Operating free-air temperature, $T_A$	ADC0804C		70	°C
	ADC0804I		85	

- NOTES: 2. The internal reference voltage is equal to the voltage applied to REF/2 or approximately equal to one-half of the  $V_{CC}$  when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage range when REF/2 is open and  $V_{CC} = 5$  V is 0 V to 5 V.  $V_{REF/2}$  for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.
3. These values are with respect to DGTL GND.
4. When the differential input voltage ( $V_{I+} - V_{I-}$ ) is less than or equal to 0 V, the output code is 0000 0000.
5. Total unadjusted error is specified only at an  $f_{clock}$  of 640 kHz with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an  $f_{clock}$  greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided  $t_W(\text{CLK})$  remains within limits.



# ADC0804C, ADC08041

## 8-BIT ANALOG-TO-DIGITAL CONVERTERS

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electrical characteristics over recommended range of operating free-air temperature,  $V_{CC} = 5\text{ V}$ ,  $f_{\text{clock}} = 640\text{ kHz}$ ,  $V_{\text{REF}/2} = 2.5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	All outputs	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -360\text{ }\mu\text{A}$	2.4			V
		DB and $\overline{\text{INTR}}$	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -10\text{ }\mu\text{A}$	4.5			
V <sub>OL</sub>	Low-level output voltage	Data outputs	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 1.6\text{ mA}$			0.4	V
		$\overline{\text{INTR}}$ output	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 1\text{ mA}$			0.4	
		CLK OUT	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 360\text{ }\mu\text{A}$			0.4	
V <sub>T+</sub>	Clock positive-going threshold voltage			2.7	3.1	3.5	V
V <sub>T-</sub>	Clock negative-going threshold voltage			1.5	1.8	2.1	V
V <sub>T+</sub> - V <sub>T-</sub>	Clock input hysteresis			0.6	1.3	2	V
I <sub>IH</sub>	High-level input current				0.005	1	$\mu\text{A}$
I <sub>IL</sub>	Low-level input current				-0.005	-1	$\mu\text{A}$
I <sub>OZ</sub>	Off-state output current		$V_O = 0$			-3	$\mu\text{A}$
			$V_O = 5\text{ V}$			3	
I <sub>OHS</sub>	Short-current output current	Output high	$V_O = 0$ , $T_A = 25^\circ\text{C}$	-4.5	-6		mA
I <sub>OLS</sub>	Short-circuit output current	Output low	$V_O = 5\text{ V}$ , $T_A = 25^\circ\text{C}$	9	16		mA
I <sub>CC</sub>	Supply current plus reference current		$V_{\text{REF}/2} = \text{open}$ , $T_A = 25^\circ\text{C}$ , $\overline{\text{CS}} = 5\text{ V}$		1.9	2.5	mA
R <sub>REF/2</sub>	Input resistance to reference ladder		See Note 6	1	1.3		k $\Omega$
C <sub>i</sub>	Input capacitance (control)				5	7.5	pF
C <sub>o</sub>	Output capacitance (DB)				5	7.5	pF

operating characteristics over recommended operating free-air temperature,  $V_{CC} = 5\text{ V}$ ,  $V_{\text{REF}/2} = 2.5\text{ V}$ ,  $f_{\text{clock}} = 640\text{ kHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error (see Notes 2 and 7)		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		$\pm 1/16$	$\pm 1/8$	LSB
	Total unadjusted error (see Notes 7 and 8)		$V_{\text{REF}/2} = 2.5\text{ V}$			$\pm 1$	LSB
	DC common-mode error (see Note 8)				$\pm 1/16$	$\pm 1/8$	LSB
t <sub>en</sub>	Output enable time		$C_L = 100\text{ pF}$		135	200	ns
t <sub>dis</sub>	Output disable time		$C_L = 10\text{ pF}$ , $R_L = 10\text{ k}\Omega$		125	200	ns
t <sub>d</sub> ( $\overline{\text{INTR}}$ )	Delay time to reset $\overline{\text{INTR}}$				300	450	nx
t <sub>conv</sub>	Conversion cycle time (see Note 9)		$f_{\text{clock}} = 100\text{ kHz to }1.46\text{ MHz}$	65 1/2		72 1/2	clock cycles
	Conversion time			103		114	$\mu\text{s}$
CR	Free-running conversion rate		$\overline{\text{INTR}}$ connected to $\overline{\text{WR}}$ , $\overline{\text{CS}}$ at 0 V			8827	conv/s

† All typical values are at  $T_A = 25^\circ\text{C}$ .

NOTES: 2. The internal reference voltage is equal to the voltage applied to REF/2 or approximately equal to one-half of the  $V_{CC}$  when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage when REF/2 is open and  $V_{CC} = 5\text{ V}$  is 0 to 5 V.  $V_{\text{REF}/2}$  for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.

6. The resistance is calculated from the current drawn from a 5-V supply applied to ANLG GND and REF/2.

7. These parameters are specified for the recommended analog input voltage range.

8. All errors are measured with reference to an ideal straight line through the end points of the analog-to-digital transfer characteristic.

9. Although internal conversion is completed in 64 clock periods, a  $\overline{\text{CS}}$  or  $\overline{\text{WR}}$  low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is completed, part of another clock period is required before a high-to-low transition of  $\overline{\text{INTR}}$  completes the cycle.



PARAMETER MEASUREMENT INFORMATION

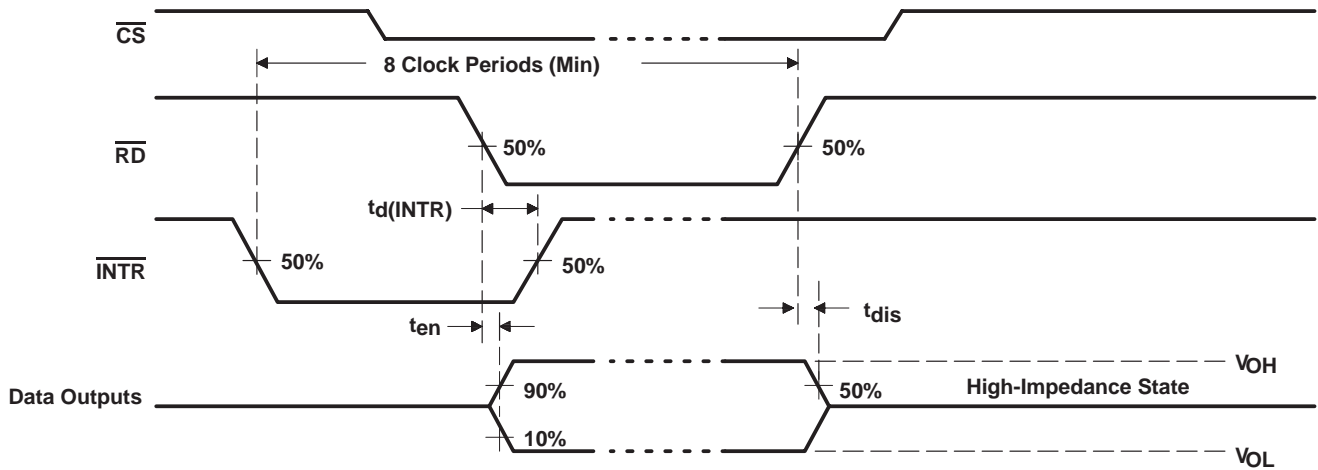


Figure 1. Read Operation Timing Diagram

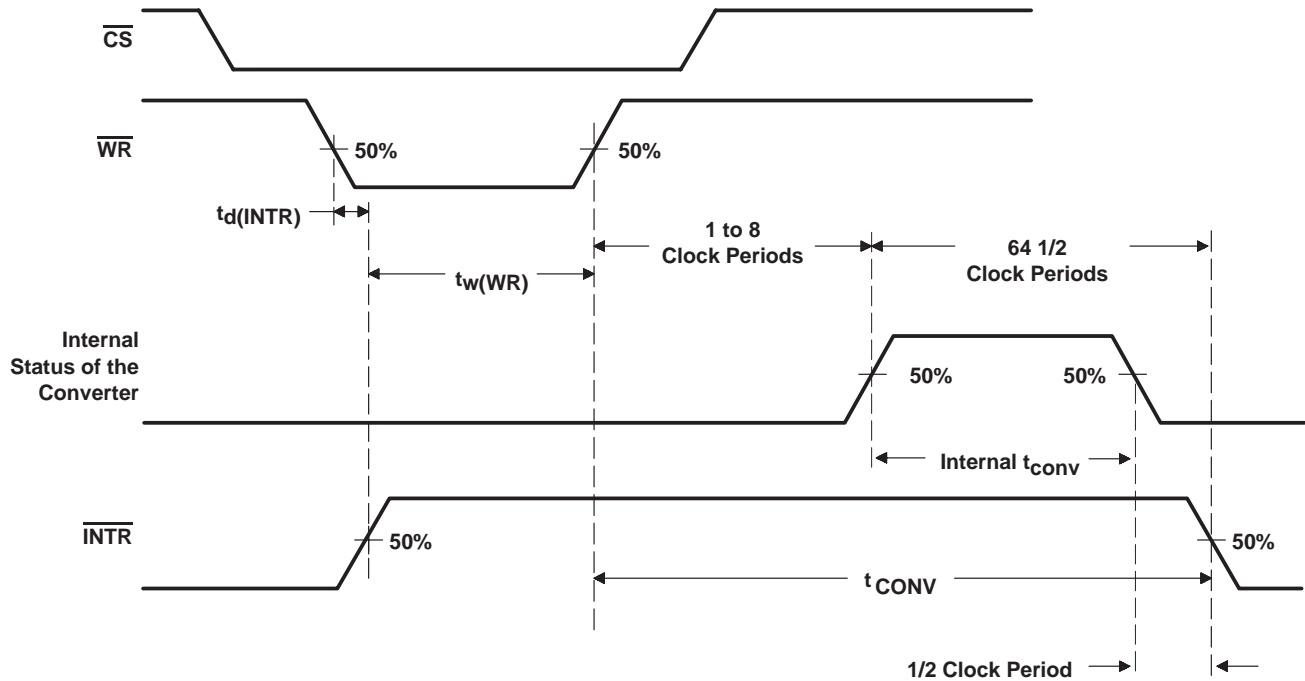


Figure 2. Write Operation Timing Diagram

# ADC0804C, ADC08041

## 8-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH DIFFERENTIAL INPUTS

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#### PRINCIPLES OF OPERATION

The ADC0804 contains a circuit equivalent to a 256-resistor network. Analog switches are sequenced by successive-approximation logic to match an analog differential input voltage ( $V_{I+} - V_{I-}$ ) to a corresponding tap on the 256-resistor network. The most significant bit (MSB) is tested first. After eight comparisons (64 clock periods), an 8-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ( $\overline{\text{INTR}}$ ) output goes low. The device can be operated in a free-running mode by connecting the  $\overline{\text{INTR}}$  output to the write ( $\overline{\text{WR}}$ ) input and holding the conversion start ( $\overline{\text{CS}}$ ) input at a low level. To ensure startup under all conditions, a low-level  $\overline{\text{WR}}$  input is required during the power-up cycle. Taking  $\overline{\text{CS}}$  low anytime after that will interrupt a conversion in process.

When  $\overline{\text{WR}}$  goes low, the ADC0804 successive-approximation register (SAR) and 8-bit shift register are reset. As long as both  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  remain low, the ADC0804 remains in a reset state. One to eight clock periods after  $\overline{\text{CS}}$  or  $\overline{\text{WR}}$  makes a low-to-high transition, conversion starts.

When  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  are low, the start flip-flop is set and the interrupt flip-flop and 8-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse, placing a logic high on the reset input of the start flip-flop. If either  $\overline{\text{CS}}$  or  $\overline{\text{WR}}$  have gone high, the set signal to the start flip-flop is removed, causing it to be reset. A logic high is placed on the D input of the 8-bit shift register and the conversion process is started. If  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  are still low, the start flip-flop, the 8-bit shift register, and the SAR remain reset. This action allows for wide  $\overline{\text{CS}}$  and  $\overline{\text{WR}}$  inputs with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the 8-bit shift register, completing the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the 3-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an  $\overline{\text{INTR}}$  output that is high during conversion and low when the conversion is completed.

When a low is at both  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$ , an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either the  $\overline{\text{CS}}$  or  $\overline{\text{RD}}$  inputs return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.



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