Quad 8-Bit, 65 MSPS Serial LVDS 3V A/D Converter

Preliminary Technical Data — AD9289

FEATURES

- Four ADCs in one package
- Serial LVDS digital output data rates up to 520 MHz (ANSI-644)
- Data clock output provided
- SNR = 47 dB (to Nyquist)
- Excellent Linearity:
  - DNL = ±0.25 LSB (Typical)
  - INL = ±0.5 LSB (Typical)
- 400 MHz full power analog bandwidth
- Power dissipation = 330 mW at 65 MSPS
- 1 Vpp – 2 Vpp input voltage range
- +3.0 V supply operation
- Power down mode

APPLICATIONS

- Tape drives
- Medical imaging

FUNCTIONAL BLOCK DIAGRAM

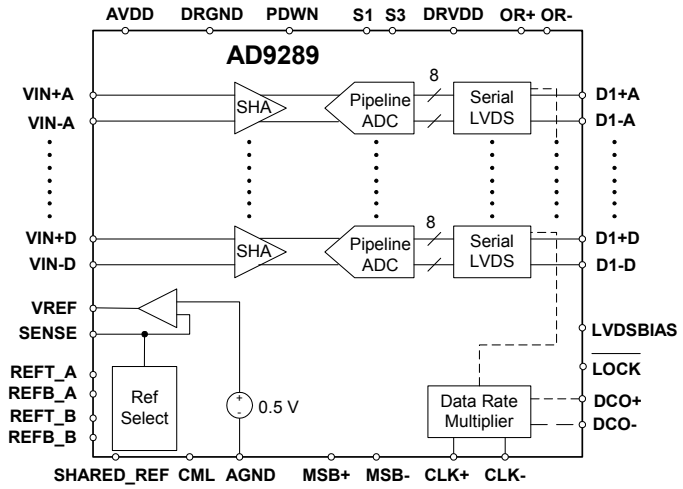

Figure 1. Functional Block Diagram

PRODUCT DESCRIPTION

The AD9289 is a quad 8-bit, 65 MSPS analog–to–digital converter with an on–chip track–and–hold circuit and is designed for low cost, low power, small size and ease of use. The product operates up to 65 MSPS conversion rate and is optimized for outstanding dynamic performance where a small package size is critical.

The ADC requires a single+3V power supply and LVDS, TTL, or PECL-compatible sample rate clock for full performance operation. No external reference or driver components are required for many applications. A separate output power supply pin supports LVDS compatible serial digital output levels.

The ADC automatically multiplies up the sample rate clock for the appropriate LVDS serial data rate. An MSB trigger is provided to signal a new output byte. Power down is supported, and the ADC consumes less than 10mW when enabled.

Fabricated on an advanced CMOS process, the AD9289 is available in a 64-ball mini-BGA package (64 CSP_BGA) specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Four analog-to-digital converters are contained in one small, space saving package.
2. A Data Clock Out (DCO) is provided which operates up to 260 MHz.
3. The outputs of each ADC are serialized and provided on the rising and falling edge of DCO (rising edge only is also an option). Output data rates up to 520 MHz (8 bits x 65 MSPS) are available.
4. The AD9289 operates from a single 3V power supply.

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AD9289—SPECIFICATIONS[1]

AVDD = 3.0V, DRVDD = 3.0V; EXT REF; DIFFERENTIAL ANALOG AND CLOCK INPUTS

Parameter		Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION					8		Bits
ACCURACY	No Missing Codes	Full	VI		Guaranteed		
	Offset Matching	25°C	I		± 25		mV
	Gain Matching[2]	25°C	I		± 2		% FS
	Differential Nonlinearity (DNL)	25°C	I		± 0.25		LSB
		Full	VI				LSB
	Integral Nonlinearity (INL)	25°C	I		± 0.5		LSB
		Full	VI				LSB
TEMPERATURE DRIFT	Offset Error	Full	V		± 16		ppm/°C
	Gain Error[2]	Full	V		± 150		ppm/°C
	Reference	Full	V				ppm/°C
REFERENCE	Internal Reference Voltage	25°C	I		0.5		V
	Output Current	Full	V				uA
	Input Current	Full	V				uA
	Input Resistance	Full	V		7		kΩ
ANALOG INPUTS	Differential Input Voltage Range				1 –2		Vpp
	Common Mode Voltage	Full	V		1.5		V
	Input Resistance	Full	V		tbd		kΩ
	Input Capacitance	Full	V		5		pF
	Analog Bandwidth, Full Power	Full	V		400		MHz
POWER SUPPLY	AVDD	Full	IV	2.7	3.0	3.6	V
	DRVDD	Full	IV	2.7	3.0	3.6	V
	Power Dissipation[3]	Full	VI		330		mW
	Power Down Dissipation	Full	VI		<10		mW
	Power Supply Rejection Ratio (PSRR)	25°C	I				mV/V
	IAVDD[3]	Full	VI		110		mA
	DRVDD[3]	Full	VI		27		mA
CROSSTALK	Crosstalk	Full	V		70		dB

Table 1

[1] Specifications subject to change without notice
[2] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 0.5 V external reference and a 1 V p-p differential analog input).
[3] Power dissipation measured with rated encode and a dc analog input (Outputs Static, I_{VDD} = 0.). I_{VCC} and I_{VDD} measured with TBD MHz analog input @ 0.5dBFS.

DIGITAL SPECIFICATIONS

AVDD = 3.0V, DRVDD = 3.0V

Parameter		Temp	Test Level	Min	Typ	Max	Unit
DIGITAL INPUTS (CLK+, CLK-)	Differential Input	Full	IV	100	350		mV
	V_{IH}	Full	IV				V
	V_{IL}	Full	IV				V
	Input Resistance	Full	IV				kΩ
	Input Capacitance	25°C	IV				pF
LOGIC INPUTS	Logic '1' Voltage	Full	IV	2.0			V
	Logic '0' Voltage	Full	IV			0.8	V
	Input Resistance	Full	IV		30		kΩ
	Input Capacitance	Full	IV		4		PF
DIGITAL OUTPUTS (LVDS Mode)	Differential Output Voltage (V_{OD})	Full	IV	247		454	mV
	Output Offset Voltage (V_{OS})	Full	IV	1.125		1.375	V
	Output Coding	Full	IV	Twos Complement or Binary			

Table 2: Digital Specifications

AC SPECIFICATIONS[1]

AVDD = 3.0 V, DRVDD = 3.0 V; INTERNAL REF; DIFFERENTIAL ANALOG AND CLOCK INPUT, LVDS OUTPUT MODE

Parameter		Temp	Test Level	Min	Typ	Max	Unit
SIGNAL TO NOISE RATIO (SNR) – Without Harmonics	f_{IN}= 10.3 MHz	25°C	V		47.5		dB
	f_{IN}= 19.6 MHz	25°C	V				dB
	f_{IN}= 32.5 MHz	25°C	I		47.5		dB
	f_{IN}= 51 MHz	25°C	V				dB
SIGNAL TO NOISE RATIO (SINAD) – With Harmonics	f_{IN}= 10.3 MHz	25°C	V		47		dB
	f_{IN}= 19.6 MHz	25°C	V				dB
	f_{IN}= 32.5 MHz	25°C	I		47		dB
	f_{IN}= 51 MHz	25°C	V				dB
EFFECTIVE NUMBER OF BITS (ENOB)	f_{IN}= 10.3 MHz	25°C	V		7.5		Bits
	f_{IN}= 19.6 MHz	25°C	V				Bits
	f_{IN}= 32.5 MHz	25°C	I		7.5		Bits
	f_{IN}= 51 MHz	25°C	V				Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR)	f_{IN}= 10.3 MHz	25°C	V		62		dB
	f_{IN}= 19.6 MHz	25°C	V				dB
	f_{IN}= 32.5 MHz	25°C	I		59		dB
	f_{IN}= 51 MHz	25°C	V				dB
SECOND AND THIRD HARMONIC DISTORTION	f_{IN}= 10.3 MHz	25°C	V		62		dBc
	f_{IN}= 19.6 MHz	25°C	V				dBc
	f_{IN}= 32.5 MHz	25°C	I		59		dBc
	f_{IN}= 51 MHz	25°C	V				dBc
TOTAL HARMONIC DISTORTION (THD)	f_{IN}= 10.3 MHz	25°C	V		60		dBc
	f_{IN}= 19.6 MHz	25°C	V				dBc
	f_{IN}= 32.5 MHz	25°C	I		58		dBc
	f_{IN}= 51 MHz	25°C	V				dBc
TWO TONE INTERMOD DISTORTION (IMD)	f_{IN1}= 19 MHz, f_{IN2}= 20 MHz	25°C	V				dBc
	f_{IN1}= xx MHz, f_{IN2}= xx MHz	25°C	V				dBc

Table 3: AC Specifications

[1] SNR/harmonics based on an analog input voltage of –0.5 dBFS referenced to a 1 Vpp full-scale input range.

SWITCHING SPECIFICATIONS

AVDD = 3.0 V, DRVDD = 3.0 V; DIFFERENTIAL ENCODE INPUT

Parameter		Temp	Test Level	Min	Typ	Max	Unit
CLOCK	Clock Rate	Full	VI	65			MSPS
	Clock Pulse Width High (t_{EH})	Full	IV	6.9			ns
	Clock Pulse Width Low (t_{EL})	Full	IV	6.9			ns
OUTPUT PARAMETERS IN LVDS MODE	Valid Time (t_V)[1]	Full	VI	1.5			ns
	Propagation Delay (t_{PD}) [1]	Full	VI		3.5		ns
	MSB Propagation Delay (t_{MSB}) [1]	Full	VI				ns
	Rise Time (t_R) (20% to 80%)	Full	V		0.7		ns
	Fall Time (t_F) (20% to 80%)	Full	V		0.7		ns
	DCO Propagation Delay (t_{CPD})	Full	VI		3		ns
	Data to DCO Skew ($t_{PD} - t_{CPD}$)	Full	IV		0.5		ns
	Pipeline Latency	Full	VI		6		cycles
APERTURE	Aperture Delay (t_A)	25°C	V				ps
	Aperture Uncertainty (Jitter)	25°C	V		<1		ps rms

Table 4: Switching Specifications

EXPLANATION OF TEST LEVELS

TEST LEVEL

I 100% production tested.

II 100% production tested at +25°C and guaranteed by design and characterization at specified temperatures.

III Sample Tested Only

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C and guaranteed by design and characterization for industrial temperature range.

[1] t_V and t_{PD} are measured from the transition points of the CLK input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 5 pF or a dc current of ±40 µA. Rise and fall times measured from 20% to 80%.

OUTLINE DIMENSIONS

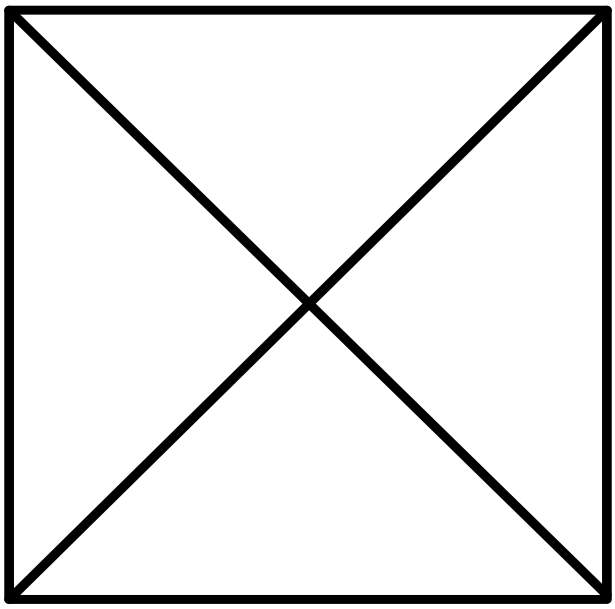

Figure 2:

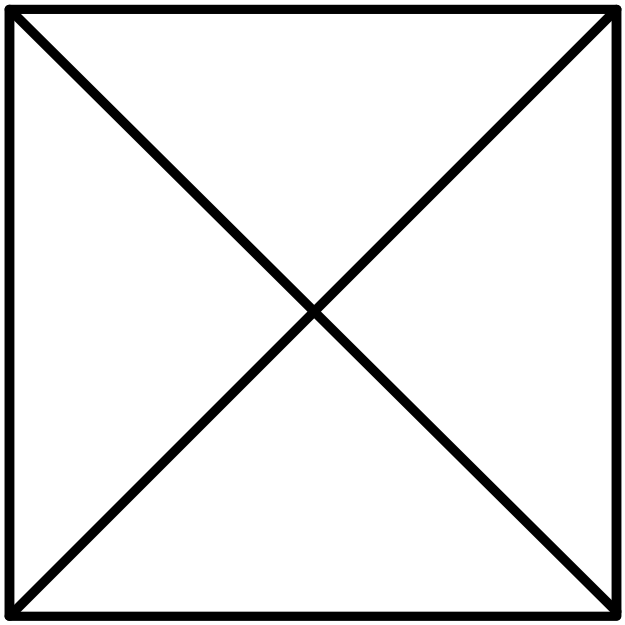

Figure 3:

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Ordering Guide

Model	Temperature Range	Description
AD9289BBC	-40°C to +85°C (Ambient)	64 CSP_BGA
AD9289/PCB	25°C (Ambient)	Evaluation Board

Table 5: Ordering Guide