

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS dual 8-bit digital-to-analog converter featuring excellent DAC-to-DAC matching.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7628TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Package	Description
Q-20	20-Pin Cerdip

1.3 Absolute Maximum Ratings.

V_{DD} to AGND	0 V, +17 V
V_{DD} to DGND	0 V, +17 V
AGND to DGND	$V_{DD} + 0.3$ V
Digital Input Voltage to DGND	-0.3 V, $V_{DD} + 0.3$ V
V_{PIN2} , V_{PIN20} to AGND	-0.3 V, $V_{DD} + 0.3$ V
$V_{REF A}$, $V_{REF B}$ to AGND	± 25 V
$V_{RFB A}$, $V_{RFB B}$ to AGND	± 25 V
Power Dissipation (Any Package) to +75°C	450 mW
Derates above +75°C by	6 mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

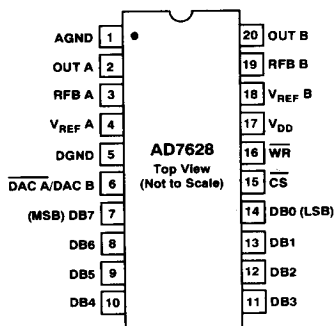
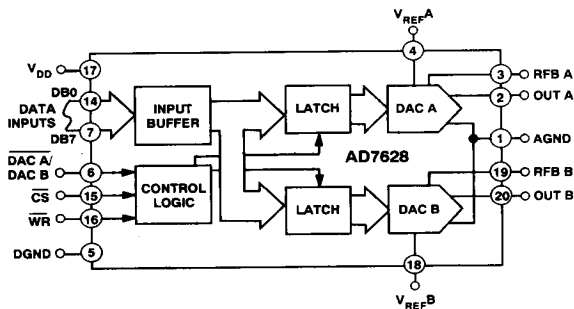
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DIGITAL-TO-ANALOG CONVERTERS

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Table 1.

Test	Symbol	Device	Limits		Sub Groups	Test Conditions	Unit
			Min	Max			
Resolution	RES	-1		8	1, 2, 3		Bits
Relative Accuracy	RA	-1	-0.5	+0.5	1, 2, 3	$V_{DD} = +10.8$ and $+15.75$	LSB
Differential Nonlinearity	DNL	-1	-1	+1	1, 2, 3	$V_{DD} = +10.8$ and $+15.75$	LSB
Gain Error	A_E	-1	-3	+3	1	$V_{DD} = +10.8$ and $+15.75$	LSB
Gain Temperature Coefficient	dA_E/dT	-1	0.0035	0.0035			%/°C
Output Leakage Current Pin 2	I_{OL}	-1	-200	+200	1, 2, 3	$V_{DD} = +10.8$ and $+15.75$ DAC Latches Loaded with 0	nA
Pin 20	I_{OL}	-1	-200	+200	1, 2, 3	$V_{DD} = +10.8$ and $+15.75$ DAC Latches Loaded with 0	nA
Reference Input Resistance Match	RM_{IN}	-1	-1	+1	1, 2, 3	$V_{DD} = +15.75$	%
Digital Input High Voltage	V_{INH}	-1	2.4		1, 2, 3	$V_{DD} = +15.75$ and $+10.8$	V
Digital Input Low Voltage	V_{INL}	-1		0.8	1, 2, 3	$V_{DD} = +15.75$ and $+10.8$	V
Digital Input Current	IN	-1	-10	+10	1, 2, 3	$V_{DD} = +15.75$ and $+10.8$	μ A
Digital Input Capacitance	C_{IN}	-1		10 15		DB0-DB7 \overline{WR} , \overline{CS} , DAC A, DAC B	pF
\overline{CS} to \overline{WR} Setup Time	t_{CS}	-1	210				ns
\overline{CS} to \overline{WR} Hold Time	t_{CH}	-1	10				ns
DAC Select to \overline{WR} Setup Time	t_{AS}	-1	210				ns
DAC Select to \overline{WR} Hold Time	t_{AH}	-1	10				ns
Data Valid to \overline{WR} Setup Time	t_{DS}	-1	210				ns
Data Valid to \overline{WR} Hold Time	t_{DH}	-1	10				ns
\overline{WR} Pulse Width	t_{WR}	-1	210				ns
Power Supply Current	I_{DD}	-1		2.5	1, 2, 3	$V_{DD} = +15.75$ and $+10.8$ for Dig Ips = V_{DD} or 0 V $V_{DD} = +10.8$ Only for Thresholds	mA
Reference Input Resistance	R_{IN}	-1	8	15	1, 2, 3	$V_{DD} = +10.8$ and $+15.75$ V	k Ω
Output Current Settling Time	t_{SL}	-1		400			ns
Feedthrough Error V_{REF} A to OUTA V_{REF} B to OUTB		-1 -1		65 65			-dB -dB

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

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4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

