# AD7490–SPECIFICATIONS

($V_{DD}$/$V_{DRIVE}$ = 2.7 V to 5.25 V, $REF_{IN}$ = 2.5 V, $f_{SCLK}$ = 20 MHz[1] – $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

| Parameter | B Version [2] | Unit | Test Conditions/Comments |
|---|---|---|---|
| DYNAMIC PERFORMANCE | | | $f_{IN}$ = 50 kHz Sine Wave, $f_{SCLK}$ = 20 MHz |
| Signal to Noise +1 Distortion (SINAD) [3] | 69 | dB min | @ 5 V, 70.5 dB typ |
| | 68 | dB min | @ 3 V, 69.5 dB typ |
| Signal to Noise Ratio (SNR)[3] | 69.5 | dB min | |
| Total Harmonic Distortion (THD) [3] | ..74 | dB max | @ 5 V, ..84 dB typ |
| | ..71 | dB max | @ 3 V, ..77 dB typ |
| Peak Harmonic or Spurious Noise (SFDR)[3] | ..75 | dB max | @ 5 V, ..86 dB typ |
| | ..73 | dB max | @ 3 V, ..80 dB typ |
| Intermodulation Distortion (IMD) [3] | | | fa = 40.1 kHz, fb = 41.5 kHz |
| Second Order Terms | ..85 | dB typ | |
| Third Order Terms | ..85 | dB typ | |
| Aperture Delay | 10 | ns typ | |
| Aperture Jitter | 50 | ps typ | |
| Channel-to-Channel Isolation[3] | ..82 | dB typ | $f_{IN}$ = 400 kHz |
| Full Power Bandwidth | 8.2 | MHz typ | @ 3 dB |
| | 1.6 | MHz typ | @ 0.1 dB |
| DC ACCURACY [3] | | | |
| Resolution | 12 | Bits | |
| Integral Nonlinearity | ±1 | LSB max | |
| Differential Nonlinearity | ..0.95/+1.5 | LSB max | Guaranteed No Missed Codes to 12 Bits |
| 0 V to $V_{REF\ IN}$ Input Range | | | Straight Binary Output Coding |
| Offset Error | ±8 | LSB max | ±0.6 LSB typ |
| Offset Error Match | ±0.5 | LSB max | |
| Gain Error | ±2 | LSB max | |
| Gain Error Match | ±0.6 | LSB max | |
| 0 V to 2 $V_{REF\ IN}$ Input Range | | | ..$V_{REF\ IN}$ to +$V_{REF\ IN}$ Biased about $V_{REF}$ with Twos Complement Output Coding Offset |
| Positive Gain Error | ±2 | LSB max | |
| Positive Gain Error Match | ±0.5 | LSB max | |
| Zero Code Error | ±8 | LSB max | ±0.6 LSB typ |
| Zero Code Error Match | ±0.5 | LSB max | |
| Negative Gain Error | ±1 | LSB max | |
| Negative Gain Error Match | ±0.5 | LSB max | |
| ANALOG INPUT | | | |
| Input Voltage Ranges | 0 to $REF_{IN}$ | V | RANGE Bit Set to 1 |
| | 0 to 2 $REF_{IN}$ | V | RANGE Bit Set to 0, $V_{DD}$/$V_{DRIVE}$ = 4.75 V to 5.25 V for 0 to 2 $REF_{IN}$ |
| DC Leakage Current | ±1 | µA max | |
| Input Capacitance | 20 | pF typ | |
| REFERENCE INPUT | | | |
| $REF_{IN}$ Input Voltage | 2.5 | V | ±1% Specified Performance |
| DC Leakage Current | ±1 | µA max | |
| $REF_{IN}$ Input Impedance | 36 | k typ | $f_{SAMPLE}$ = 1 MSPS |
| LOGIC INPUTS | | | |
| Input High Voltage, $V_{INH}$ | 0.7 $V_{DRIVE}$ | V min | |
| Input Low Voltage, $V_{INL}$ | 0.3 $V_{DRIVE}$ | V max | |
| Input Current, $I_{IN}$ | ±1 | µA max | Typically 10 nA, $V_{IN}$ 5 0 V or $V_{DRIVE}$ |
| Input Capacitance, $C_{IN}$[4] | 10 | pF max | |
| LOGIC OUTPUTS | | | |
| Output High Voltage, $V_{OH}$ | $V_{DRIVE}$ ..0.2 | V min | $I_{SOURCE}$ = 200 µA; $V_{DD}$ = 2.7 V to 5.25 V |
| Output Low Voltage, $V_{OL}$ | 0.4 | V max | $I_{SINK}$ = 200 µA |
| Floating-State Leakage Current | ±10 | µA max | Weak/Tri Bit Set to 0 |
| Floating-State Output Capacitance[4] | 10 | pF max | Weak/Tri Bit Set to 0 |
| Output Coding | Straight (Natural) Binary | | Coding Bit Set to 1 |
| | Twos Complement | | Coding Bit Set to 0 |

| Parameter | B Version [2] | Unit | Test Conditions/Comments |
|---|---|---|---|
| CONVERSION RATE | | | |
| Conversion Time | 800 | ns max | 16 SCLK Cycles, SCLK = 20 MHz |
| Track-and-Hold Acquisition Time [3] | 300 | ns max | Sine Wave Input |
| | 300 | ns max | Full-Scale Step Input |
| Throughput Rate | 1 | MSPS max | @ 5 V (See Serial Interface section.) |
| POWER REQUIREMENTS | | | |
| $V_{DD}$ | 2.7/5.25 | V min/max | |
| $V_{DRIVE}$ | 2.7/5.25 | V min/max | |
| $I_{DD}$ [5] | | | Digital I/Ps = 0 V or $V_{DRIVE}$ |
| Normal Mode (Static) | 600 | µA typ | $V_{DD}$ = 2.7 V to 5.25 V, SCLK On or Off |
| Normal Mode (Operational) | 2.5 | mA max | $V_{DD}$ = 4.75 V to 5.25 V, $f_{SCLK}$ = 20 MHz |
| ($f_S$ = Max Throughput) | 1.8 | mA max | $V_{DD}$ = 2.7 V to 3.6 V, $f_{SCLK}$ = 20 MHz |
| Auto Standby Mode | 1.55 | mA typ | $f_{SAMPLE}$ = 500 kSPS |
| | 92 | µA max | Static |
| Auto Shutdown Mode | 960 | µA typ | $f_{SAMPLE}$ = 250 kSPS |
| | 0.5 | µA max | Static |
| Full Shutdown Mode | 0.5 | µA max | SCLK On or Off (20 nA typ) |
| Power Dissipation[5] | | | |
| Normal Mode (Operational) | 12.5 | mW max | $V_{DD}$ = 5 V, $f_{SCLK}$ = 20 MHz |
| | 5.4 | mW max | $V_{DD}$ = 3 V, $f_{SCLK}$ = 20 MHz |
| Auto Standby Mode (Static) | 460 | µW max | $V_{DD}$ = 5 V |
| | 276 | µW max | $V_{DD}$ = 3 V |
| Auto Shutdown Mode (Static) | 2.5 | µW max | $V_{DD}$ = 5 V |
| | 1.5 | µW max | $V_{DD}$ = 3 V |
| Full Shutdown Mode | 2.5 | µW max | $V_{DD}$ = 5 V |
| | 1.5 | µW max | $V_{DD}$ = 3 V |

NOTES
[1]Specifications apply for $f_{SCLK}$ up to 20 MHz. However, for serial interfacing requirements, see Timing Specifications.
[2]Temperature Ranges (B Version): –40°C to +85°C.
[3]See Terminology section.
[4]Sample tested at 25°C to ensure compliance.
[5]See Power Versus Throughput Rate section.
Specifications subject to change without notice.

# TIMING SPECIFICATIONS[1] ($V_{DD}$ = 2.7 V to 5.25 V, $V_{DRIVE} \le V_{DD}$, $V_{REF}$ = 2.5 V, $T_A = T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | | Unit | Description |
|---|---|---|---|---|
| | $V_{DD}$ = 3 V | $V_{DD}$ = 5 V | | |
| $f_{SCLK}$[2] | 10 | 10 | kHz min | |
| | 16 | 20 | MHz max | |
| $t_{CONVERT}$ | 16 $t_{SCLK}$ | 16 $t_{SCLK}$ | | |
| $t_{QUIET}$ | 50 | 50 | ns min | Minimum Quiet Time Required between Bus Relinquish and Start of Next Conversion |
| $t_2$ | 12 | 10 | ns min | CS to SCLK Setup Time |
| $t_3$[3] | 20 | 14 | ns max | Delay from CS until DOUT Three-State Disabled |
| $t_3b$[4] | 30 | 20 | ns max | Delay from CS to DOUT Valid |
| $t_4$[3] | 60 | 40 | ns max | Data Access Time after SCLK Falling Edge |
| $t_5$ | 0.4 $t_{SCLK}$ | 0.4 $t_{SCLK}$ | ns min | SCLK Low Pulsewidth |
| $t_6$ | 0.4 $t_{SCLK}$ | 0.4 $t_{SCLK}$ | ns min | SCLK High Pulsewidth |
| $t_7$ | 15 | 15 | ns min | SCLK to DOUT Valid Hold Time |
| $t_8$[5] | 15/50 | 15/50 | ns min/max | SCLK Falling Edge to DOUT High Impedance |
| $t_9$ | 20 | 20 | ns min | DIN Setup Time prior to SCLK Falling Edge |
| $t_{10}$ | 5 | 5 | ns min | DIN Hold Time after SCLK Falling Edge |
| $t_{11}$ | 20 | 20 | ns min | Sixteenth SCLK Falling Edge to CS High |
| $t_{12}$ | 1 | 1 | µs max | Power-Up Time from Full Power-Down/ Auto Shutdown/Auto Standby Modes |

NOTES

[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of 1.6 V. (See Figure 1.) The 3 V operating range spans from 2.7 V to 3.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40. The maximum SCLK frequency is 16 MHz with $V_{DD}$ = 3 V to give a throughput of 870 kSPS. Care must be taken when interfacing to account for data access time, $t_4$, and the setup time required for the user's processor. These two times will determine the maximum SCLK frequency with which the user's system can operate. (See Serial Interface section.)

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.4 V or 0.7 $V_{DRIVE}$ V.

[4]$t_3b$ represents a worst-case figure for having ADD3 available on the DOUT line, i.e., if the AD7490 went back into three-state at the end of a conversion and some other device took control of the bus between conversions, the user would have to wait a maximum time of $t_3b$ before having ADD3 valid on DOUT line. If the DOUT line is weakly driven to ADD3 between conversions, then the user would typically have to wait 17 ns at 3 V and 12 ns at 5 V after the CS falling edge before seeing ADD3 valid on DOUT.

[5]$t_8$ is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, $t_8$, quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

Table II. Channel Selection

| ADD3 | ADD2 | ADD1 | ADD0 | Analog Input Channel |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $V_{IN}$ 0 |
| 0 | 0 | 0 | 1 | $V_{IN}$ 1 |
| 0 | 0 | 1 | 0 | $V_{IN}$ 2 |
| 0 | 0 | 1 | 1 | $V_{IN}$ 3 |
| 0 | 1 | 0 | 0 | $V_{IN}$ 4 |
| 0 | 1 | 0 | 1 | $V_{IN}$ 5 |
| 0 | 1 | 1 | 0 | $V_{IN}$ 6 |
| 0 | 1 | 1 | 1 | $V_{IN}$ 7 |
| 1 | 0 | 0 | 0 | $V_{IN}$ 8 |
| 1 | 0 | 0 | 1 | $V_{IN}$ 9 |
| 1 | 0 | 1 | 0 | $V_{IN}$ 10 |
| 1 | 0 | 1 | 1 | $V_{IN}$ 11 |
| 1 | 1 | 0 | 0 | $V_{IN}$ 12 |
| 1 | 1 | 0 | 1 | $V_{IN}$ 13 |
| 1 | 1 | 1 | 0 | $V_{IN}$ 14 |
| 1 | 1 | 1 | 1 | $V_{IN}$ 15 |

Table III. Power Mode Selection

| PM1 | PM0 | Mode |
|---|---|---|
| 1 | 1 | Normal Operation<br>In this mode, the AD7490 remains in full power mode regardless of the status of any of the logic inputs. This mode allows the fastest possible throughput rate from the AD7490. |
| 1 | 0 | Full Shutdown<br>In this mode, the AD7490 is in full shut-down mode, with all circuitry on the AD7490 powering down. The AD7490 retains the information in the Control Register while in full shutdown. The part remains in full shutdown until these bits are changed in the Control Register. |
| 0 | 1 | Auto Shutdown<br>In this mode, the AD7490 automatically enters shutdown mode at the end of each conversion when the Control Register is updated. Wake-up time from shutdown is 1 μs and the user should ensure that 1μs has elapsed before attempting to perform a valid conversion on the part in this mode. |
| 0 | 0 | Auto Standby<br>In this standby mode, portions of the AD7490 are powered down, but the on-chip bias generator remains powered-up. This mode is similar to Auto Shutdown and allows the part to power-up within one dummy cycle, i.e., 1 μs with a 20 MHz SCLK. |

For more information, see the Modes of Operation section.

SEQUENCER OPERATION

The configuration of the SEQ and Shadow Bits in the Control Register allows the user to select a particular mode of operation of the sequencer function. Table IV outlines the four modes of operation of the Sequencer.

Table IV. Sequence Selection

| SEQ | SHADOW | Sequence Type |
|---|---|---|
| 0 | 0 | This configuration means the sequence function is not used. The analog input channel selected for each individual conversion is determined by the contents of the channel address bits ADD0 through ADD3 in each prior write operation. This mode of operation reflects the normal operation of a multichannel ADC, without sequencer function being used, where each write to the AD7490 selects the next channel for conversion. (See Figure 2.) |
| 0 | 1 | This configuration selects the Shadow Register for programming. After the write to the Control Register, the following write operation will load the contents of the Shadow Register. This will program the sequence of channels to be converted on continuously with each successive valid CS falling edge. (See Shadow Register, Table V, and Figure 3.) The channels selected need not be consecutive. |
| 1 | 0 | If the SEQ and SHADOW Bits are set in this way, then the sequence function will not be interrupted upon completion of the WRITE operation. This allows other bits in the Control Register to be altered while in a sequence without terminating the cycle. |
| 1 | 1 | This configuration is used in conjunction with the channel address bits ADD3 to ADD0 to program continuous conversions on a consecutive sequence of channels from Channel 0 through to a selected final channel as determined by the channel address bits in the Control Register. (See Figure 4.) |

## APPLICATION HINTS

### Grounding and Layout

The AD7490 has very good immunity to noise on the power supplies as can be seen by the PSRR vs. Supply Ripple Frequency plot, TPC 3. However, care should still be taken with regard to grounding and layout.

The printed circuit board that houses the AD7490 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. All three AGND pins of the AD7490 should be sunk in the AGND plane. Digital and analog ground planes should be joined at only one place. If the AD7490 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7490.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7490 to avoid noise coupling. The power supply lines to the AD7490 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to AGND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1µF capacitors should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types or surface mount types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

### PCB Design Guidelines For Chip Scale Package

The lands on the chip scale package (CP-32), are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This will ensure that the solder joint size is maximized. The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This will ensure that shorting is avoided. Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz. copper to plug the via. The user should connect the printed circuit board thermal pad to AGND.

### Evaluating the AD7490 Performance

The recommended layout for the AD7490 is outlined in the evaluation board for the AD7490. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-BOARD CONTROLLER. The EVAL-BOARD CON TROLLER can be used in conjunction with the AD7490 Evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/ evaluate the ac and dc performance of the AD7490.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7490. The software and documentation are on a CD shipped with the evaluation board.

# Revision History

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| 10/02—Data Sheet changed from REV. 0 to REV. A. | |
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