

### FEATURES

- 12-Bit Linearity and Monotonic AD5582
- 10-Bit Linearity and Monotonic AD5583
- Wide Operating Range: Single +5 V to +15 V or  
Dual  $\pm 5$  V Supply
- Unipolar or Bipolar Operation
- Double Buffered Registers Enable Independent or  
Simultaneous Multichannel Update
- 4 Independent Rail-to-Rail Reference Inputs
- Parallel Interface
- Data Readback Capability
- 5  $\mu$ s Settling Time
- Buffered Output
- Built-In Matching Resistor Simplifies  
Negative Reference
- Compact Footprint: TSSOP-48
- Extended Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

### APPLICATIONS

- Process Control Equipment
- Closed-Loop Servo Control
- Data Acquisition Systems
- Digitally Controlled Calibration
- Motor Control
- Optical Network Control Loops

### GENERAL DESCRIPTION

The AD5582/AD5583 family of quad, 12-/10-bit, voltage output digital-to-analog converters is designed to operate from a single +5 V to +15 V or dual  $\pm 5$  V supply. Built using an advanced BiCMOS process, this high performance DAC is cost effective and compact. It offers the user ease of use in single-or dual-supply systems.

The applied external reference  $V_{REF}$  determines the full-scale output voltage. Valid  $V_{REF}$  values include  $V_{SS} < V_{REF} < V_{DD}$  resulting in a wide selection of full-scale outputs. For multiplying and wide dynamic applications, ac reference inputs can be as high as  $|V_{DD} - V_{SS}|$ . Two built-in precision trimmed resistors are available and can be configured easily to provide four-quadrant multiplications.

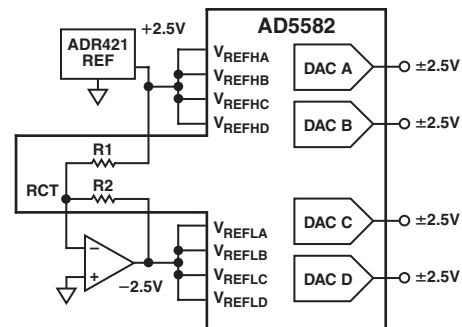
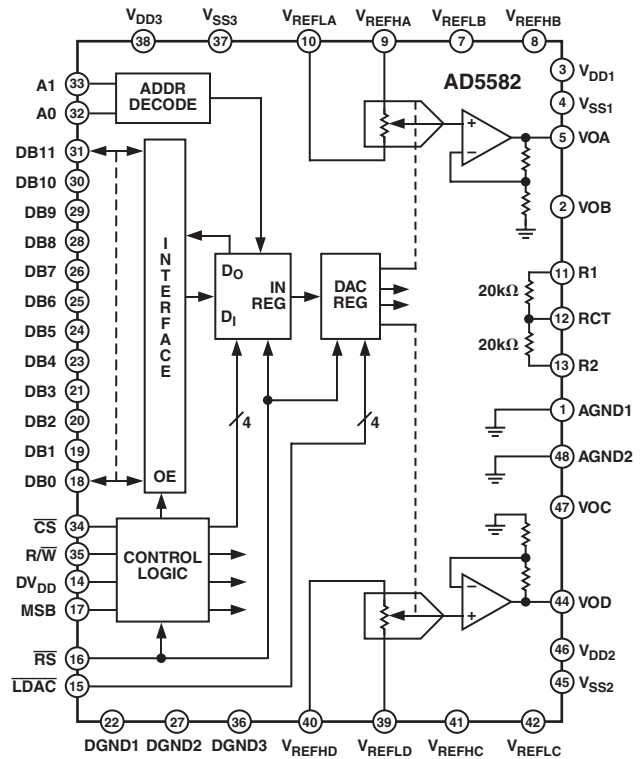
A doubled-buffered parallel interface offers 25 Mbps data load rates. A common level sensitive load DAC strobe ( $\overline{LDAC}$ ) input allows simultaneous update of all DAC outputs from previously loaded input registers. An external asynchronous reset ( $\overline{RS}$ ) forces all registers to the zero code state when  $\overline{MSB} = 0$  or to midscale when  $\overline{MSB} = 1$ .

Both parts are offered in the same pinout to allow users to select the amount of resolution appropriate for their application without PCB layout changes.

### REV. 0

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### FUNCTIONAL BLOCK DIAGRAM



DIGITAL CIRCUITRY OMITTED FOR CLARITY

Figure 1. Using Built-In Matching Resistors to Generate a Negative Voltage Reference

AD5582 is well suited for DAC8412 replacement in medium voltage applications in new designs.

The AD5582/AD5583 are specified over the extended industrial ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) temperature range and offered in a thin and compact 1.1 mm TSSOP-48 package.

# AD5582/AD5583—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS ( $V_{DD} = +5\text{ V}$ , $V_{SS} = -5\text{ V}$ , $DV_{DD} = +5\text{ V} \pm 10\%$ , $V_{REFH} = +2.5\text{ V}$ , $V_{REFL} = -2.5\text{ V}$ , $-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
<b>STATIC PERFORMANCE</b>						
Resolution <sup>2</sup>	N	AD5582 AD5583		12 10		Bits Bits
Relative Accuracy <sup>3</sup>	INL		-1		+1	LSB
Differential Nonlinearity <sup>3</sup>	DNL	Monotonic	-1			LSB
Zero-Scale Error	$V_{ZSE}$	Data = 000 <sub>H</sub> for AD5582 and AD5583	-2		+2	LSB
Gain Error	$V_{GE}$	Data = FFF <sub>H</sub> for AD5582 and 3FF <sub>H</sub> for AD5583	-2		+2	LSB
Gain Error Full-Scale Tempco <sup>4</sup>	$V_{GE}$ $TCV_{FS}$	$V_{DD} = 2.7\text{ V} - 4.5\text{ V}$	-4	1.5	+4	LSB ppm/°C
<b>REFERENCE INPUT</b>						
$V_{REFH}$ Input Range	$V_{REFH}$		$V_{REFL} + 0.5$		$V_{DD}$	V
$V_{REFL}$ Input Range <sup>5</sup>	$V_{REFL}$		$V_{SS}$		$V_{REFH} - 0.5$	V
Input Resistance	$R_{REF}$	Data = 555 <sub>H</sub> (Minimum $R_{REF}$ ) for AD5582 and 155 <sub>H</sub> for AD5583	12	20		k $\Omega$ <sup>1</sup>
Input Capacitance <sup>4</sup>	$C_{REF}$			80		pF
REF Input Current	$I_{REF}$	Data = 555 <sub>H</sub> for AD5582			500	$\mu\text{A}$
REF Multiplying Bandwidth	$BW_{REF}$	Code = Full Scale			1.3	MHz
R1–R2 Matching	R1/R2	AD5582 AD5583			$\pm 0.025$ $\pm 0.100$	% %
<b>ANALOG OUTPUT</b>						
Output Current <sup>6</sup>	$I_{OUT}$	Data = 800 <sub>H</sub> for AD5582 and 200 <sub>H</sub> for AD5583, $\Delta V_{OUT} \leq 4\text{ mV}$			$\pm 2$	mA
Capacitive Load <sup>4</sup>	$C_L$	No Oscillation		2000		pF
<b>LOGIC INPUTS</b>						
Logic Input Low Voltage	$V_{IL}$	$DV_{DD} = 5\text{ V} \pm 10\%$ $DV_{DD} = 3\text{ V} \pm 10\%$			0.8 0.4	V V
Logic Input High Voltage	$V_{IH}$	$DV_{DD} = 5\text{ V} \pm 10\%$ $DV_{DD} = 3\text{ V} \pm 10\%$	2.4 2.1			V V
Input Leakage Current	$I_{IL}$			0.01	1	$\mu\text{A}$
Input Capacitance <sup>4</sup>	$C_{IL}$			5		pF
Output Voltage High	$V_{OH}$	$I_{OH} = -0.8\text{ mA}$	2.4			V
Output Voltage Low	$V_{OL}$	$I_{OL} = 1.2\text{ mA}$ , $T_A = 85^{\circ}\text{C}$ $I_{OL} = 0.6\text{ mA}$ , $DV_{DD} = 3\text{ V}$ $I_{OL} = 1.0\text{ mA}$ , $T_A = 125^{\circ}\text{C}$ , $I_{OL} = 0.5\text{ mA}$ , $DV_{DD} = 3\text{ V}$			0.4 0.4	V V
<b>AC CHARACTERISTICS</b>						
Output Slew Rate	SR	Data = Zero Scale to Full Scale to Zero Scale		2		V/ $\mu\text{s}$
Settling Time <sup>7</sup>	$t_s$	To $\pm 0.1\%$ of Full Scale		5		$\mu\text{s}$
DAC Glitch	Q	Code 7FF <sub>H</sub> to 800 <sub>H</sub> to 7FF <sub>H</sub> for AD5582 and 1FF <sub>H</sub> to 200 <sub>H</sub> to 1FF <sub>H</sub> for AD5583		100		nVs
Digital Feedthrough	$V_{OUT}/t_{CS}$	Data = Midscale, $\overline{CS}$ Toggles at $f = 16\text{ MHz}$		5		nVs
Analog Crosstalk	$V_{OUT}/V_{REF}$	$V_{REF} = 1.5\text{ V dc} + 1\text{ V p-p}$ , Data = 000 <sub>H</sub> , $f = 100\text{ kHz}$		-80		dB
Output Noise	$e_N$	$f = 1\text{ kHz}$		33		nV/ $\sqrt{\text{Hz}}$

Parameter	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
<b>SUPPLY CHARACTERISTICS</b>						
Single-Supply Voltage Range	V <sub>DD</sub>	V <sub>SS</sub> = 0 V	3		18	V
Dual-Supply Voltage Range	V <sub>DD</sub> /V <sub>SS</sub>	V <sub>DD</sub> = +2.7 V to +6.5 V, V <sub>SS</sub> = -6.5 V to -2.7 V	-9		+9	V
Digital Logic Supply	DV <sub>DD</sub>		2.7		8	V
Positive Supply Current <sup>6</sup>	I <sub>DD</sub>	V <sub>IL</sub> = 0 V, No Load		1.7	3	mA
Negative Supply Current	I <sub>SS</sub>	V <sub>IL</sub> = 0 V, No Load		1.5	3	mA
Power Dissipation	P <sub>DISS</sub>	V <sub>IL</sub> = 0 V, No Load		16	30	mW
Power Supply Sensitivity	P <sub>SS</sub>	ΔV <sub>DD</sub> = ±5%		30		ppm/V

**NOTES**

<sup>1</sup>Typical specifications represent average readings measured at 25°C.

<sup>2</sup>DAC Output Equation:  $V_{OUT} = V_{REFL} + [(V_{REFH} - V_{REFL}) \times D/2^N]$ , where D = data loaded in corresponding DAC Register A, B, C, D, and N equals the number of bits; AD5582 = 12 bits, AD5583 = 10 bits. One LSB step voltage =  $(V_{REFH} - V_{REFL})/4096$  V and  $(V_{REFH} - V_{REFL})/1024$  V for AD5582 and AD5583, respectively.

<sup>3</sup>The first two codes (000<sub>H</sub>, 001<sub>H</sub>) of the AD5583 and the first four codes (000<sub>H</sub>, 001<sub>H</sub>, 002<sub>H</sub>, 003<sub>H</sub>) of the AD5582 are excluded from the linearity error measurement in single-supply operation.

<sup>4</sup>These parameters are guaranteed by design and not subject to production testing.

<sup>5</sup>Dual-supply operation, V<sub>REFL</sub> = V<sub>SS</sub>, exclude the lowest eight codes for the AD5582 and two codes for the AD5583 for INL and DNL errors.

<sup>6</sup>Short circuit output and supply currents are 24 mA and 25 mA, respectively.

<sup>7</sup>The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground in single-supply operation.

Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS (V<sub>DD</sub> = +15 V, V<sub>SS</sub> = 0 V, DV<sub>DD</sub> = +5 V ± 10%, V<sub>REFH</sub> = +10 V, V<sub>REFL</sub> = 0 V, -40°C < T<sub>A</sub> < +125°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
<b>STATIC PERFORMANCE</b>						
Resolution <sup>2</sup>	N	AD5582 AD5583		12 10		Bits Bits
Relative Accuracy <sup>3</sup>	INL		-1		+1	LSB
Differential Nonlinearity <sup>3</sup>	DNL	Monotonic	-1			LSB
Zero-Scale Error	V <sub>ZSE</sub>	Data = 000 <sub>H</sub> for AD5582 and AD5583	-2		+2	LSB
Gain Error	V <sub>GE</sub>	Data = FFF <sub>H</sub> for AD5582 and 3FF <sub>H</sub> for AD5583	-2		+2	LSB
Full-Scale Tempco <sup>4</sup>	TCV <sub>FS</sub>			1.5		ppm/°C
<b>REFERENCE INPUT</b>						
V <sub>REFH</sub> Input Range	V <sub>REFH</sub>		V <sub>REFL</sub> + 0.5		V <sub>DD</sub>	V
V <sub>REFL</sub> Input Range <sup>5</sup>	V <sub>REFL</sub>		V <sub>SS</sub>		V <sub>REFH</sub> - 0.5	V
Input Resistance	R <sub>REF</sub>	Data = 555 <sub>H</sub> (Minimum R <sub>REF</sub> ) for AD5582 and 155 <sub>H</sub> for AD5583	12	20		kΩ <sup>1</sup>
Input Capacitance <sup>4</sup>	C <sub>REF</sub>			80		pF
REF Input Current	I <sub>REF</sub>	Data = 555 <sub>H</sub> for AD5582			1000	μA
REF Multiplying Bandwidth	BW <sub>REF</sub>	Code = Full Scale			1.3	MHz
R1-R2 Matching	R1/R2	AD5582 AD5583			±0.025 ±0.100	% %
<b>ANALOG OUTPUT</b>						
Output Current <sup>6</sup>	I <sub>OUT</sub>	Data = 800 <sub>H</sub> for AD5582 and 200 <sub>H</sub> for AD5583, ΔV <sub>OUT</sub> ≤ 4 mV			2	mA
Capacitive Load <sup>4</sup>	C <sub>L</sub>	No Oscillation		2000		pF
<b>LOGIC INPUTS/OUTPUTS</b>						
Logic Input Low Voltage	V <sub>IL</sub>	DV <sub>DD</sub> = 3 V ± 10%			0.8 0.4	V V
Logic Input High Voltage	V <sub>IH</sub>	DV <sub>DD</sub> = 3 V ± 10%	2.4 2.1			V V
Input Leakage Current	I <sub>IL</sub>					μA
Input Capacitance <sup>4</sup>	C <sub>IL</sub>					pF
Output Voltage High	V <sub>OH</sub>	I <sub>OH</sub> = -0.8 mA	2.4			V
Output Voltage Low	V <sub>OL</sub>	I <sub>OL</sub> = 1.2 mA, T <sub>A</sub> = 85°C I <sub>OL</sub> = 0.6 mA, DV <sub>DD</sub> = 3 V I <sub>OL</sub> = 1.0 mA, T <sub>A</sub> = 125°C I <sub>OL</sub> = 0.5 mA, DV <sub>DD</sub> = 3 V			0.4	V

# AD5582/AD5583

## ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
<b>AC CHARACTERISTICS</b>						
Output Slew Rate	SR	Data = Zero Scale to Full Scale to Zero Scale		2		V/μs
Settling Time <sup>7</sup>	t <sub>s</sub>	To ±0.1% of Full Scale		14		μs
DAC Glitch	Q	Code 7FF <sub>H</sub> to 800 <sub>H</sub> to 7FF <sub>H</sub> for AD5582 and 1FF <sub>H</sub> to 200 <sub>H</sub> to 1FF <sub>H</sub> for AD5583		100		nVs
Digital Feedthrough	V <sub>OUT</sub> /t <sub>CS</sub>	Data = Midscale, $\overline{CS}$ Toggles at f = 16 MHz		5		nVs
Analog Crosstalk	V <sub>OUT</sub> /V <sub>REF</sub>	V <sub>REF</sub> = 1.5 V dc + 1 V p-p, Data = 000 <sub>H</sub> , f = 100 kHz		-80		dB
Output Noise	e <sub>N</sub>	f = 1 kHz		33		nV/ $\sqrt{\text{Hz}}$
<b>SUPPLY CHARACTERISTICS</b>						
Single-Supply Voltage Range	V <sub>DD</sub>	V <sub>SS</sub> = 0 V	3		16.5	V
Dual-Supply Voltage Range	V <sub>DD</sub> /V <sub>SS</sub>	V <sub>DD</sub> = +2.7 V to +6.5 V, V <sub>SS</sub> = -6.5 V to -2.7 V	-6.5		+6.5	V
Digital Logic Supply	DV <sub>DD</sub>		2.7		6.5	V
Positive Supply Current <sup>6</sup>	I <sub>DD</sub>	V <sub>IL</sub> = 0 V, No Load		2.3	3.5	mA
Power Dissipation	P <sub>DISS</sub>	V <sub>IL</sub> = 0 V, No Load		34.5	52.5	mW
Power Supply Sensitivity	PSS	ΔV <sub>DD</sub> = ±5%		30		ppm/V

### NOTES

<sup>1</sup>Typical specifications represent average readings measured at 25°C.

<sup>2</sup>DAC Output Equation:  $V_{OUT} = V_{REFL} + [(V_{REFH} - V_{REFL}) \times D/2^N]$ , where D = data in decimal loaded in corresponding DAC Register A, B, C, D, and N equals the number of bits; AD5582 = 12 bits, AD5583 = 10 bits. One LSB step voltage =  $(V_{REFH} - V_{REFL})/4096$  V and  $(V_{REFH} - V_{REFL})/1024$  V for AD5582 and AD5583, respectively.

<sup>3</sup>The first two codes (000<sub>H</sub>, 001<sub>H</sub>) of the AD5583 and the first four codes (000<sub>H</sub>, 001<sub>H</sub>, 002<sub>H</sub>, 003<sub>H</sub>) of the AD5582 are excluded from the linearity error measurement in single-supply operation.

<sup>4</sup>These parameters are guaranteed by design and not subject to production testing.

<sup>5</sup>Dual-supply operation, V<sub>REFL</sub> = V<sub>SS</sub>, exclude the lowest eight codes for the AD5582 and two codes for the AD5583 for INL and DNL errors.

<sup>6</sup>Short circuit output and supply currents are 24 mA and 25 mA, respectively.

<sup>7</sup>The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground in single-supply operation.

Specifications subject to change without notice.

## TIMING CHARACTERISTICS ( $V_{DD} = 15\text{ V}$ or $5\text{ V}$ , $V_{SS} = 0\text{ V}$ , $DV_{DD} = 5\text{ V} \pm 10\%$ , $V_{REFH} = 10\text{ V}$ , $V_{REFL} = 0\text{ V}$ , $-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INTERFACE TIMING*						
Clock Frequency	$f_{CLK}$				25	MHz
Chip Select Write Pulsewidth	$t_{WCS}$		20			ns
Chip Select Read Pulsewidth	$t_{RCS}$		130			ns
Write Setup	$t_{WS}$		0			ns
Write Hold	$t_{WH}$		0			ns
Address Setup	$t_{AS}$		0			ns
Address Hold	$t_{AH}$		0			ns
Load Setup	$t_{LS}$		0			ns
Load Hold	$t_{LH}$		0			ns
Write Data Setup	$t_{WDS}$		0			ns
Write Data Hold	$t_{WDH}$		0			ns
Load Data Pulsewidth	$t_{LDW}$		20			ns
Reset Pulsewidth	$t_{RESET}$		20			ns
Read Data Hold	$t_{RDH}$		0			ns
Read Data Setup	$t_{RDS}$		0			ns
Data to Hi-Z	$t_{DZ}$	$C_L = 10\text{ pF}$			100	ns
Chip Select to Data	$t_{CSD}$	$C_L = 10\text{ pF}$			100	ns
Chip Select Repetitive Pulsewidth	$t_{CSP}$		10			ns
Load Setup in Double Buffer Mode	$t_{LDS}$		20			ns
Load Data Hold	$t_{LDH}$		0			ns

\*All input control signals are specified with  $t_R = t_F = 2\text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Specifications subject to change without notice.

## TIMING CHARACTERISTICS ( $V_{DD} = 15\text{ V}$ or $5\text{ V}$ , $V_{SS} = 0\text{ V}$ , $DV_{DD} = 3\text{ V} \pm 10\%$ , $V_{REFH} = 10\text{ V}$ , $V_{REFL} = 0\text{ V}$ , $-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INTERFACE TIMING*						
Clock Frequency	$f_{CLK}$				14	MHz
Chip Select Write Pulsewidth	$t_{WCS}$		35			ns
Chip Select Read Pulsewidth	$t_{RCS}$		130			ns
Write Setup	$t_{WS}$		0			ns
Write Hold	$t_{WH}$		0			ns
Address Setup	$t_{AS}$		0			ns
Address Hold	$t_{AH}$		0			ns
Load Setup	$t_{LS}$		0			ns
Load Hold	$t_{LH}$		0			ns
Write Data Setup	$t_{WDS}$		0			ns
Write Data Hold	$t_{WDH}$		0			ns
Load Data Pulsewidth	$t_{LDW}$		35			ns
Reset Pulsewidth	$t_{RESET}$		35			ns
Read Data Hold	$t_{RDH}$		0			ns
Read Data Setup	$t_{RDS}$		0			ns
Data to Hi-Z	$t_{DZ}$	$C_L = 10\text{ pF}$	80		100	ns
Chip Select to Data	$t_{CSD}$	$C_L = 10\text{ pF}$	80		100	ns
Chip Select Repetitive Pulsewidth	$t_{CSP}$		20			ns
Load Setup in Double Buffer Mode	$t_{LDS}$		35			ns
Load Data Hold	$t_{LDH}$		0			ns

\*All input control signals are specified with  $t_R = t_F = 2\text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Specifications subject to change without notice.

# AD5582/AD5583

## ABSOLUTE MAXIMUM RATINGS\*

V <sub>DD</sub> to V <sub>SS</sub>	-0.3 V to +18 V
V <sub>DD</sub> to GND	-0.3 V to +18 V
V <sub>SS</sub> to GND	+0.3 V to -9 V
V <sub>DD</sub> to V <sub>REF+</sub>	-0.3 V to (V <sub>DD</sub> - V <sub>SS</sub> )
V <sub>REF-</sub> to V <sub>SS</sub>	-0.3 V to (V <sub>DD</sub> - V <sub>SS</sub> )
V <sub>REFH</sub> to V <sub>REFL</sub>	-0.3 V to (V <sub>DD</sub> - V <sub>SS</sub> )
DV <sub>DD</sub> to GND	8 V
Logic Inputs to GND	V <sub>SS</sub> - 0.3 V, V <sub>DD</sub> + 0.3 V
V <sub>OUT</sub> to GND	V <sub>SS</sub> - 0.3 V, V <sub>DD</sub> + 0.3 V
I <sub>OUT</sub> Short Circuit to GND	24 mA
Thermal Resistance Junction to Ambient, θ <sub>JA</sub>	115°C/W

Thermal Resistance Junction to Case, θ <sub>JC</sub>	42°C/W
Maximum Junction Temperature (T <sub>J</sub> Max)	150°C
Package Power Dissipation = (T <sub>J</sub> Max - T <sub>A</sub> )/θ <sub>JA</sub>	
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
RU-48 (Soldering, 60 secs)	300°C

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING GUIDE\*

Model	Resolution (Bits)	Temperature Range	Package Description	Package Option	Container Quantity	Top Marking
AD5582YRU-REEL	12	-40°C to +125°C	TSSOP-48	RU-48	2500	AD5582Y
AD5583YRU-REEL	10	-40°C to +125°C	TSSOP-48	RU-48	2500	AD5583Y
AD5582YRU	12	-40°C to +125°C	TSSOP-48	RU-48	39	AD5582Y
AD5583YRU	10	-40°C to +125°C	TSSOP-48	RU-48	39	AD5583Y

\*The AD5582 contains 4116 transistors. The die size measures 108 mil × 144 mil.

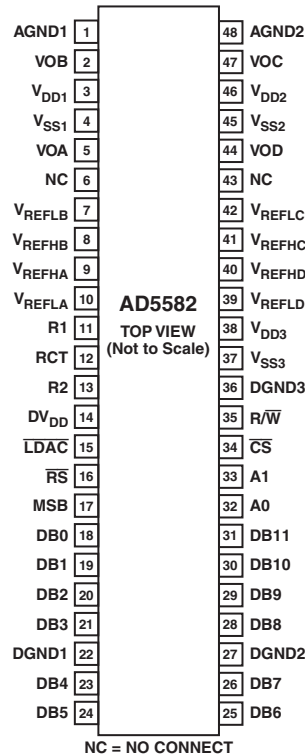
First row marking is shown in the table above. Second row marking contains date code in YYWW format. Third row marking contains the lot number.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5582/AD5583 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## AD5582 PIN CONFIGURATION



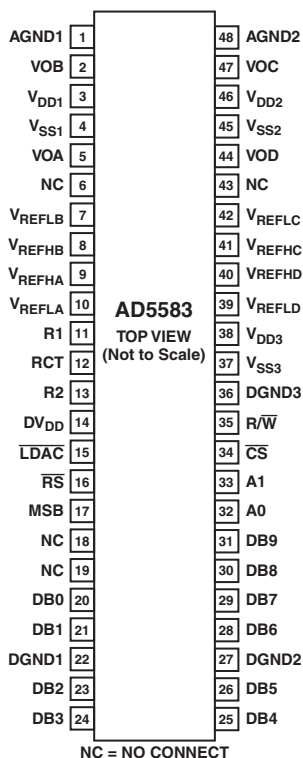
### AD5582 PIN FUNCTION DESCRIPTIONS\*

Pin No.	Mnemonic	Description	Pin No.	Mnemonic	Description
1	AGND1	Analog Ground for DAC A and B	25	DB6	Data Bit 6
2	VOB	DAC B Output	26	DB7	Data Bit 7
3	V <sub>DD1</sub>	Positive Power Supply for DAC A and B	27	DGND2	Digital Ground 2
4	V <sub>SS1</sub>	Negative Power Supply for DAC A and B	28	DB8	Data Bit 8
5	VOA	DAC A Output	29	DB9	Data Bit 9
6	NC	No Connect	30	DB10	Data Bit 10
7	V <sub>REFLB</sub>	DAC B Voltage Reference Low Terminal	31	DB11	Data Bit 11
8	V <sub>REFHB</sub>	DAC B Voltage Reference High Terminal	32	A0	Address Input 0
9	V <sub>REFHA</sub>	DAC A Voltage Reference High Terminal	33	A1	Address Input 1
10	V <sub>REFLA</sub>	DAC A Voltage Reference Low Terminal	34	$\overline{CS}$	Chip Select, Active Low
11	R1	R1 Terminal (for Negative Reference)	35	R/ $\overline{W}$	Read/Write Mode Select
12	RCT	Center Tap Terminal (for Negative Reference)	36	DGND3	Digital Ground 3
13	R2	R2 Terminal (for Negative Reference)	37	V <sub>SS3</sub>	Negative Power Supply for Analog Switches
14	DV <sub>DD</sub>	Power Supply for Digital Circuits	38	V <sub>DD3</sub>	Positive Power Supply for Analog Switches
15	$\overline{LDAC}$	DAC Register Load, Active Low Level Sensitive	39	V <sub>REFLD</sub>	DAC D Voltage Reference Low Terminal
16	$\overline{RS}$	Reset Strobe	40	V <sub>REFHD</sub>	DAC D Voltage Reference High Terminal
17	MSB	MSB = 0, Reset to 000 <sub>H</sub> , MSB = 1, Reset to 800 <sub>H</sub>	41	V <sub>REFHC</sub>	DAC C Voltage Reference High Terminal
18	DB0	Data Bit 0	42	V <sub>REFLC</sub>	DAC C Voltage Reference Low Terminal
19	DB1	Data Bit 1	43	NC	No Connect
20	DB2	Data Bit 2	44	VOD	DAC D Output
21	DB3	Data Bit 3	45	V <sub>SS2</sub>	Negative Power Supply for DAC C and D
22	DGND1	Digital Ground 1	46	V <sub>DD2</sub>	Positive Power Supply for DAC C and D
23	DB4	Data Bit 4	47	VOC	DAC C Output
24	DB5	Data Bit 5	48	AGND2	Analog Ground for DAC C and D

\*AD5582 optimizes internal layout design to reduce die area so that all supply voltage pins are required to be connected externally. See Figure 5.

# AD5582/AD5583

## AD5583 PIN CONFIGURATION



## AD5583 PIN FUNCTION DESCRIPTIONS\*

Pin No.	Mnemonic	Description	Pin No.	Mnemonic	Description
1	AGND1	Analog Ground for DAC A and B	25	DB4	Data Bit 4
2	VOB	DAC B Output	26	DB5	Data Bit 5
3	V <sub>DD1</sub>	Positive Power Supply for DAC A and B	27	DGND2	Digital Ground 2
4	V <sub>SS1</sub>	Negative Power Supply for DAC A and B	28	DB6	Data Bit 6
5	VOA	DAC A Output	29	DB7	Data Bit 7
6	NC	No Connect	30	DB8	Data Bit 8
7	V <sub>REFLB</sub>	DAC B Voltage Reference Low Terminal	31	DB9	Data Bit 9
8	V <sub>REFHB</sub>	DAC B Voltage Reference High Terminal	32	A0	Address Input 0
9	V <sub>REFHA</sub>	DAC A Voltage Reference High Terminal	33	A1	Address Input 1
10	V <sub>REFLA</sub>	DAC A Voltage Reference Low Terminal	34	$\overline{CS}$	Chip Select, Active Low
11	R1	R1 Terminal (for Negative Reference)	35	R/ $\overline{W}$	Read/Write Mode Select
12	RCT	Center Tap Terminal (for Negative Reference)	36	DGND3	Digital Ground 3
13	R2	R2 Terminal (for Negative Reference)	37	V <sub>SS3</sub>	Negative Power Supply for Analog Switches
14	DV <sub>DD</sub>	Power Supply for Digital Circuits	38	V <sub>DD3</sub>	Positive Power Supply for Analog Switches
15	$\overline{LDAC}$	DAC Register Load, Active Low Level Sensitive	39	V <sub>REFLD</sub>	DAC D Voltage Reference Low Terminal
16	$\overline{RS}$	Reset Strobe	40	V <sub>REFHD</sub>	DAC D Voltage Reference High Terminal
17	MSB	MSB = 0, Reset to 000 <sub>H</sub> , MSB = 1, Reset to 200 <sub>H</sub>	41	V <sub>REFHC</sub>	DAC C Voltage Reference High Terminal
18	NS	No Connection	42	V <sub>REFLC</sub>	DAC C Voltage Reference Low Terminal
19	NS	No Connection	43	NC	No Connect
20	DB0	Data Bit 0	44	VOD	DAC D Output
21	DB1	Data Bit 1	45	V <sub>SS2</sub>	Negative Power Supply for DAC C and D
22	DGND1	Digital Ground 1	46	V <sub>DD2</sub>	Positive Power Supply for DAC C and D
23	DB2	Data Bit 2	47	VOC	DAC C Output
24	DB3	Data Bit 3	48	AGND2	Analog Ground for DAC C and D

\*AD5583 optimizes internal layout design to reduce die area so that all supply voltage pins are required to be connected externally. See Figure 5.



TIMING DIAGRAMS

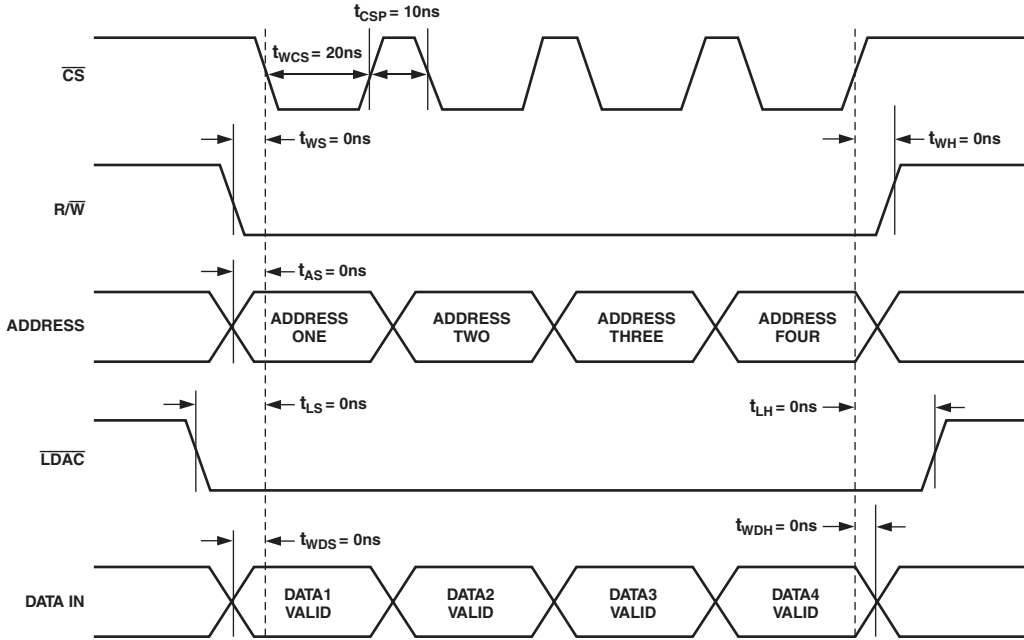


Figure 2a. Single Buffer Mode, Output Updated Individually,  $DV_{DD} = 5\text{ V}$

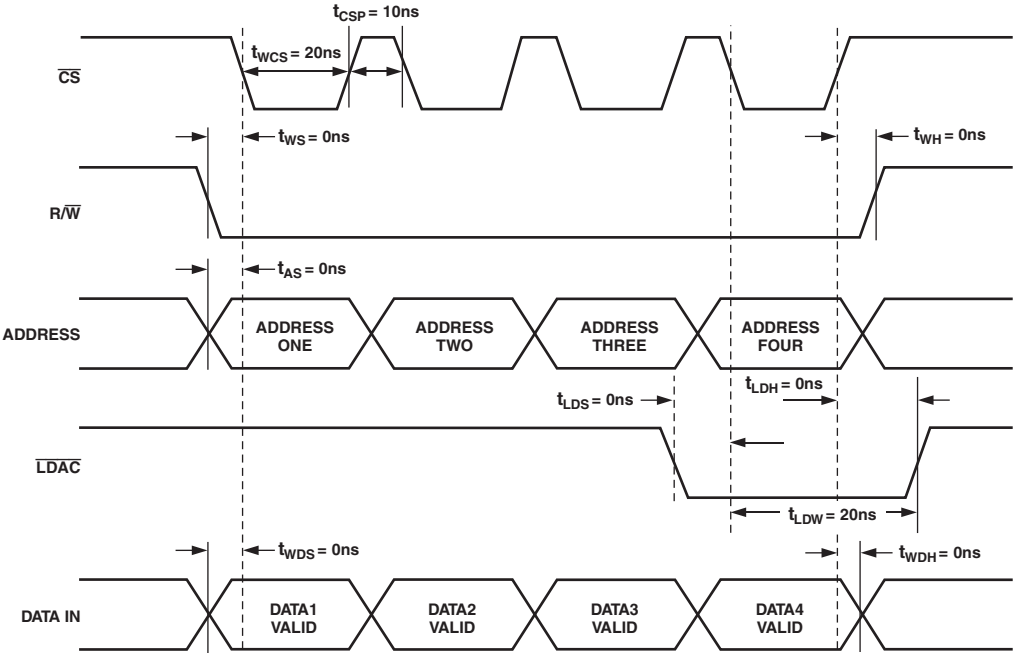


Figure 2b. Double Buffer Mode, Output Updated Simultaneously,  $DV_{DD} = 5\text{ V}$

# AD5582/AD5583

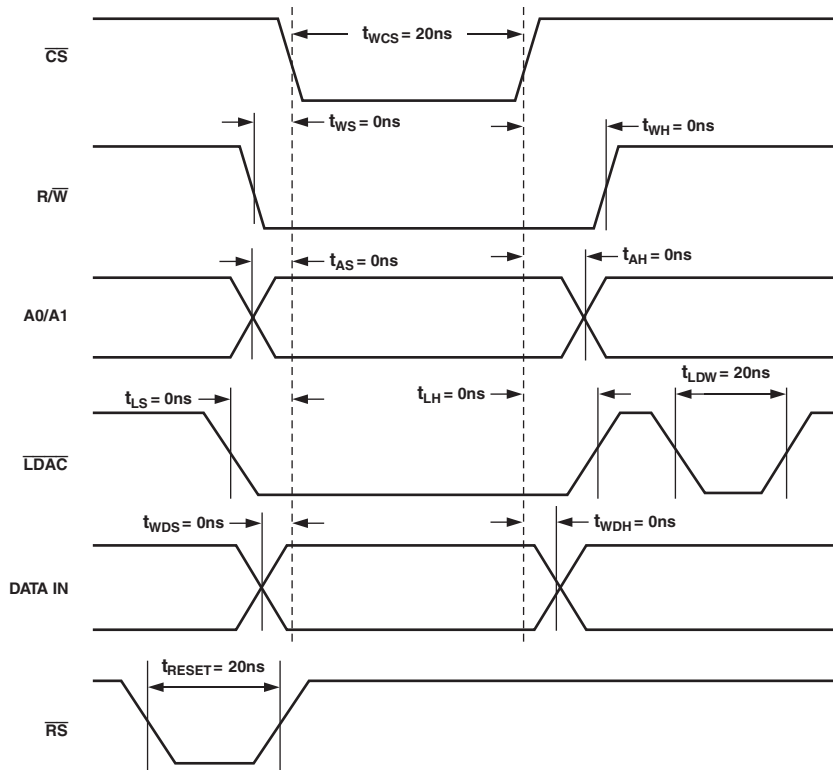


Figure 2c. Data Write (Input and Output Registers) Timing

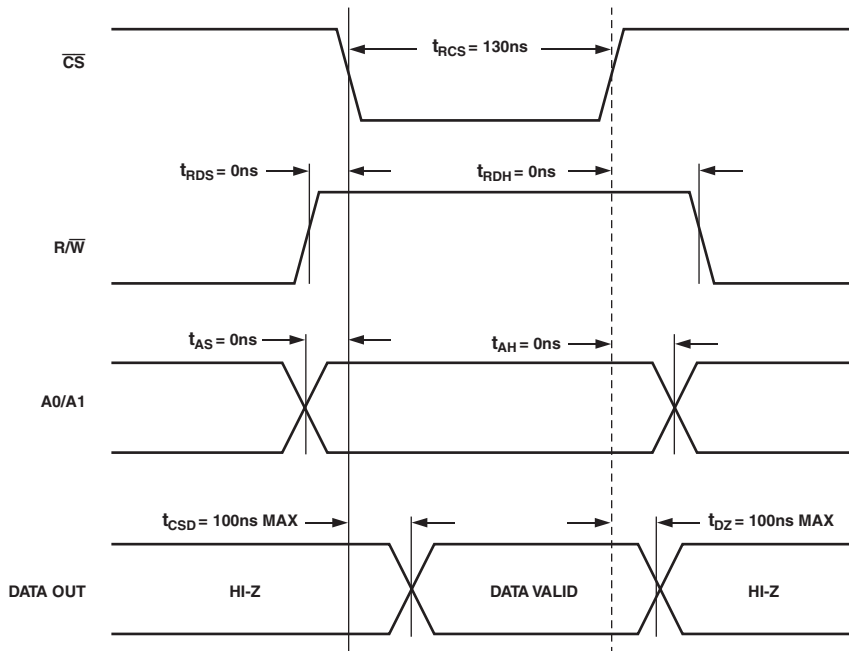
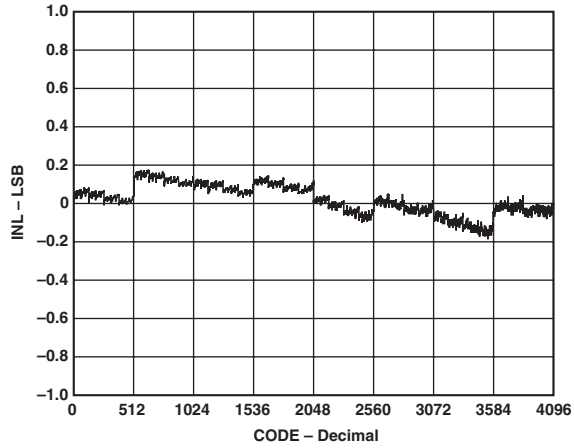
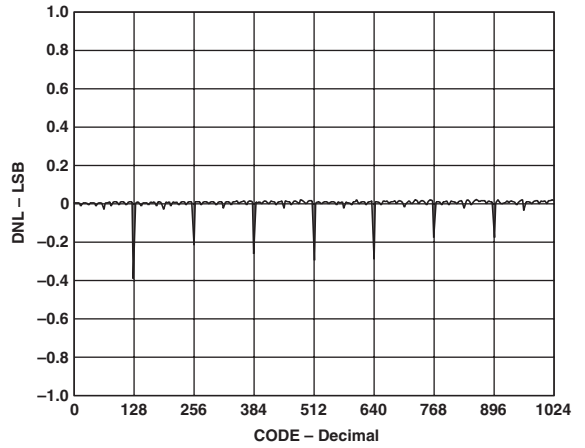


Figure 2d. Data Output (Read Timing)

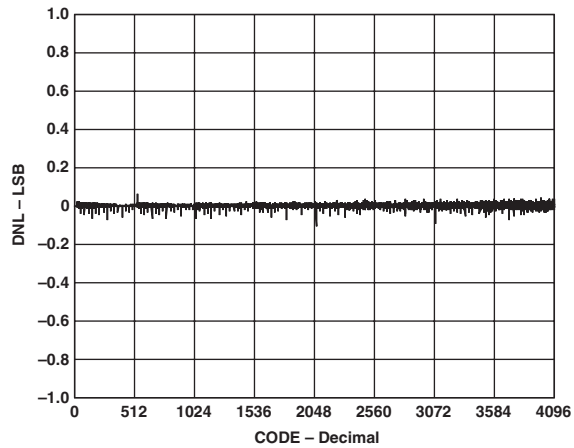
# Typical Performance Characteristics—AD5582/AD5583



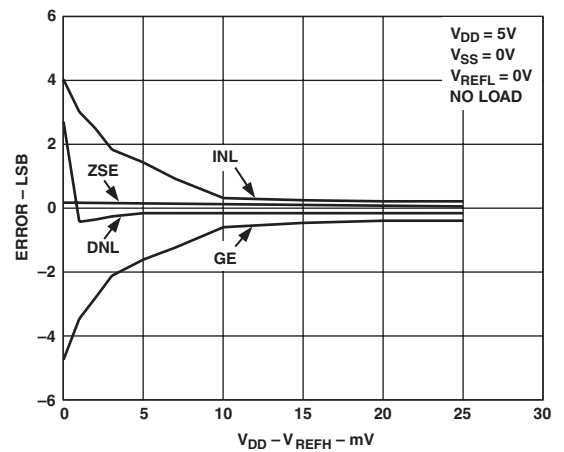
TPC 1. AD5582 Integral Nonlinearity Error



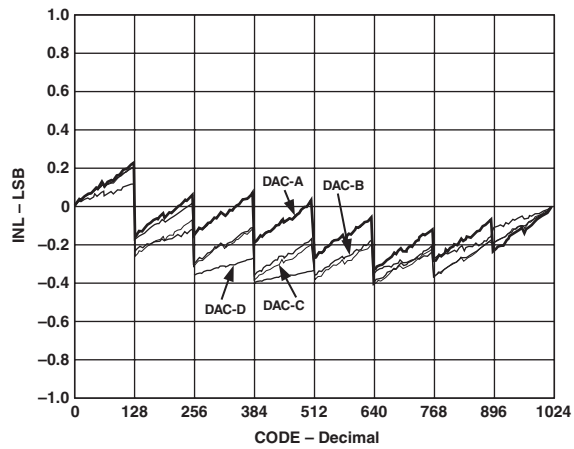
TPC 4. AD5583 Differential Nonlinearity Error



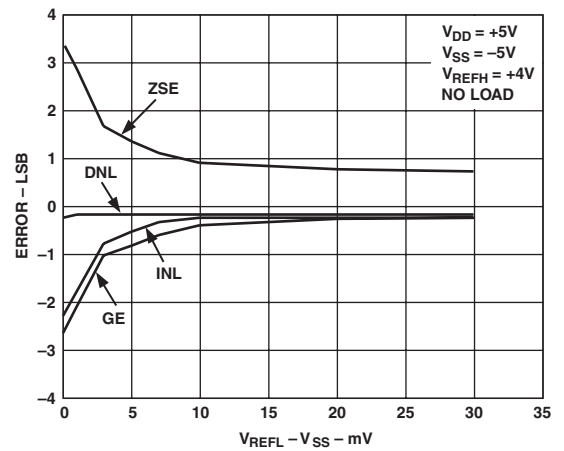
TPC 2. AD5582 Differential Nonlinearity Error



TPC 5. AD5582 INL, DNL, ZSE, and GE at Positive Rail-to-Rail Operation

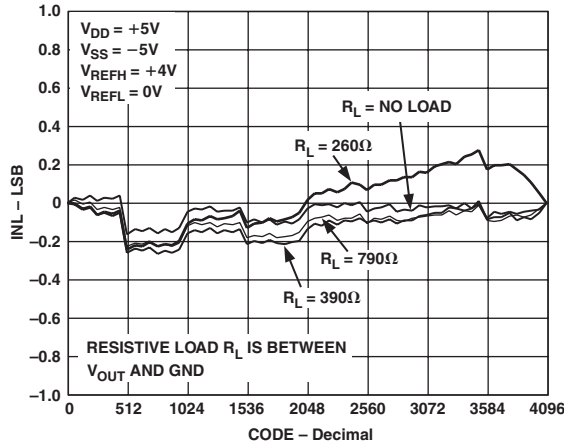


TPC 3. AD5583 Integral Nonlinearity Error

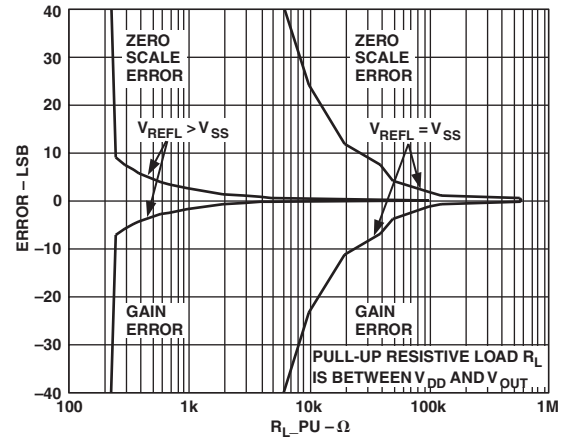


TPC 6. AD5582 INL, DNL, GE, and ZSE at Negative Rail-to-Rail Operation

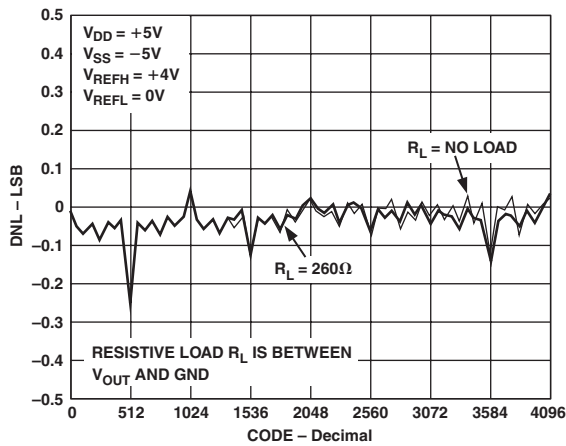
# AD5582/AD5583



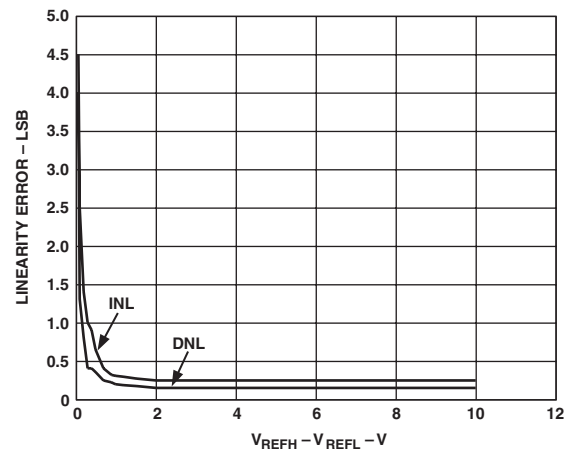
TPC 7. AD5582 INL at Various Resistive Loads



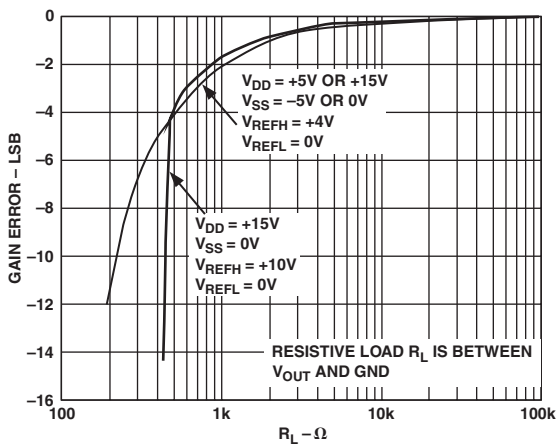
TPC 10. AD5582 Gain and Zero-Scale Error vs. Pull-Up Resistive Loads



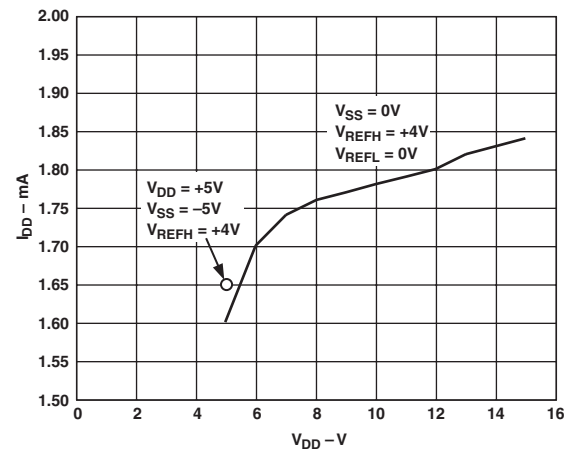
TPC 8. AD5582 DNL at Various Resistive Loads



TPC 11. AD5582 Linearity Errors vs. Differential Reference Ranges



TPC 9. AD5582 Gain Error vs. Resistive Load



TPC 12. AD5582 Supply Current vs. Supply Voltage













# AD5582/AD5583

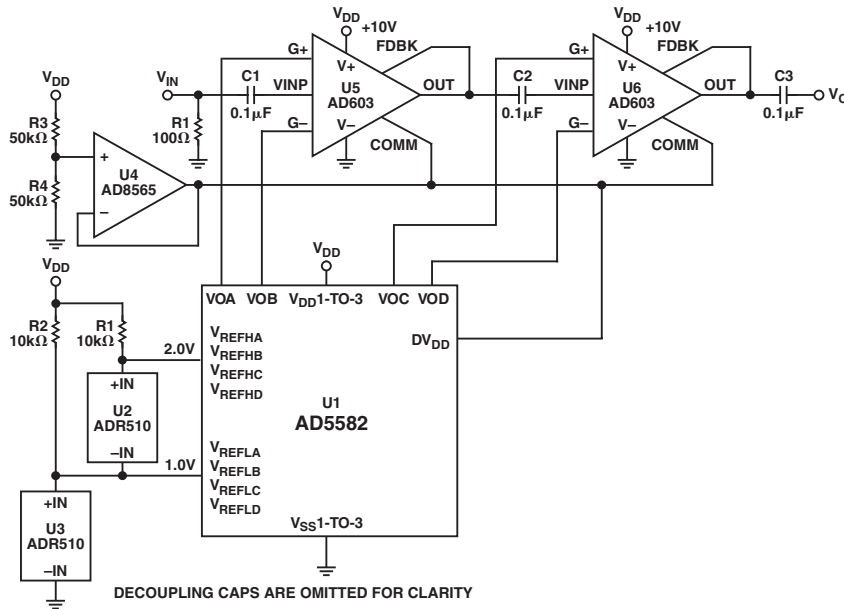


Figure 8. Programmable PGA

In this circuit, the inverting input of the op amp forces the  $V_O$  to be equal to the DAC output. The load current is then delivered by the supply via the N-Ch FET N1. U3 needs to be a rail-to-rail input type. With a  $V_{DD}$  of 5 V, this circuit can source a maximum of 200 mA at 4.096 V full scale, 100 mA at midscale, and 50 mA near zero-scale outputs. Higher current can be achieved with N1 in a larger package mounted on heat sink.

## Programmable PGA

The AD603 is a low noise, voltage controlled amplifier for use in RF and IF AGC (automatic gain control) systems. It provides accurate, pin selectable gains of  $-11$  dB to  $+31$  dB with a bandwidth of 90 MHz, or 9 dB to 51 dB with a bandwidth of 9 MHz. Any intermediate gain range may be arranged using one external resistor between Pin 5 and Pin 7. The input referred noise spectral density is only 1.3 nV/ $\sqrt{\text{Hz}}$  and power consumption is 125 mW at the recommended  $\pm 5$  V supplies.

The decibel gain is linear in dB, accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 M $\Omega$ ), low bias (200 nA) differential input; the scaling is 25 mV/dB, requiring a gain control voltage of only 1 V to span the central 40 dB of the gain range. An overrange and underrange of 1 dB is provided whatever the selected range. The gain control response time is less than 1 ms for a 40 dB change.

The differential gain control interface allows the use of either differential or single-ended positive or negative control voltages, where the common-mode range is  $-1.2$  V to  $+2.0$  V. The AD5582/AD5583 is ideally suited to provide the differential input range of 1 V within the common-mode range of 0 V to 2 V. To accomplish this, place  $V_{REFH}$  at 2.0 V and  $V_{REFL}$  at 1.0 V, then all 4096 V levels of the AD5582 will fall within the gain control range of the AD603. Please refer to the AD603 data sheet for further information regarding gain control, layout, and general operation.

## 18-Bit Bipolar DAC

The multichannel, high accuracy, and differential reference capabilities of the AD5582 make it well suited for an enhanced resolution configuration. Three of the four channels of the AD5582 can be cascaded to form one high resolution DAC, as shown in Figure 9, that has a potential of much higher bit resolution than a single channel.

As DAC A and B are moving together to form the coarse adjustment, their outputs are used as the differential references for DAC C. DAC C provides 12-bit fine adjustment but its full adjustment range C is bounded by these differential references programmed by DAC A and B. As a result, the differential references range dictates the final resolution of this circuit. To keep INL and DNL within 1 LSB error at 12-bit resolution (see TPC 11), DAC C differential references are set to 156.25 mV. With  $V_{REFH}/V_{REFL}$  of  $\pm 5.000$  V, the codes of DAC A and B must always be maintained at 64 steps apart when DAC A and B are moving together. The equation that yields 18-bit resolution becomes:

$$V_O = \frac{D_C}{4096} \left[ \begin{array}{l} V_{REF} \left( \frac{D_A}{2048} - 1 \right) \\ -V_{REF} \left( \frac{D_B}{2048} - 1 \right) \end{array} \right] + V_{REF} \left( \frac{D_B}{2048} - 1 \right) \quad (6)$$

where  $D_A$ ,  $D_B$ , and  $D_C$  are the decimal equivalent of the data bits of DAC A, B, and C, respectively. The benefit of achieving such high resolution comes with an expense of programming complexity, as shown in Table II. Notice D is the decimal equivalent of the 18-bit data bit, which must be translated to the equivalent  $D_A$ ,  $D_B$ , and  $D_C$  settings. It can be shown that D is equal to:

$$D = \frac{D_C(D_A - D_B)}{64} + 64D_B - 2^{18} \quad (7)$$

and the condition of

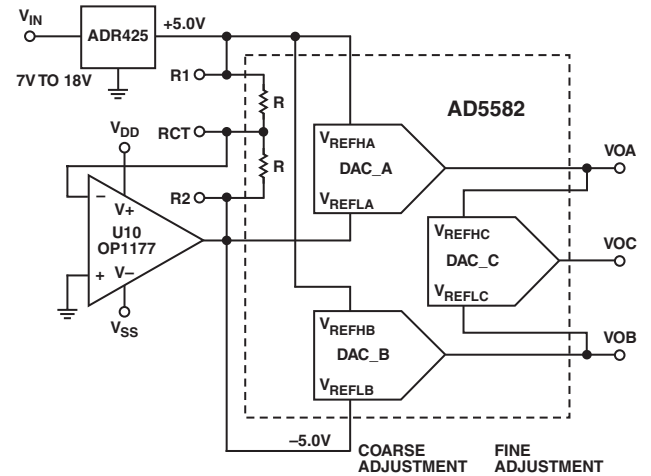
$$D_A = D_B + 64 \quad (8)$$

must always be applied.

**Table II. 18-Bit DAC Programming Example**

D	D <sub>A</sub>	D <sub>B</sub>	D <sub>C</sub>	V <sub>O</sub>
0	64	0	0	-5.00000
2048	64	0	2048	-4.92188
61440	1024	960	0	-2.65625
63488	1024	960	2048	-2.57813
126976	2048	1984	0	-0.15625
129024	2048	1984	2048	-0.07813
257984	4095	4031	0	4.84375
260032	4095	4031	2048	4.920654

Finally, an 18-bit bipolar DAC is formed with DAC A/DAC B controlling the coarse 6-bit and DAC C providing the fine 12-bit adjustment within each coarse step. Notice that this DAC provides  $2^{18}$  numbers of steps of adjustment; the precision remains at 12-bits accurate because of the limitation of the DAC C differential references. As a result, this circuit is suitable for those applications that require 18 bits of adjustment while absolute accuracy is not required.

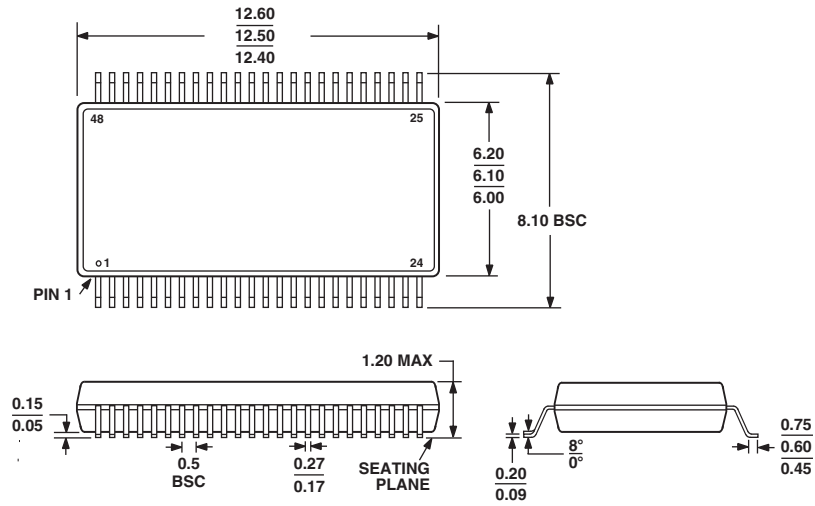


*Figure 9. 18-Bit Bipolar DAC*

## OUTLINE DIMENSIONS

### 48-Lead Thin Shrink Small Outline Package (TSSOP) (RU-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153ED