

## Radiation Hardened Octal Three-State Transparent Latch

January 1996

### Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96725 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose ..... >300K RAD (Si)
- Single Event Upset (SEU) Immunity: <math>1 \times 10^{-10}</math> Errors/Bit/Day (Typ)
- SEU LET Threshold ..... >100 MEV-cm<sup>2</sup>/mg
- Dose Rate Upset ..... >10<sup>11</sup> RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability ..... >10<sup>12</sup> RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range ..... -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range ..... 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay ..... 18ns (Max), 12ns (Typ)

### Description

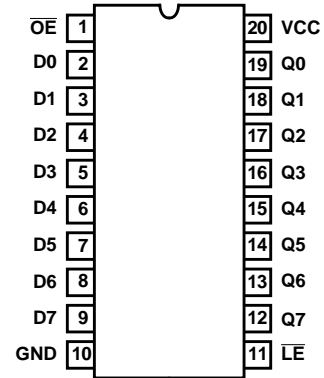
The Intersil ACTS573MS is a Radiation Hardened Octal Transparent Latch with an active low output enable. The outputs are transparent to the inputs when the latch enable ( $\overline{LE}$ ) is High. When the latch goes low the data is latched. The output enable controls the three-state outputs. When the output enable pins ( $\overline{OE}$ ) are high the output is in a high impedance state. The latch operation is independent of the state of output enable.

The ACTS573MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic family.

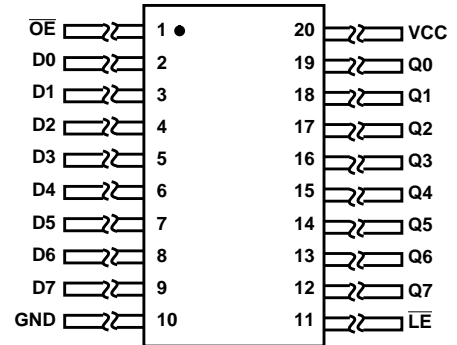
The ACTS573MS is supplied in a 20 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line package (D suffix).

### Pinouts

20 LEAD CERAMIC DUAL-IN-LINE  
MIL-STD-1835 DESIGNATOR,  
CDIP2-T20, LEAD FINISH C  
TOP VIEW



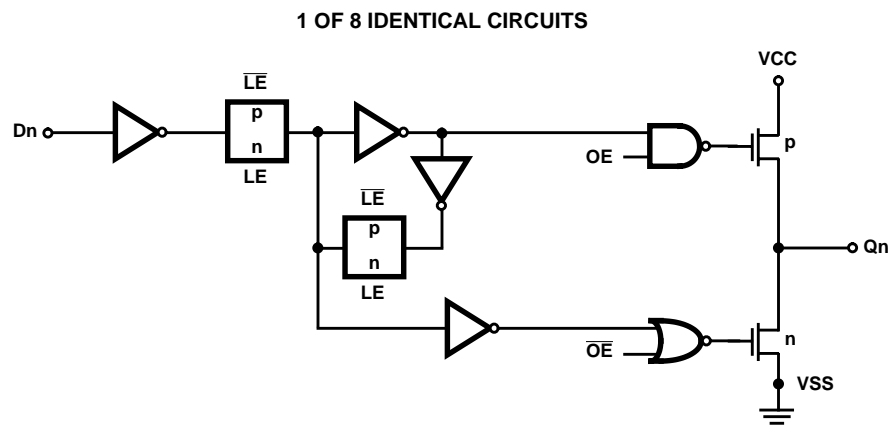
20 LEAD CERAMIC FLATPACK  
MIL-STD-1835 DESIGNATOR,  
CDFP4-F20, LEAD FINISH C  
TOP VIEW



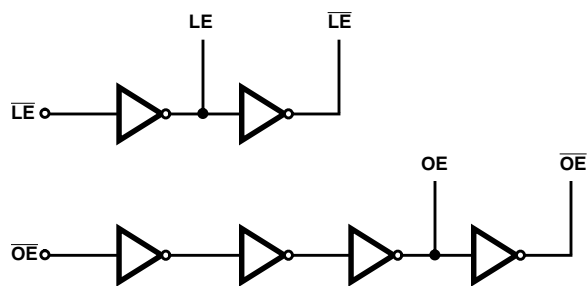
### Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9672501VRC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead SBDIP
5962F9672501VXC	-55°C to +125°C	MIL-PRF-38535 Class V	20 Lead Ceramic Flatpack
ACTS573D/Sample	25°C	Sample	20 Lead SBDIP
ACTS573K/Sample	25°C	Sample	20 Lead Ceramic Flatpack
ACTS573HMSR	25°C	Die	Die

Functional Diagram



COMMON CONTROLS



TRUTH TABLE

OE	LE	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

NOTE: L = Low Logic Level, H = High Logic Level, X = Don't Care, Z = High Impedance, l = Low Voltage Level Prior to High-to-Low Latch Enable Transition, h = High Voltage Level Prior to High-to-Low Latch Enable Transition.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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# ACTS573MS

## Die Characteristics

### DIE DIMENSIONS:

102 mils x 102 mils  
2,600mm x 2,600mm

### METALLIZATION:

Type: AlSi  
Metal 1 Thickness:  $7.125\text{k}\text{\AA} \pm 1.125\text{k}\text{\AA}$   
Metal 2 Thickness:  $9\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

### GLASSIVATION:

Type:  $\text{SiO}_2$   
Thickness:  $8\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

### WORST CASE CURRENT DENSITY:

$< 2.0 \times 10^5 \text{ A/cm}^2$

### BOND PAD SIZE:

$> 4.3 \text{ mils} \times 4.3 \text{ mils}$   
 $> 110\mu\text{m} \times 110\mu\text{m}$

## Metallization Mask Layout

