

# 9324 93L24

## 5-BIT COMPARATOR

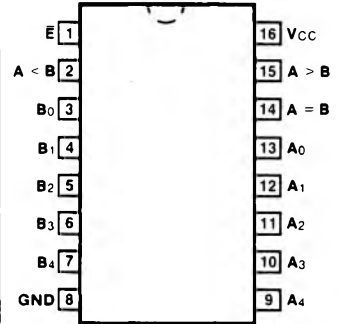
**DESCRIPTION** — The '24 expandable comparators provide comparison between two 5-bit words and give three outputs — "less than", "greater than" and "equal to". A HIGH on the active LOW Enable Input forces all three outputs LOW.

- **THREE SEPARATE OUTPUTS — A < B, A > B, A = B**
- **EASILY EXPANDABLE**
- **ACTIVE LOW ENABLE INPUT**

**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	9324PC, 93L24PC		9B
Ceramic DIP (D)	A	9324DC, 93L24DC	9324DM, 93L24DM	6B
Flatpak (F)	A	9324FC, 93L24FC	9324FM, 93L24FM	4L

**CONNECTION DIAGRAM**  
PINOUT A



6

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

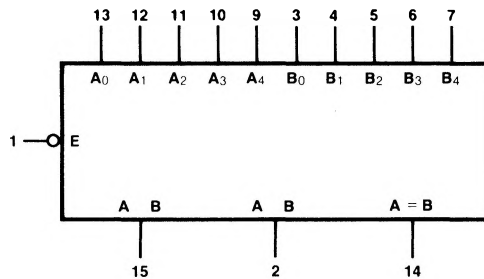
PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW
$\bar{E}$	Enable Input (Active LOW)	2.0/2.0	1.0/0.5
A <sub>0</sub> — A <sub>4</sub>	Word A Parallel Inputs	2.0/2.0	1.0/0.5
B <sub>0</sub> — B <sub>4</sub>	Word B Parallel Inputs	2.0/2.0	1.0/0.5
A < B	A Less than B Output (Active HIGH)	20/10	10/5.0 (3.0)
A > B	A Greater than B Output (Active HIGH)	20/10	10/5.0 (3.0)
A = B	A Equal to B Output (Active HIGH)	20/10	10/5.0 (3.0)

**FUNCTIONAL DESCRIPTION** — The '24 5-bit comparators use combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable Input ( $\bar{E}$ ).

Tying the  $A > B$  output from one device into an  $A$  input on another device and the  $A < B$  output into the corresponding  $B$  input permits easy expansion.

The  $A_4$  and  $B_4$  inputs are the most significant inputs and  $A_0, B_0$  the least significant. Thus if  $A_4$  is HIGH and  $B_4$  is LOW, the  $A > B$  output will be HIGH regardless of all other inputs except  $E$ .

### LOGIC SYMBOL



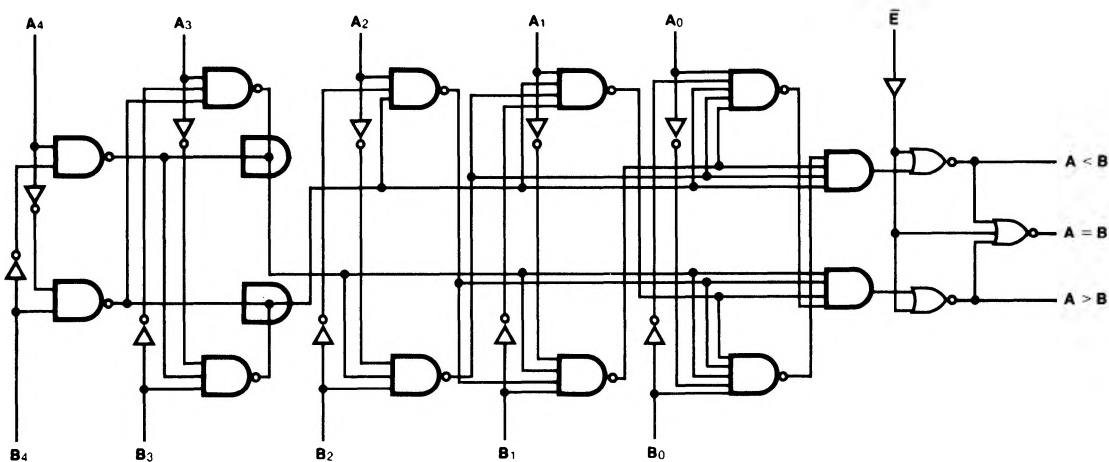
V<sub>CC</sub> = Pin 16  
GND = Pin 8

### TRUTH TABLE

INPUTS			OUTPUTS		
$\bar{E}$	A <sub>n</sub>	B <sub>n</sub>	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word B > Word A		H	L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## LOGIC DIAGRAM



## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		Min	Max	Min	Max		
$I_{CC}$	Power Supply Current	81		21		mA	$V_{CC} = \text{Max}$

AC CHARACTERISTICS:  $V_{CC} = +5.0 \text{ V}$ ,  $T_A = +25^\circ \text{ C}$  (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		UNITS	CONDITIONS
		$C_L = 15 \text{ pF}$		$C_L = 15 \text{ pF}$			
		Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\bar{E}$ to $A = B$	14		32		ns	Figs. 3-1, 3-4
		14		35			
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_2$ to $A > B$	25		54		ns	Figs. 3-1, 3-5
		22		75			
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_2$ to $A < B$	26		70		ns	Figs. 3-1, 3-4
		21		77			
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_2$ to $A = B$	30		100		ns	Figs. 3-1, 3-20
		32		102			