

PIN NAMES	DESCRIPTION	HIGH/LOW	HIGH/LOW	
Ēa, Ēb	Enable Inputs (Active LOW)	1.0/1.0	0.5/0.25	
A0a, A1a, A0b, A1b	Address Inputs	1.0/1.0	0.5/0.25	
$\left. \begin{array}{c} \overline{O}_{0a} - \overline{O}_{3a} \\ \overline{O}_{0b} - \overline{O}_{3b} \end{array} \right\}$	Decoder Outputs (Active LOW)	20/10	10/5.0 (3.0)	
			L	

**FUNCTIONAL DESCRIPTION** — The '21 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in the logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

## 

INPUTS			OUTPUTS				
Ē	Ao	<b>A</b> 1	Ō0	Ōı	Ō2	$\overline{O}_3$	
L	L	L	L	н	Н	н	
L	н	L	н	L	н	н	
L	L	н	н	н	L	н	
L	н	н	н	н	н	L	H = HIGH Voltage Leve
н	X	Х	н	н	н	Н	L = LOW Voltage Level X = Immaterial

## LOGIC DIAGRAM



## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX		3L	UNITS	CONDITIONS
•••••••		Min	Max	Min	Max	••••••	
lcc	Power Supply Current		50		13.2	mA	V <sub>CC</sub> = Max

## AC CHARACTERISTICS: $V_{CC} = +5.0 V$ , $T_A = +25^{\circ}C$ (See Section 3 for waveforms and load configurations)

		93XX	<b>93L</b> C <sub>L</sub> = 15 pF		UNITS	CONDITIONS
SYMBOL	PARAMETER	C <sub>L</sub> = 15 pF				
		Min Max	Min	Max		
tPLH tPHL	Propagation Delay $A_n$ to $\overline{O}_n$	20 21		50 65	ns	Figs. 3-1, 3-20
tPLH tPHL	Propagation Delay Ē to Ōn	14 18		40 52	ns	Figs. 3-1, 3-5