DATA SHEET

80CL410/83CL410

Low voltage/low power single-chip 8-bit microcontroller with I^2C

Product specification

1995 Jan 20

IC20 Data Handbook

Philips Semiconductors

PHILIPS

Low voltage/low power single-chip 8-bit microcontroller with I²C

80CL410/83CL410

DESCRIPTION

The 80CL410/83CL410 (hereafter generically referred to as 8XCL410) is manufactured in an advanced CMOS process that allows the part to operate at supply voltages down to 1.8V and oscillator frequencies down to DC. The 8XCL410 has the same instruction set as the 80C51.

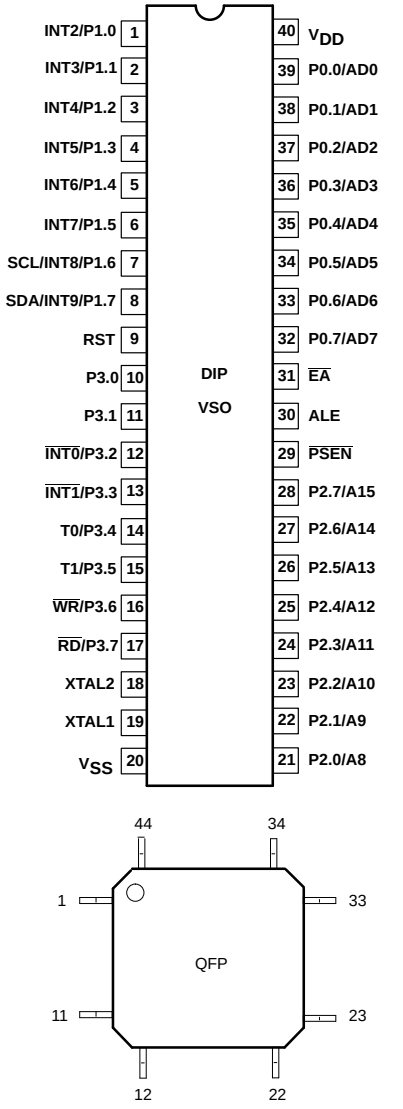
The 8XCL410 features a 4k byte ROM (83CL410), 128 bytes RAM (both ROM and RAM are externally expandable to 64k bytes), four 8-bit ports, two 16-bit timer/counters, an I²C serial interface, a thirteen source, two priority level nested interrupt structure, and on-chip oscillator circuitry suitable for quartz crystal, ceramic resonator, RC, or LC.

The 8XCL410 has two reduced power modes that are the same as those on the standard 80C51. The special reduced power feature of this part is that it can be stopped and then restarted. Running from an external clock source, the clock can be stopped and after a period of time restarted. The 8XCL410 will resume operation from where it was when the code stopped with no loss of internal state, RAM contents, or Special Function Register contents. If the internal oscillator is used the part cannot be stopped and started, but the power-down mode, which can be terminated via an interrupt, can be used to achieve similar power savings and then restart without loss of on-chip RAM and Special Function Register values.

FEATURES

- Single supply voltage 1.8V to 6.0V
- Frequency from DC to 12MHz
- 80C51 based architecture
  - 4k × 8 ROM (64k external)
  - 128 × 8 RAM (64k external)
  - Four 8-bit I/O ports
  - Two 16-bit timer/counters
  - A thirteen-source, two-level, nested priority interrupt structure
  - 10 external interrupts
- Fully static 80C51 CPU
- I²C Serial Interface
- Two power control modes
  - Idle mode
  - Power-down mode – can be terminated by reset or external interrupt
- Wake-up via external interrupts at port 1
- Single supply voltage 1.8V to 6.0V
- Frequency range of DC to 12MHz
- On-chip oscillator (quartz crystal, ceramic resonator, RC, LC)
- Very low power consumption
- Operating temperature range: –40 to +85°C

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP PIN FUNCTIONS.

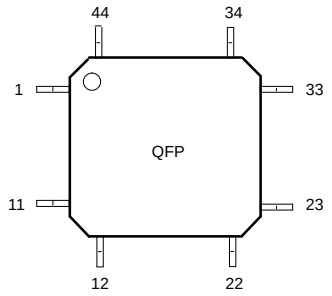
ORDERING CODE

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER[1]		TEMPERATURE °C AND PACKAGE	FREQUENCY	Drawing Number
ROMless	ROM	ROMless	ROM			
P80CL410HFP	P83CL410HFP	P80CL410HF N	P83CL410HF N	–40 to +85, 40-Pin Plastic Dual In-line Package	32kHZ to 12MHz	SOT129-1
P80CL410HFT	P83CL410HFT	P80CL410HF D	P83CL410HF D	–40 to +85, 40-Pin Plastic Very Small Outline Package	32kHZ to 12MHz	SOT158-1
	P83CL410HFH			–40 to +85, 44-Pin Plastic Quad Flat Pack	32kHZ to 12MHz	SOT307-2

NOTE:
1. Parts ordered by the Philips North America part number will be marked with the Philips part marking.

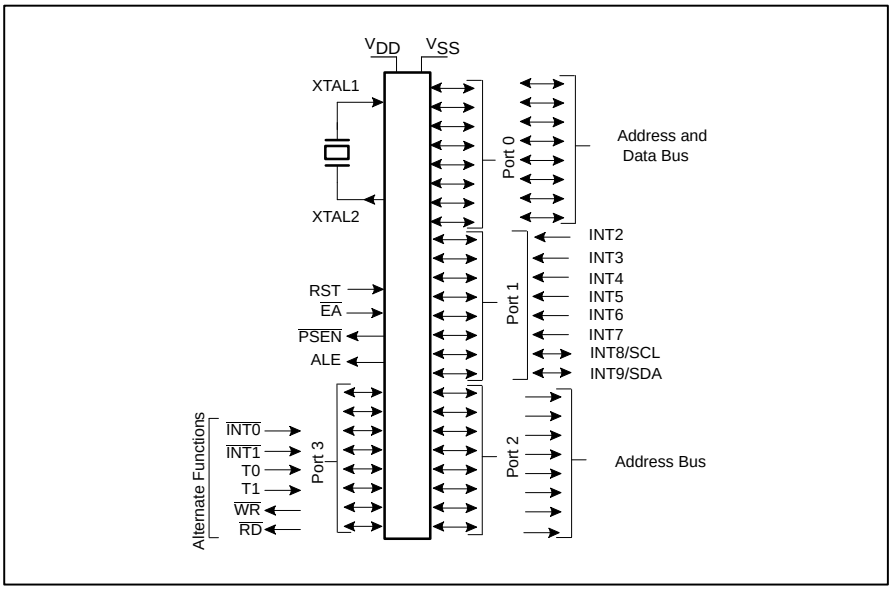
For emulation purposes, the P85CL000 (Piggyback version) with 256 bytes of RAM is recommended.

PLASTIC QUAD FLAT PACK PIN FUNCTIONS

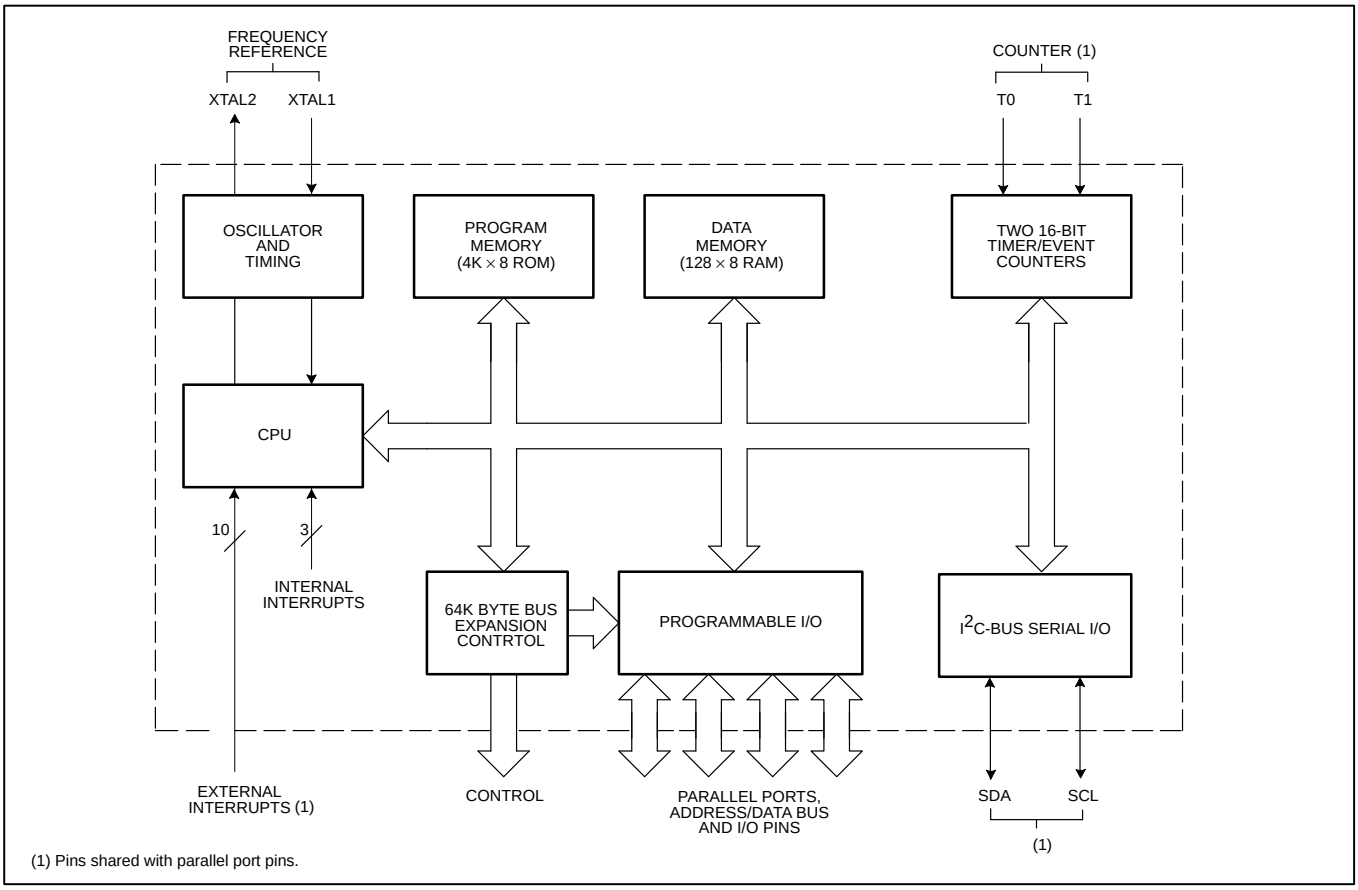


Pin	Function	Pin	Function
1	P1.5/INT7	23	P2.5/A13
2	P1.6/INT8/SCL	24	P2.6/A14
3	P1.7/INT9/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0	27	ALE
6	NC	28	NC
7	P3.1	29	$\overline{EA}$
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{DD}
17	NC	39	NC
18	P2.0/A8	40	P1.0/INT2
19	P2.1/A9	41	P1.1/INT3
20	P2.2/A10	42	P1.2/INT4
21	P2.3/A11	43	P1.3/INT5
22	P2.4/A12	44	P1.4/INT6

LOGIC SYMBOL



BLOCK DIAGRAM



(1) Pins shared with parallel port pins.

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	QFP	DIL40/ VSO40		
V_{SS}	16	20	I	**Ground:** 0V reference.
V_{DD}	38	40	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	30–37	39–32	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	40–44 1–3	1–8	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Additional functions include:
		7	I/O	**SCL (P1.6):** I^2C serial bus clock.
		8	I/O	**SDA (P1.7):** I^2C serial bus data.
		1–8	I	**INT2–INT9 (P1.0–P1.7):** Additional external interrupts.
P2.0–P2.7	18–25	21–28	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	5, 7–13	10–17	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	8	12	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt 0
	9	13	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	10	14	I	**T0 (P3.4):** Timer 0 external input
	11	15	I	**T1 (P3.5):** Timer 1 external input
	12	16	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	13	17	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
RST	4	9	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{DD}.
ALE	27	30	O	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
$\overline{\text{PSEN}}$	26	29	O	**Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}$	29	31	I	**External Access Enable:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H to 0FFFH. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH.
XTAL1	15	19	I	**Crystal 1:** Input to the inverting oscillator amplifier and input for an external clock source.
XTAL2	14	18	O	**Crystal 2:** Output from the inverting oscillator amplifier.

Table 1. 8XCL410 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data pointer (2 bytes):										
DPH	High byte	83H									00H
DPL	Low byte	82H									00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP0*#	Interrupt priority 0	B8H	–	–	PS1	–	PT1	PX1	PT0	PX0	xx000000B
			FF	FE	FD	FC	FB	FA	F9	F8	
IP1*#	Interrupt priority 1	F8H	PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2	00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IEN0*#	Interrupt enable 0	A8H	EA	–	ES1	–	ET1	EX1	ET0	EX0	00H
			EF	EE	ED	EC	EB	EA	E9	E8	
IEN1*#	Interrupt enable 1	E8H	EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2	00H
			C7	C6	C5	C4	C3	C2	C1	C0	
IRQ1*#	Interrupt request flag	C0H	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2	00H
IX1#	Interrupt polarity	E9H									00H
P0*	Port 0	80H	87	86	85	84	83	82	81	80	FFH
P1*	Port 1	90H	97	96	95	94	93	92	91	90	FFH
P2*	Port 2	A0H	A7	A6	A5	A4	A3	A2	A1	A0	FFH
P3*	Port 3	B0H	B7	B6	B5	B4	B3	B2	B1	B0	FFH
PCON	Power control	87H	SMOD	–	–	–	GF1	GF0	PD	IDL	0xxx0000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
S1ADR#	Slave address	DBH									00H
			DF	DE	DD	DC	DB	DA	D9	D8	
S1CON*#	Serial control	D8H	–	ENS1	STA	STO	SI	AA	CR1	CR0	x0000000B
S1DAT#	Serial data	DAH									00H
S1STA#	Serial status	D9H									11111000B
SP	Stack pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer/counter control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TMOD	Timer/counter mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
TH0	Timer 0 high byte	8CH									00H
TH1	Timer 1 high byte	8DH									00H
TL0	Timer 0 low byte	8AH									00H
TL1	Timer 1 low byte	8BH									00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.

PORT OPTIONS

The pins of port 1 (not P1.6/SCL or P1.7/SDA), port 2, and port 3 may be individually configured with one of the following port options (see Figure 1):

Option 1: **Standard Port**—quasi-bidirectional I/O with pull-up. The strong booster pull-up p1 is turned on for two oscillator periods after a 0-to-1 transition in the port latch. See Figure 1(a).

Option 2: **Open Drain**—quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor. See Figure 1(b).

Option 3: **Push-Pull**—output with drive capability in both polarities. Under this option, pins can only be used as outputs. See Figure 1(c).

The definition of port options for port 0 is slightly different.

Two cases have to be examined. First, accesses to external memory ($\overline{EA}$ = 0 or access above the built-in memory boundary), and second, I/O accesses.

External Memory Accesses

Option 1: True 0 and 1 are written as address to the external memory (strong pull-up is used).

Option 2: An external pull-up resistor is needed for external accesses.

Option 3: Not allowed for external memory accesses as the port can only be used as output.

I/O Accesses

Option 1: When writing a 1 to the port latch, the strong pull-up p1 will be on for two oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2: Open drain—quasi-bidirectional I/O with n-channel open drain output. Use as an output requires the connection of an external pull-up resistor. See Figure 1(c).

Option 3: Push-Pull—output with drive capability in both polarities. Under this option, pins can only be used as outputs.

Individual mask selection of the post-reset state is available on any of the above pins. Make your selection by appending “S” or “R” to option 1, 2, or 3 above (e.g., 1S for a standard I/O to be set after RESET or 2R for an open-drain I/O to be reset after RESET.

Option S: **Set**—after reset, this pin will be initialized High.

Option R: **Reset**—after reset, this pin will be initialized Low.

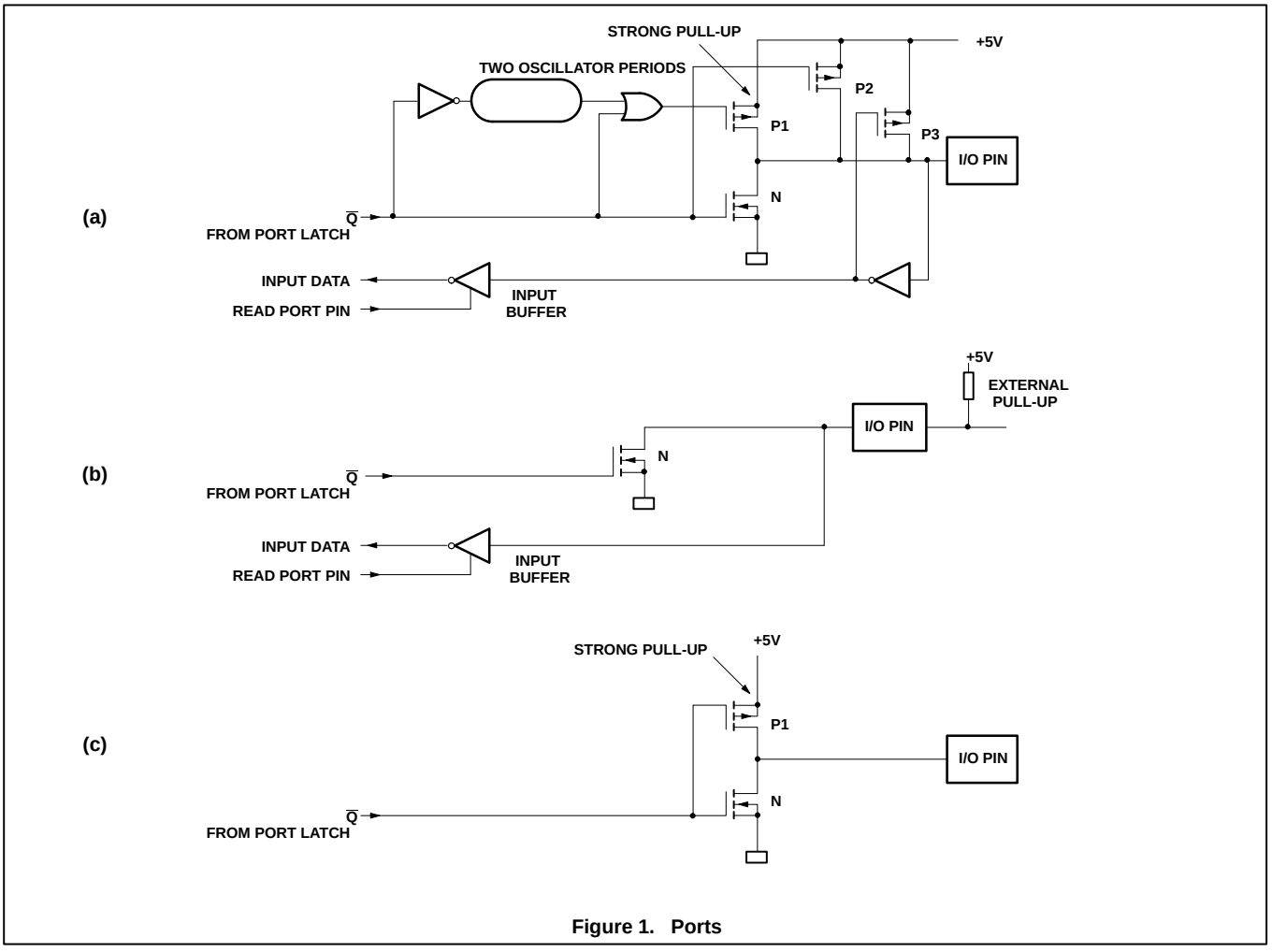


Figure 1. Ports

POWER-DOWN MODE

The instruction setting PCON.1 is the last executed prior to going into the power-down mode. In power-down mode, the oscillator is stopped. The contents of the the on-chip RAM and SFRs are preserved. The port pins output the values held by their respective SFRs. ALE and $\overline{PSEN}$ are held low.

In the power-down mode, V_{DD} may be reduced to minimize power consumption. However, the supply voltage must not be reduced until the power-down mode is active, and must be restored before the hardware reset is applied and frees the oscillator. Reset must be held active until the oscillator has restarted and stabilized.

From the power-down mode the part can be restarted by using either the wake-up mode or the Reset Mode.

Wake-Up Mode

Setting both PD and IDL bits in the PCON register forces the controller into the power-down mode. Setting both bits enable the controller to be woken-up from the power-down mode via either an enabled external interrupt INT2–INT9, or a reset operation.

An external interrupt for an enabled interrupt INT2–INT9 at port 1 starts both the oscillator and the delay counter. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods after the interrupt is detected. This is controlled by the on-chip delay counter. After this, the PD flag will be reset, the controller is now in the Idle mode and the interrupt will be handled in the normal way.

Reset Mode

Setting only the PD bit in the PCON register again forces the controller into the power-down mode, but in this case it can only be restored to normal operation with a direct reset operation.

To restore normal operation, the RESET pin has to be kept High for a minimum of 24 oscillator periods. The on-chip delay counter is inactive. The user has to insure that the oscillator is stable before any operation is attempted. Figure 2 illustrates the two possibilities for wake-up.

IDLE MODE

The instruction that sets PCON.0 is the last instruction executed before going into idle mode. In idle mode, the internal clock is stopped for the CPU, but not for the interrupt, timer, and serial port functions. The CPU status is preserved along with the stack pointer, program counter, program status word and accumulator. The RAM and all other registers maintain their data during idle mode. The port pins retain the logical states they held at idle mode activation. ALE and $\overline{PSEN}$ hold at the logic high level.

There are two methods used to terminate the idle mode. Activation of any interrupt will cause PCON to be cleared by hardware; terminating idle mode. The interrupt is serviced, and following the instruction RETI, the next instruction to be executed will be the one following the instruction that put the device in the the idle mode.

Flag bits GF0 and GF1 can be used to determine whether the interrupt was received during normal execution or idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.

The second method of terminating the idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for only two machine cycles to complete the reset operation. Reset redefines all SFRs, but does not affect the state of the on-chip RAM.

The status of the external pins during idle and power-down mode is shown in Table 2. If the power-down mode is activated while accessing external memory, port data held in the special function register P2 is restored to port 2. If the data is a logic 1, the port pin is held high during the power-down mode.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Floating	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Floating	Data	Data	Data

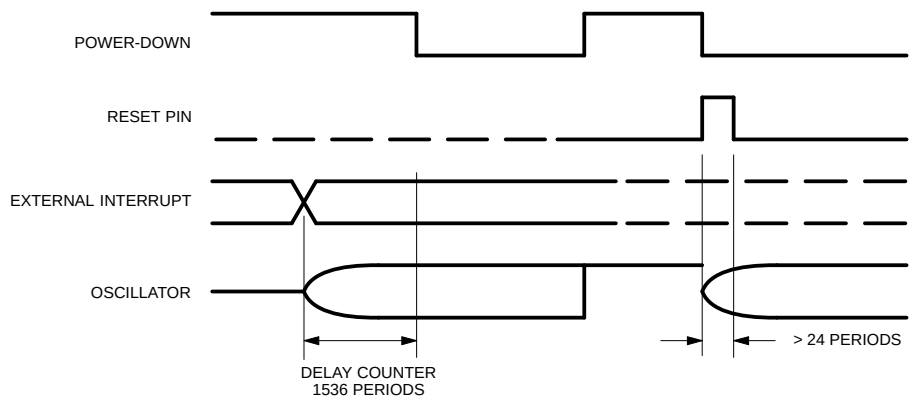


Figure 2. Wake-Up Operation

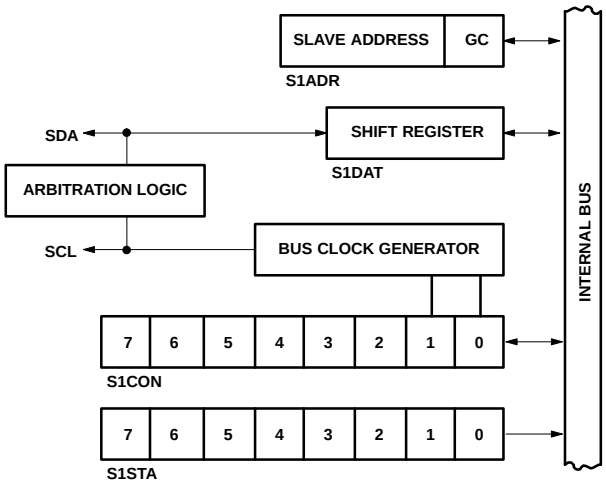


Figure 3. Serial I/O

I²C-BUS SERIAL I/O

The serial port supports the twin line I²C-bus. The I²C-bus consists of a data line (SDA) and a clock line (SCL). These lines also function as I/O port lines P1.7 and P1.6 respectively. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware. The I²C-bus serial I/O has complete autonomy in byte handling and operates in four modes:

– Master transmitter
– Master receiver
– Slave transmitter
– Slave receiver

These functions are controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR the slave address register. Slave address recognition is performed by hardware.

S1CON (D8H)
Serial control register

CR2	ENS1	STA	STO	SI	AA	CR1	CR0

CR0, CR1, CR2

These three bits determine the serial clock frequency when SIO is in a master mode.

AA

Assert acknowledge bit. When the AA flag is set, an acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when:

– own slave address is received
– general call address is received (S1ADR.0 = 1)
– data byte received while device is programmed as master
– data byte received while device is selected slave

With AA = 0, no acknowledge will be returned. Consequently, no interrupt is requested when the “own slave address” or general call address is received.

SI

SIO interrupt flag. When the SI flag is set, an acknowledge is returned after any one of the following conditions:

– a start condition is generated in master mode
– own slave address received during AA = 1
– general call address received while S1ADR.0 and AA = 1
– data byte received or transmitted in master mode (even if arbitration is lost)
– data byte received or transmitted as selected slave
– stop or start condition received as selected slave receiver or transmitter

STO

STOP flag. With this bit set while in master mode, a STOP condition is generated. When a STOP condition is detected on the bus, the SIO hardware clears the STO flag. In the slave mode, the STO flag may also be set to recover from an error condition. In this case, no STOP condition is transmitted to the I²C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases SDA and SCL. The SIO then switches to the “not addressed” slave receiver mode. The STO flag is automatically cleared by hardware.

STA

START flag. When the STA bit is set in slave mode, the SIO hardware checks the status of the I²C-bus and generates a START condition if the bus is free. If STA is set while the SIO is in master mode, SIO transmits a repeated START condition.

ENS1

When ENS1 = 0, the SIO is disabled. The SDA and SCL outputs are in a high-impedance state; P1.6 and P1.7 function as open drain ports.

When ENS1 = 1, the SIO is enabled. The P1.6 and P1.7 port latches must be set to logic 1.

S1STA (D9H)
Status register

SC4	SC3	SC2	SC1	SC0	0	0	0

S1STA is an 8-bit read-only special function register. S1STA.3–S1STA.7 hold a status code. S1STA.0–S1STA.2 are held LOW. The contents of S1STA may be used as a vector to a service routine. This optimizes response time of the software and consequently that of the I²C-bus.

The following is a list of the status codes:

Abbreviations used:

SLA: 7-bit slave address
R: Read bit
W: Write bit
$\overline{ACK}$: Acknowledgement (acknowledge bit = 0)
ACK: Not Acknowledge (acknowledge bit = 1)
DATA: 8-bit byte to or from the I²C-bus
MST: Master
SLV: Slave
TRX: Transmitter
REC: Receiver

MST/TRX mode
S1STA value

08H – a START condition has been transmitted
10H – a repeated START condition has been transmitted
18H – SLA and W have been transmitted, ACK received
20H – SLA and W have been transmitted, $\overline{ACK}$ received
28H – DATA of S1DAT has been transmitted, ACK received
30H – DATA of S1DAT has been transmitted, $\overline{ACK}$ received
38H – Arbitration lost in SLA, R/W or DATA

MST/REC mode
S1STA value

08H – a START condition has been transmitted
10H – a repeated START condition has been transmitted
38H – Arbitration lost while returning $\overline{ACK}$
40H – SLA and R have been transmitted, ACK received
48H – SLA and R have been transmitted, $\overline{ACK}$ received
50H – DATA has been received, ACK returned
58H – DATA has been received, $\overline{ACK}$ returned

SLV/REC mode
S1STA value

60H – Own SLA and W have been received, ACK returned
68H – Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned
70H – General CALL has been received, ACK returned
78H – Arbitration lost in SLA, R/W as MST. General CALL has been received
80H – Previously addressed with own SLA. DATA byte received, ACK returned
88H – Previously addressed with own SLA. DATA byte received, $\overline{ACK}$ returned
90H – Previously addressed with general CALL. DATA byte has been received, ACK has been returned
98H – Previously addressed with general CALL. DATA byte has been received, $\overline{ACK}$ has been returned
A0H – A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX

SLV/TRX mode
S1STA value

A8H – Own SLA and R have been received, ACK returned
B0H – Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned
B8H – DATA byte has been transmitted, ACK received
C0H – DATA byte has been transmitted, $\overline{ACK}$ received
C8H – Last DATA byte has been transmitted (AA = logic 0), ACK received

Miscellaneous
S1STA value

00H – Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition
F8H – No relevant state interruption available, SI = 0.

S1DAT (DAH)
Data Shift Register

7	6	5	4	3	2	1	0

Data shift register S1DAT
This register contains the serial data to be transmitted or data that has just been received. Bit 7 is transmitted or received first, i.e., data is shifted from left to right.

S1ADR (DBH)
Slave Address Register

7	6	5	4	3	2	1	0

S1ADR.0, GC: 0 = general CALL address is not recognized
1 = general CALL address is recognized

S1ADR.7-1: own slave address

This 8-bit register may be loaded with the 7-bit slave address, to which the controller will respond when programmed as a slave receiver/transmitter. The LSB bit (GC) is used to determine whether the general CALL address is recognized.

Table 3. SCL Frequency

CR2	CR1	CR0	f_{OSC} DIVIDED BY	BIT RATE (kHz) at f_{OSC}		
				3.58MHz	6MHz	12MHz
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50	100
1	1	0	60	59.7	100	–
1	1	1	not allowed	–	–	–

INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a multiple-source, two-priority level, nested interrupt system is provided. The 8XCL410 acknowledges interrupt requests from thirteen sources, as follows:

- INT0 and INT1
- Timer 0 and timer 1
- I^2C-bus serial I/O interrupt
- INT2 to INT9 (port 1)

Each interrupt vectors to a separate location in program memory for its service routine. Each source can be individually enabled or disabled by corresponding bits in the internal enable registers (IEN0, IEN1) The priority level is selected via the interrupt priority register (IP0, IP1). All enabled sources can be globally disabled or enabled.

External Interrupts INT2–INT9

Port 1 lines serve an alternative purpose as eight additional interrupts INT2–INT9. When enabled, each of these lines can “wake-up” the device from power-down mode. Using the IX1 register, each pin may be initialized to either active high or low. IRQ1 is the interrupt request flag register. Each flag, if the interrupt is enabled, will be set on an interrupt request but it must be cleared by software.

IEN0 (A8H)
Interrupt enable register

7	6	5	4	3	2	1	0
EA	—	ES1	—	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EEA	General enable/disable control 0 = no interrupt is enabled 1 = any individually enabled interrupt will be accepted
IEN0.6	—	(unused)
IEN0.5	ES1	Enable I_2C SIO interrupt
IEN0.4	—	(unused)
IEN0.3	ET1	Enable Timer T1 interrupt
IEN0.2	EX1	Enable external interrupt 1
IEN0.1	ET0	Enable Timer T0 interrupt
IEN0.0	EX0	Enable external interrupt 0

IEN1 (E8H)
Interrupt enable register

7	6	5	4	3	2	1	0
EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Bit	Symbol	Function
IEN1.7	EX9	Enable external interrupt 9
IEN1.6	EX8	Enable external interrupt 8
IEN1.5	EX7	Enable external interrupt 7
IEN1.4	EX6	Enable external interrupt 6
IEN1.3	EX5	Enable external interrupt 5
IEN1.2	EX4	Enable external interrupt 4
IEN1.1	EX3	Enable external interrupt 3
IEN1.0	EX2	Enable external interrupt 2

where 0 = interrupt disabled
1 = interrupt enabled

IP0 (B8H)
Interrupt priority register

7	6	5	4	3	2	1	0
—	—	PS1	—	PT1	PX1	PT0	PX0

Bit	Symbol	Function
IP0.7	—	(unused)
IP0.6	—	(unused)
IP0.5	PS1	I_2C SIO interrupt priority level
IP0.4	—	(unused)
IP0.3	PT1	Timer 1 interrupt prioity level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt prioity level
IP0.0	PX0	External interrupt 0 priority level

IP1 (F8H)
Interrupt priority register

7	6	5	4	3	2	1	0
PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Bit	Symbol	Function
IP1.7	PX9	External interrupt 9 priority level
IP1.6	PX8	External interrupt 8 priority level
IP1.5	PX7	External interrupt 7 priority level
IP1.4	PX6	External interrupt 6 priority level
IP1.3	PX5	External interrupt 5 priority level
IP1.2	PX4	External interrupt 4 priority level
IP1.1	PX3	External interrupt 3 priority level
IP1.0	PX2	External interrupt 2 priority level

Interrupt priority is as follows:
0 – low priority
1 – high priority

IX1 (E9H)
Interrupt polarity register

7	6	5	4	3	2	1	0
IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Bit	Symbol	Function
IX1.7	IL9	External interrupt 9 polarity level
IX1.6	IL8	External interrupt 8 polarity level
IX1.5	IL7	External interrupt 7 polarity level
IX1.4	IL6	External interrupt 6 polarity level
IX1.3	IL5	External interrupt 5 polarity level
IX1.2	IL4	External interrupt 4 polarity level
IX1.1	IL3	External interrupt 3 polarity level
IX1.0	IL2	External interrupt 2 polarity level

Writing either a “1” or “0” to an IX1 register bit sets the priority level of the corresponding external interrupt to active High or Low, respectively.

IRQ1 (C0H)
Interrupt request flag register

7	6	5	4	3	2	1	0
IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Bit	Symbol	Function
IRQ1.7	IQ9	External interrupt 9 request flag
IRQ1.6	IQ8	External interrupt 8 request flag
IRQ1.5	IQ7	External interrupt 7 request flag
IRQ1.4	IQ6	External interrupt 6 request flag
IRQ1.3	IQ5	External interrupt 5 request flag
IRQ1.2	IQ4	External interrupt 4 request flag
IRQ1.1	IQ3	External interrupt 3 request flag
IRQ1.0	IQ2	External interrupt 2 request flag

Priority	Vector	Source
X0 (highest)	0003H	External 0
S1	002BH	I^2C port
X5	0053H	External 5
T0	000BH	Timer 0
X6	005BH	External 6
X1	0013H	External 1
X2	003BH	External 2
X7	0063H	External 7
T1	001BH	Timer 1
X3	0043H	External 3
X8	006BH	External 8
X4	004BH	External 4
X9 (lowest)	0073H	External 9

Register	Function	SFR Address
IX1	Interrupt polarity register	E9H
IRQ1	Interrupt request flag register	C0H
IEN0	Interrupt enable register	A8H
IEN1	Interrupt enable register (INT2–INT9)	E8H
IP0	Interrupt priority register	B8H
IP1	Interrupt priority register (INT2–INT9)	F8H

OSCILLATOR CIRCUITRY

The on-chip oscillator circuitry of the 8XCL410 is a single stage inverting amplifier biased by an internal feedback resistor. (See Figure 4.) The oscillator can be operated with a quartz crystal, ceramic resonator, LC network or RC network. See Figure 5 for different configurations. When ordering parts, it is necessary to specify an oscillator option. The options are: RC when an RC network will be used, OSC 2 for oscillator operation below 4MHz, OSC 3 for oscillator operation from 4MHz to 10MHz, OSC 4 for oscillator operation above 10MHz, and 32kHz if 32kHz to 400kHz operation is desired.

For operation as a standard quartz oscillator, no external components are needed (except at 32KHz). When using external capacitors, ceramic resonators, coils, and RC networks to drive the oscillator, five different configurations are supported (see Figure 5 and Table 4).

In the power-down mode the oscillator is stopped and XTAL1 is pulled high. The oscillator inverter is switched off to ensure no current will flow. To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Figure 5(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is split using a flip-flop.

The following options are provided for optimum on-chip oscillator performance. Please state option when ordering:

Osc.1: Figure 5(c). An option for 32kHz clock applications with external trimmer for frequency adjustment.

A 4.7MΩ bias resistor must be connected in parallel with the crystal.

Osc.2: Figure 5(e). An option for low-power, low-frequency operations using LC components or quartz.

Osc.3: An option for medium frequency range applications.

Osc.4: An option for high frequency range applications.

RC: Figure 5(g). An option for an RC oscillator.

The equivalent circuit data of the internal oscillator compares with that of matched crystals.

The externally adjustable RC oscillator has a frequency range from 100kHz to 500kHz. (See Figure 7.)

Power-on Reset

The 8XCL410 contains on-chip circuitry which switch the port pins to the customer-defined logic level as soon as V_{DD} exceeds 1.3V if the mask option “ON” has been chosen (see Figures 8 and 9). As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods.

An hysteresis of approximately 50mV at a typical power-on switching level of 1.3V will ensure correct operation.

The on-chip power–on reset circuitry can also be switched off via the mask option “OFF”. This option reduces the power-down current to typically 800µA and can be chosen if external reset circuitry is used. For applications not requiring the internal reset, option “OFF” should be chosen.

An automatic reset can be obtained at power-on by connecting the RST pin to V_{DD} via a 10µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor discharges through the internal resistor R_{RST} to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

P80CL410: ROM-less VERSION OF P83CL410

The P80CL410 is a low voltage ROMless version of the P83CL410. The mask options on the P80CL410 are fixed as follows:

- Port Options:
  All ports except P16/P17 have option “1S”, i.e., standard port, High after reset. The ports P16/P17 have option “2S”, i.e., open drain, High after reset.
- Oscillator option: OSC3
- Power-on Reset option: OFF

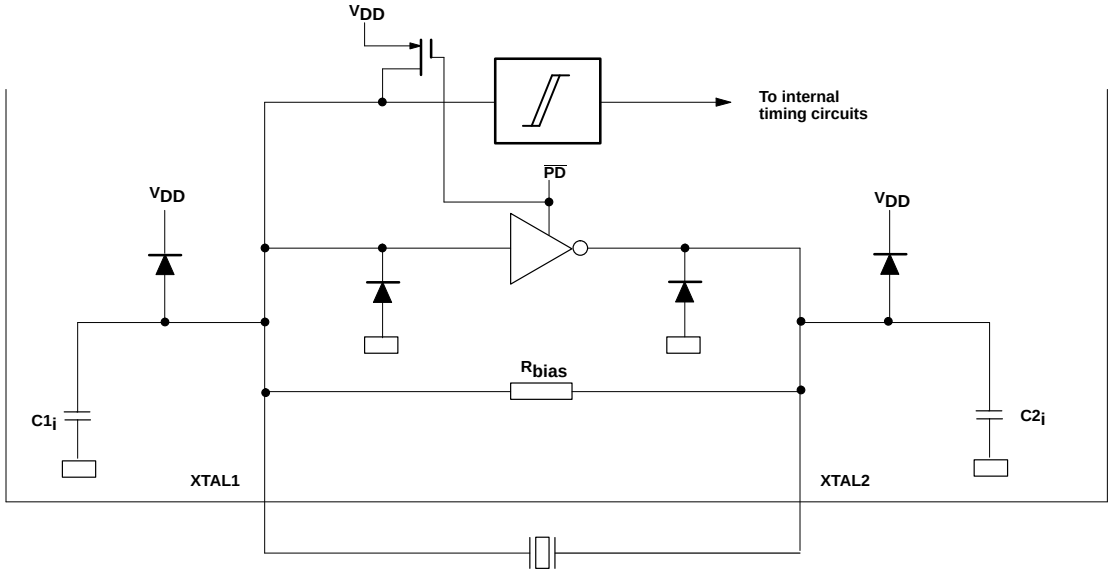


Figure 4. Oscillator

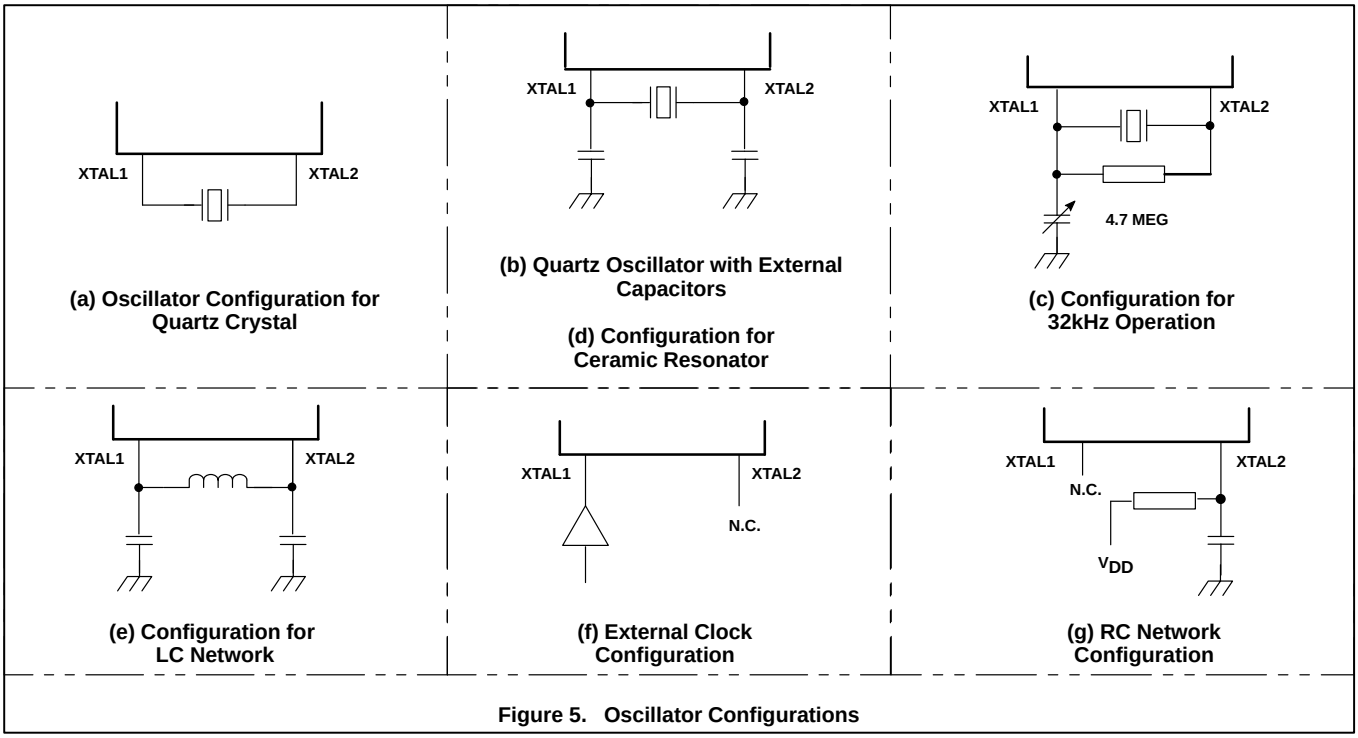


Figure 5. Oscillator Configurations

Table 4. Oscillator Type Selection Guide

RESONATOR	f (MHz)	OPTION	C1 EXT. MIN	C1 EXT. MAX	C2 EXT. MIN	C2 EXT. MAX	MAXIMUM RESONATOR SERIES RESISTANCE
Quartz	0.032	Osc.1	5	15	0	0	15kΩ[1]
Quartz	1.0	Osc.2	0	30	0	30	600Ω
Quartz	3.58	Osc.2	0	15	0	15	100Ω
Quartz	4.0	Osc.2	0	20	0	20	75Ω
Quartz	6.0	Osc.3	0	10	0	10	60Ω
Quartz	10.0	Osc.4	0	15	0	15	60Ω
Quartz	12.0	Osc.4	0	10	0	10	40Ω
Quartz	16.0	Osc.4	0	15	0	15	20Ω
PXE	0.455	Osc.2	40	50	40	50	10Ω
PXE	1.0	Osc.2	15	50	15	50	100Ω
PXE	3.58	Osc.2	0	40	0	40	10Ω
PXE	4.0	Osc.2	0	40	0	40	10Ω
PXE	6.0	Osc.2	0	20	0	20	5Ω
PXE	10.0	Osc.3	0	15	0	15	6Ω
PXE	12.0	Osc.4	10	40	10	40	6Ω
LC		Osc.2	20	90	20	90	10µH = 1Ω 100µH = 5Ω 1mH = 75Ω

NOTE:
1. 32kHz quartz crystals with a series resistance higher than 15kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5V.

Table 5. Oscillator Equivalent Circuit Parameters (see Figure 6)

PARAMETER	OPTION	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Transconductance	Osc.1	g_m	T = +25°C; V_{DD} = 4.5V	–	15	–	µs
	Osc.2	g_m	T = +25°C; V_{DD} = 4.5V	200	600	1000	µs
	Osc.3	g_m	T = +25°C; V_{DD} = 4.5V	400	1500	4000	µs
	Osc.4	g_m	T = +25°C; V_{DD} = 4.5V	1000	4000	10000	µs
Input capacitance	Osc.1	$c1_i$		–	3.0	–	pF
	Osc.2	$c1_i$		–	8.0	–	pF
	Osc.3	$c1_i$		–	8.0	–	pF
	Osc.4	$c1_i$		–	8.0	–	pF
Output capacitance	Osc.1	$c2_i$		–	23.0	–	pF
	Osc.2	$c2_i$		–	8.0	–	pF
	Osc.3	$c2_i$		–	8.0	–	pF
	Osc.4	$c2_i$		–	8.0	–	pF
Output resistance	Osc.1	R2		–	3800	–	kΩ
	Osc.2	R2		–	65	–	kΩ
	Osc.3	R2		–	18	–	kΩ
	Osc.4	R2		–	5.0	–	kΩ

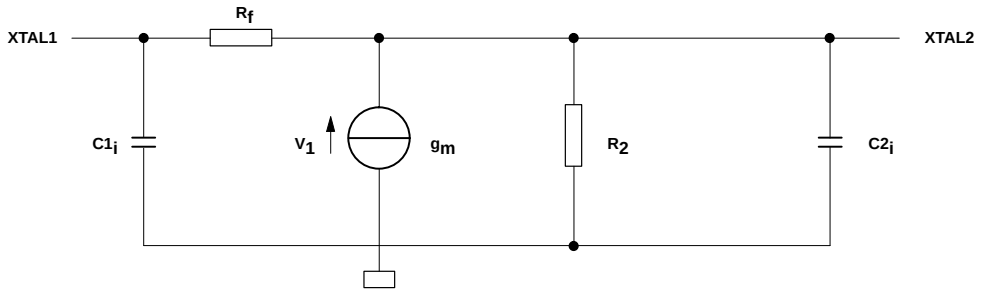


Figure 6. Equivalent Circuit Diagram

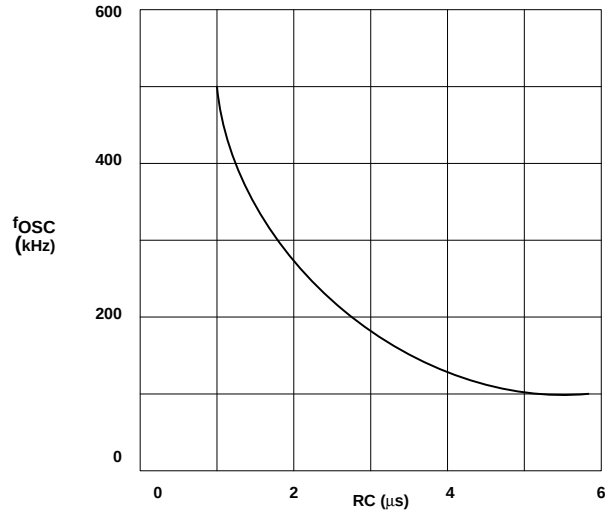


Figure 7. Frequency as a Function of RC

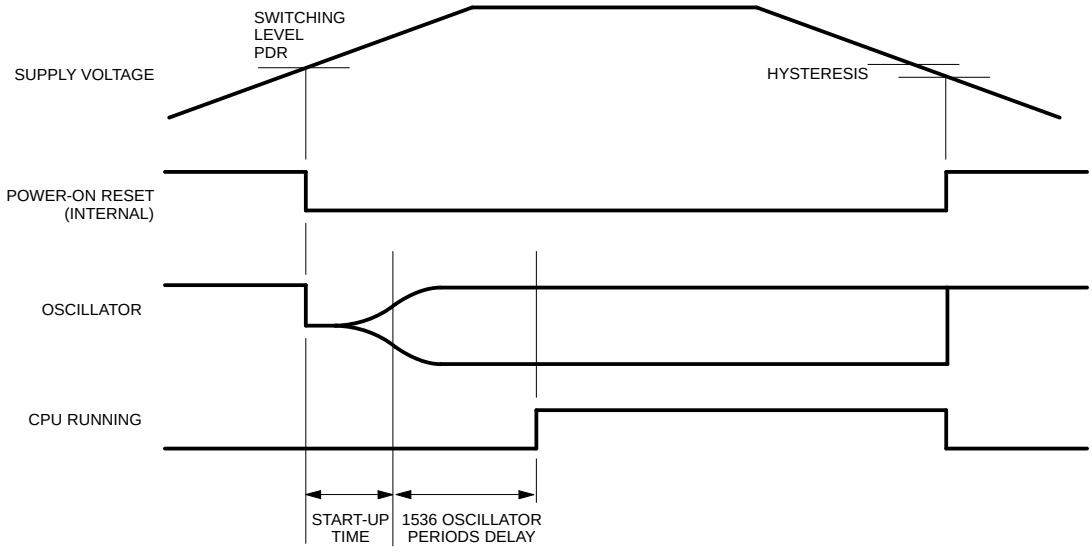


Figure 8. Power-on Reset Switching Level

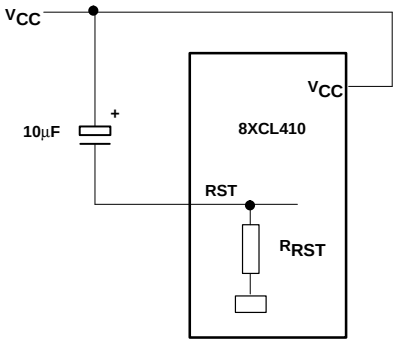


Figure 9. Recommended Power-on Reset Circuitry

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Supply voltage	–0.5 to +6.5	V
All input voltages	–0.5 to V_{DD} +0.5	V
DC current into any input or output	5	mA
Total power dissipation	300	mW
Storage temperature range	–65 to +150	°C
Operating ambient temperature range	–40 to +85	°C
Operating junction temperature	125	°C

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

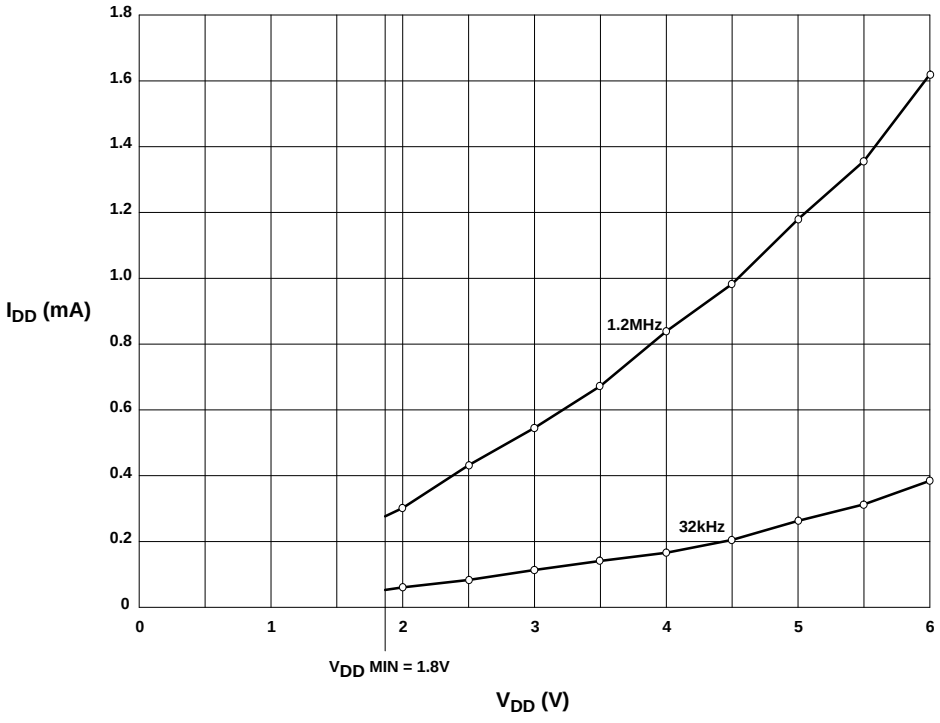
DC ELECTRICAL CHARACTERISTICS

T_{amb} = –40°C to +85°C, V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
V_{DD}	Supply voltage RAM retention voltage in power-down mode	f_{CLK} (see Figure 13)	1.8 1.0	6.0 —	V V
I_{DD}	Power supply current: Operating[1]				
	OSC 1 option	f_{CLK} = 32kHz, V_{DD} = 1.8V, T_{amb} = +25°C	—	50	µA
	OSC 2 option	f_{CLK} = 3.58MHz, V_{DD} = 3V	—	2.5	mA
	OSC 2 option	f_{CLK} = 10MHz, V_{DD} = 5V	—	14	mA
	OSC 3 option	f_{CLK} = 12MHz, V_{DD} = 5V	—	16	mA
	OSC 4 option	f_{CLK} = 12MHz, V_{DD} = 5V	—	20	mA
	Idle mode[2]				
	OSC 1 option	f_{CLK} = 32kHz, V_{DD} = 1.8V, T_{amb} = +25°C	—	25	µA
	OSC 2 option	f_{CLK} = 3.58MHz, V_{DD} = 3V	—	1.0	mA
	OSC 2 option	f_{CLK} = 10MHz, V_{DD} = 5V	—	5.0	mA
	OSC 3 option	f_{CLK} = 12MHz, V_{DD} = 5V	—	7.0	mA
	OSC 4 option	f_{CLK} = 12MHz, V_{DD} = 5V	—	8.5	mA
	Power-down mode[3]	V_{DD} = 1.8V, T_{amb} = +25°C	—	10	µA
V_{IL}	Input low voltage		V_{SS}	$0.3V_{DD}$	V
V_{IH}	Input high voltage		$0.7V_{DD}$	V_{DD}	V
I_{OL}	Output sink current, except SDA, SCL	V_{DD} = 5V, V_{OL} = 0.4V V_{DD} = 2.5V, V_{OL} = 0.4V	1.6 0.7		mA mA
I_{OL1}	Output sink current, SDA, SCL	V_{DD} = 5V, V_{OL} = 0.4V	3.0		mA
I_{OH}	Output source current (push-pull options only)	V_{DD} = 5V, V_{OH} = V_{DD} – 0.4V V_{DD} = 2.5V, V_{OH} = V_{DD} – 0.4V	1.6 0.7		mA mA
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{DD} = 5V,V_{IN} = 0.4V V_{DD} = 2.5V,V_{IN} = 0.4V		–100 –50	µA µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	V_{DD} = 5V, V_{IN} = V_{DD}/2 V_{DD} = 2.5V, V_{IN} = V_{DD}/2		–1.0 –500	mA µA
I_{LI}	Input leakage current, port 0, $\overline{EA}$	V_{SS} < V_I < V_{DD}		±10	µA
R_{RST}	Internal reset pull-down resistor		10	200	kΩ

NOTES:

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with t_r = t_f = 10ns; V_{IL} = V_{SS}, V_{IH} = V_{DD}; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}; all open drain outputs connected to V_{SS}.
2. The idle supply current is measured with all output pins disconnected; XTAL1 driven with t_r = t_f = 10ns; V_{IL} = V_{SS}, V_{IH} = V_{DD}; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL1 not connected; $\overline{EA}$ = port 0 = V_{DD}; RST = V_{SS}; all open-drain outputs connected to V_{SS}.
4. The RC-oscillator is not implemented in this version.
5. Circuits with “power-on reset” option “OFF” are tested at V_{DDMIN} = 1.8V, with option “ON” (typically 1.3V) are tested at V_{DDMIN} = 2.3V.



Typical Operating Current Versus Supply and Frequency (32kHz–1.2MHz) at +25°C

AC ELECTRICAL CHARACTERISTICS

T_{amb} = –40°C to +85°C, V_{SS} = 0V[1, 2]

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
Program Memory							
$1/t_{CLCL}$		Oscillator frequency			0	20	MHz
t_{LL}	10	ALE pulse width	127		$2t_{CLCL}$–40		ns
t_{AL}	10	Address valid to ALE low	43		t_{CLCL}–40		ns
t_{LA}	10	Address hold after ALE low	48		t_{CLCL}–35		ns
t_{LIV}	10	ALE low to valid instruction in		233		$4t_{CLCL}$–100	ns
t_{LC}	10	ALE low to $\overline{PSEN}$ low	58		t_{CLCL}–25		ns
t_{CC}	10	$\overline{PSEN}$ pulse width	215		$3t_{CLCL}$–35		ns
t_{CIV}	10	$\overline{PSEN}$ low to valid instruction in		125		$3t_{CLCL}$–125	ns
t_{CI}	10	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{CIF}	10	Input instruction float after $\overline{PSEN}$		63		t_{CLCL}–20	ns
t_{AVI}	10	Address to valid instruction in		302		$5t_{CLCL}$–115	ns
t_{AFC}	10	$\overline{PSEN}$ low to address float	0		0		ns
Data Memory							
t_{RR}	11	$\overline{RD}$ pulse width	400		$6t_{CLCL}$–100		ns
t_{WW}	12	$\overline{WR}$ pulse width	400		$6t_{CLCL}$–100		ns
t_{LA}	11, 12	Address hold time after ALE	48	–	t_{CLCL}–35	–	ns
t_{RD}	11	$\overline{RD}$ low to valid data in		250		$5t_{CLCL}$–165	ns
t_{DFR}	11	Data float after $\overline{RD}$		97		$2t_{CLCL}$–70	ns
t_{LD}	11	ALE low to valid data in		517		$8t_{CLCL}$–150	ns
t_{AD}	11	Address to valid data in		585		$9t_{CLCL}$–165	ns
t_{LW}	11, 12	ALE low to $\overline{RD}$ or $\overline{WR}$ low	200	300	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AW}	11, 12	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	203		$4t_{CLCL}$–130		ns
t_{DWX}	12	Data valid to $\overline{WR}$ transition	23		t_{CLCL}–60		ns
t_{DW}	11	Data valid to $\overline{WR}$	433	–	$7t_{CLCL}$–150	–	ns
t_{WD}	12	Data hold after $\overline{WR}$	33		t_{CLCL}–50		ns
t_{AFR}	11	$\overline{RD}$ low to address float[3]		12		12	ns
t_{WHLH}	11, 12	$\overline{RD}$ or $\overline{WR}$ high to ALE high	43	123	t_{CLCL}–40	t_{CLCL}+40	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 50pF, load capacitance for all other outputs = 40pF.
3. Interfacing the 8XCL410 to devices with float time up to 75ns is permitted. This limited bus connection will not cause damage to port 0 drivers.

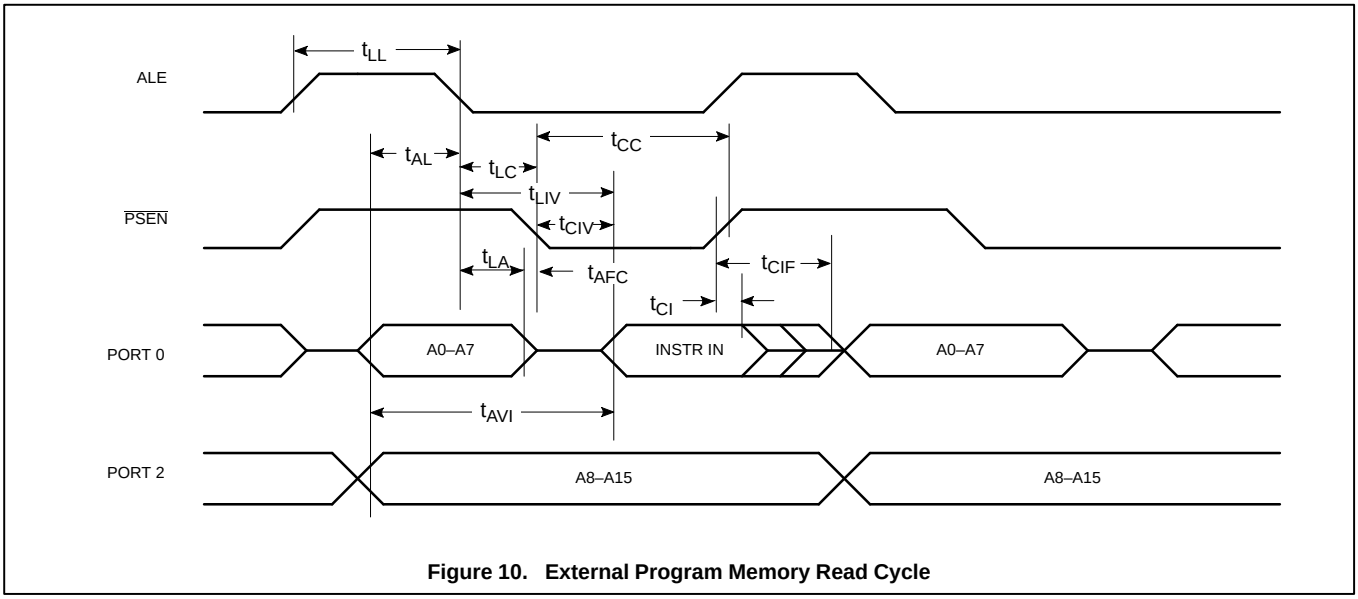


Figure 10. External Program Memory Read Cycle

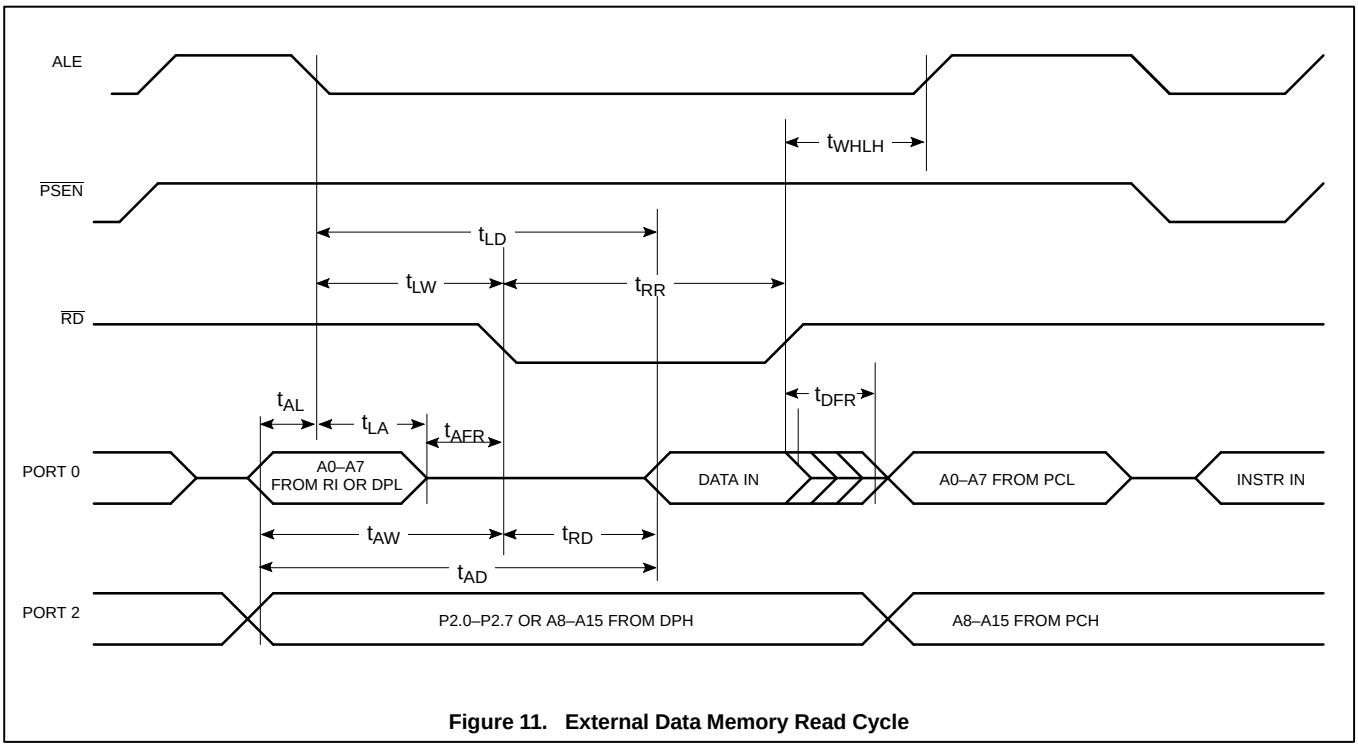


Figure 11. External Data Memory Read Cycle

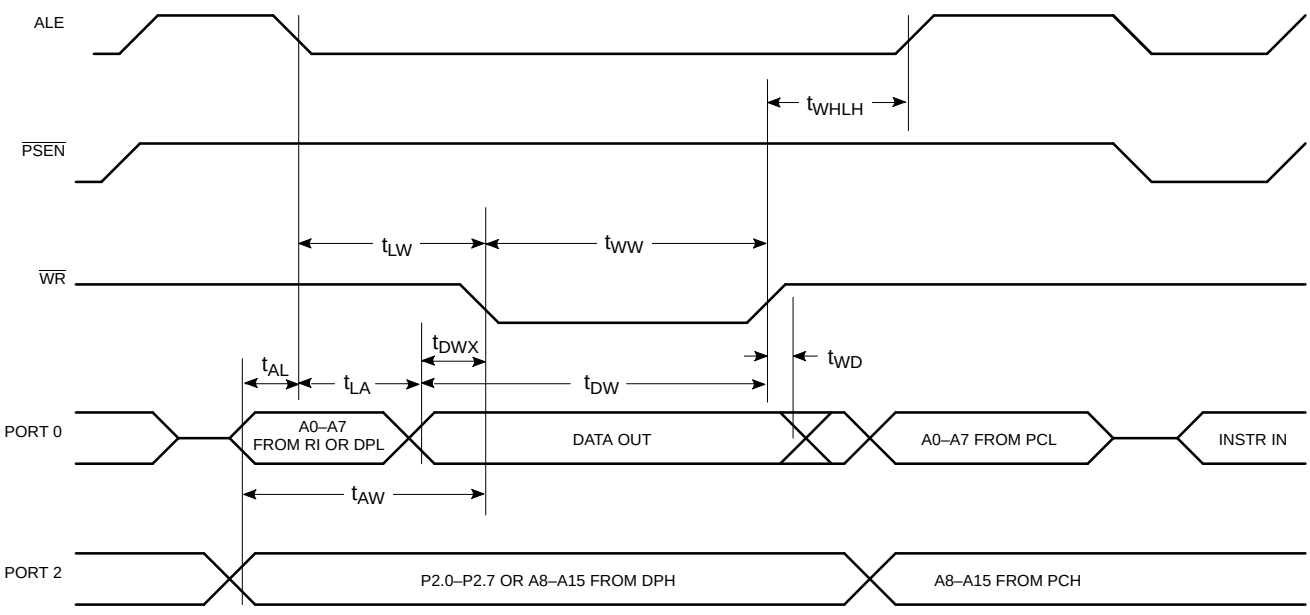


Figure 12. External Data Memory Write Cycle

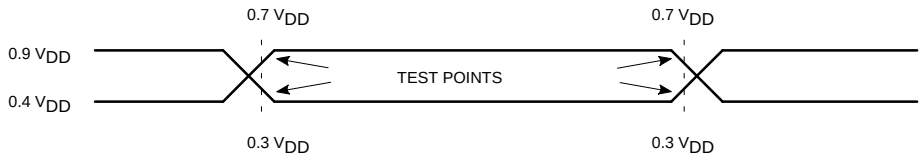


Figure 13. AC Testing Input Waveform

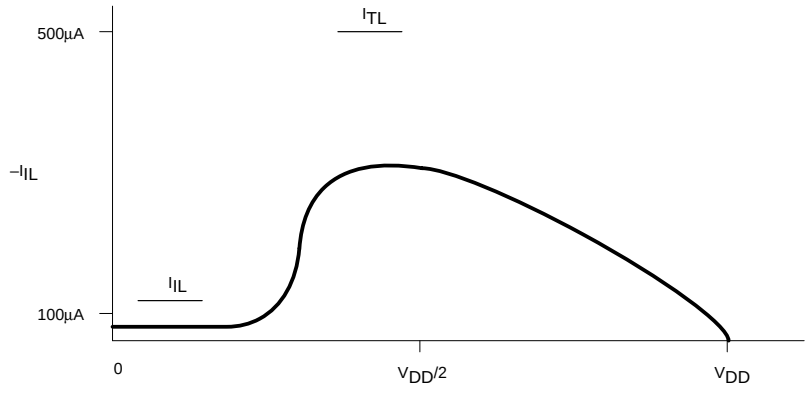
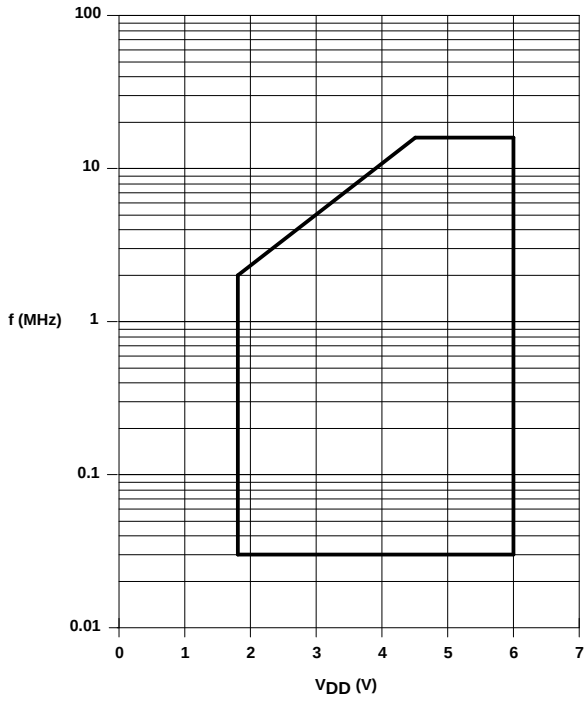


Figure 14. Input Current



NOTE: Below 32kHz, clock has to be supplied externally.

Figure 15. Frequency Operating Range

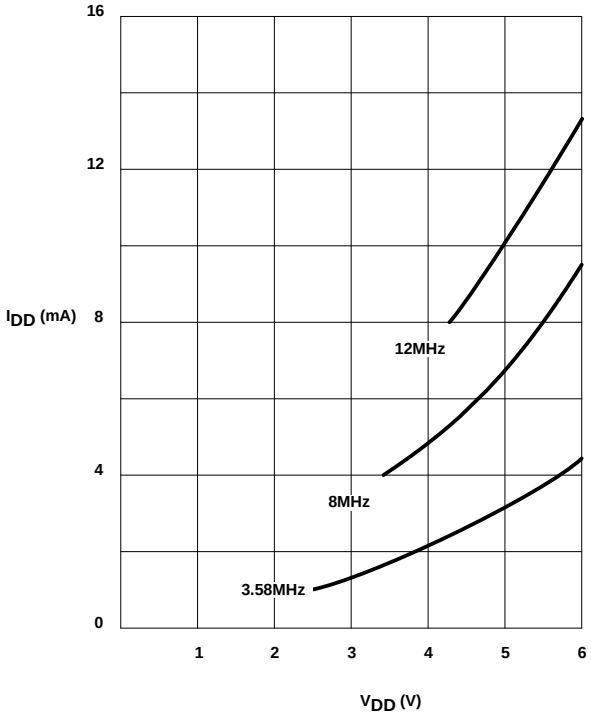


Figure 16. Typical Operating Current as a Function of Frequency and V_{DD}, T_{amb} = 25°C

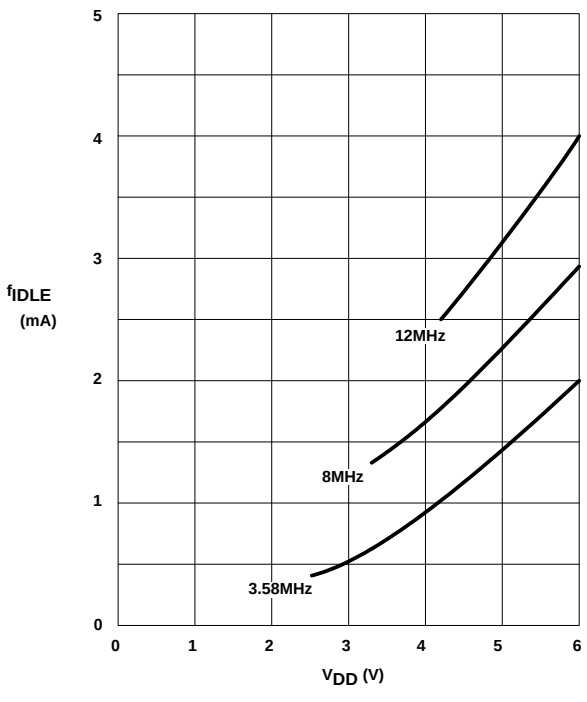


Figure 17. Typical Idle Current as a Function of Frequency and V_{DD}, T_{amb} = 25°C

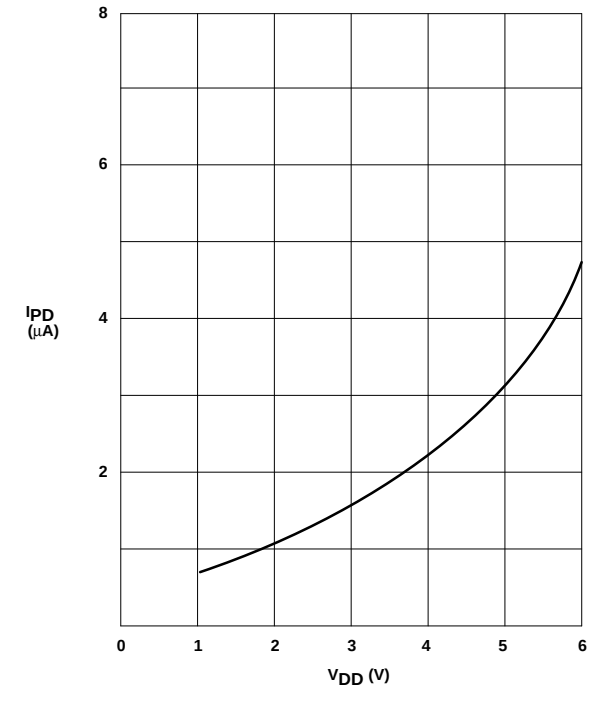


Figure 18. Typical Power-Down Current Vs. Frequency and V_{DD}, T_{amb} = 25ºC

PIGGYBACK SPECIFICATION

The differences between the masked version and the piggyback are described herein.

General Description

The P85CL000HFZ is a piggy-back version with 256 bytes of RAM used for emulation of the P83CL410 microcontroller. The P85CL000HFZ is manufactured in an advanced CMOS technology. The instruction set of the P85CL000HFZ is based on that of the 8051. The device has low power consumption and a wide supply voltage range. The P85CL000HFZ has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. For timing and AC/DC characteristics, please refer to the P83CL410 specifications.

Features

- Full static 80C51 CPU
- 8-bit CPU, RAM, I/O in a single 40-lead DIP
- Socket for up to 16k external EPROM
- 256 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- External memory expandable up to 128K, external ROM up to 64K and/or RAM up to 64K
- Thirteen source, thirteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- I²C-bus interface for serial transfer on two lines
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth up to 128 bytes
  - multiply, divide, subtract and compare instructions
- STOP and IDLE instructions
- Wake-up via external interrupts at port 1
- Single supply voltage of 1.8V to 6.0V
- On-chip oscillator (option: oscillator 4)
- Very low current consumption
- Operating temperature range: –40 to +85°C

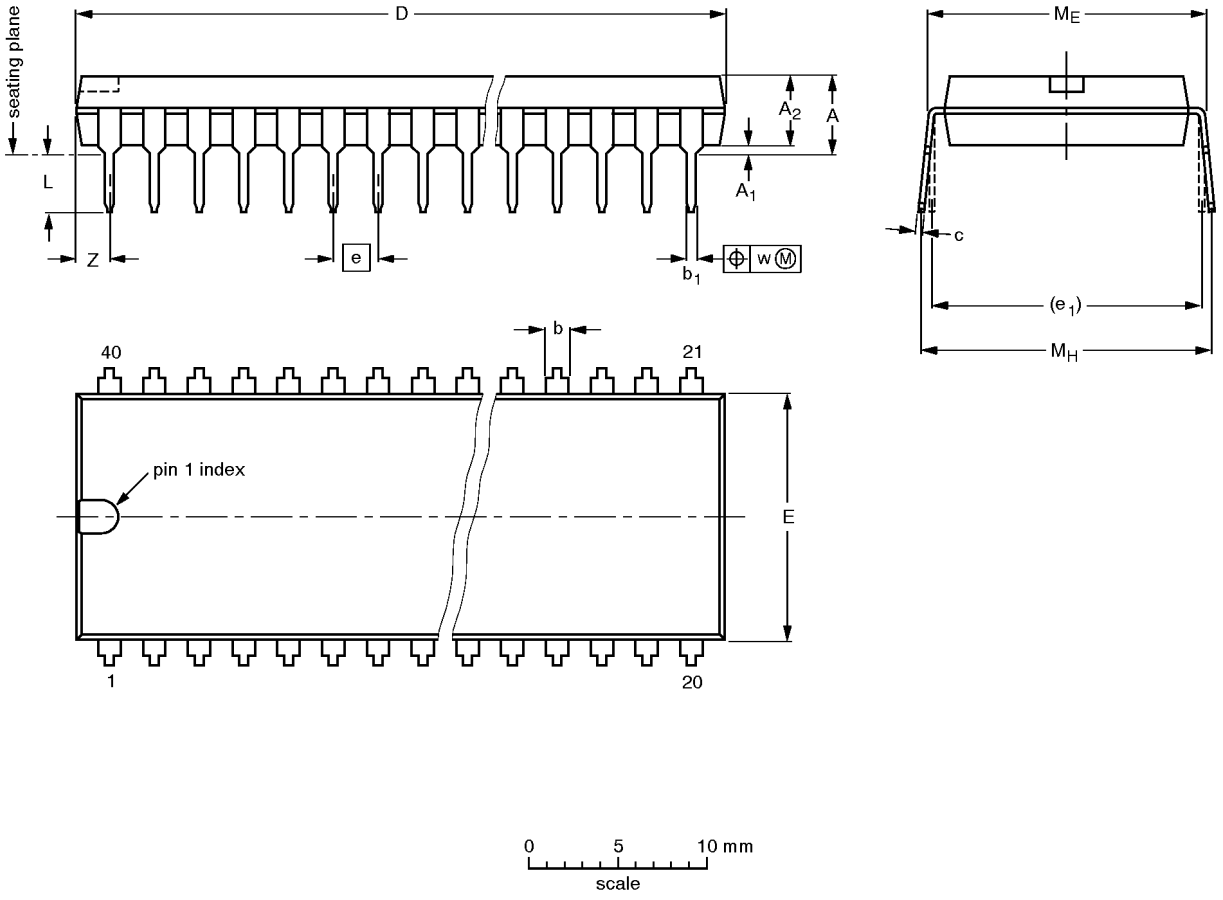
STANDARD PIGGYBACK

Types: P85CL000HFZ
Emulation for: P83CL410, P80CL51

List of differences between masked microcontroller and corresponding piggyback:

PARAMETER	MASKED CONTROLLER	PIGGYBACK
RAM size	128	256
ROM size	4k	EPROM size dependent (max 16k)
Port option	1, 2, 3	1
Oscillator option	Osc. 1, 2, 3, 4, RC	Osc. 4
Mech. dimensions	Standard Dual In-Line, Small Outline	See SOT158A
Current cons.	I_{DD}	I_{DD} (OSC. 4) + I_{EPROM}
Voltage range	full	full, limited by EPROM
ESD	specification	not tested (different package)

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

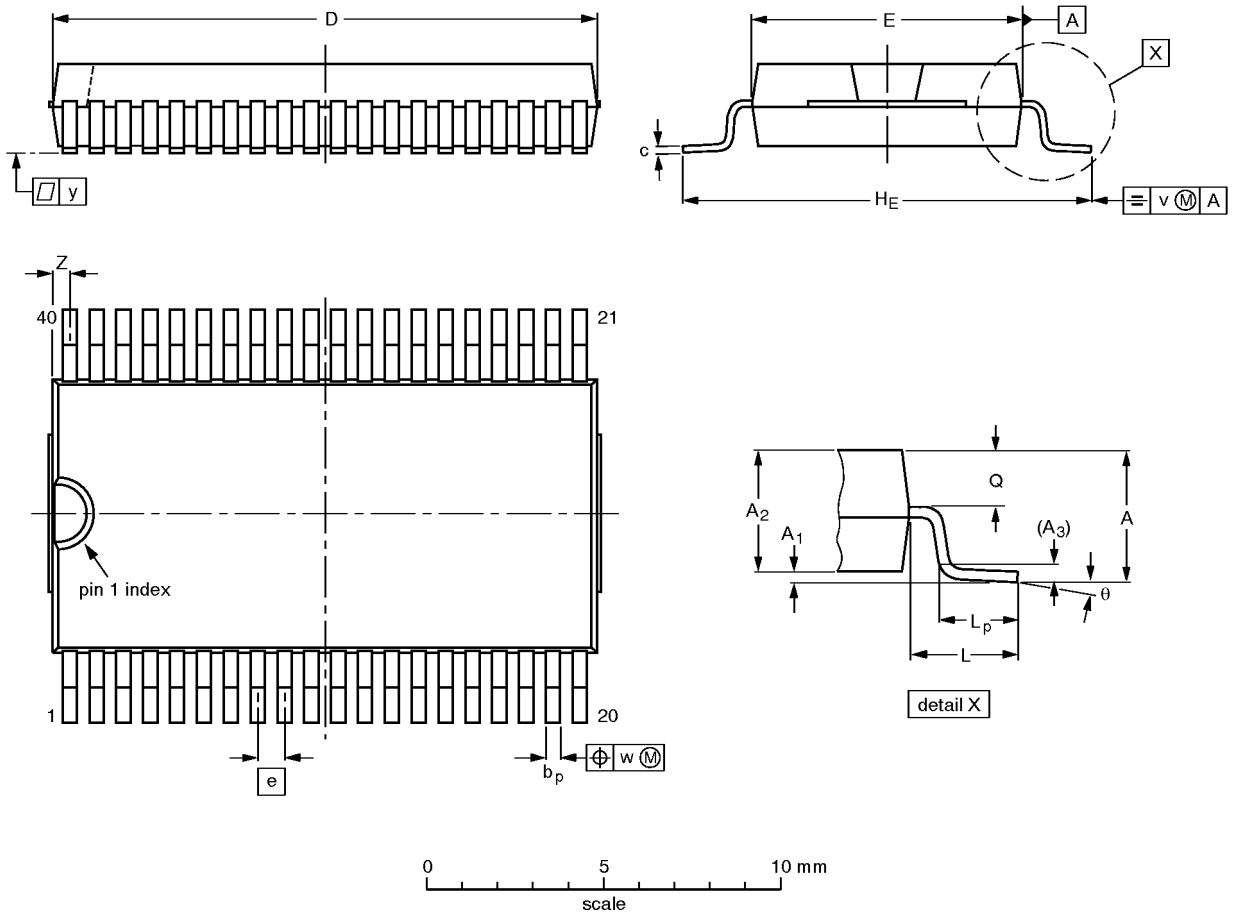
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

VSO40: plastic very small outline package; 40 leads **SOT158-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

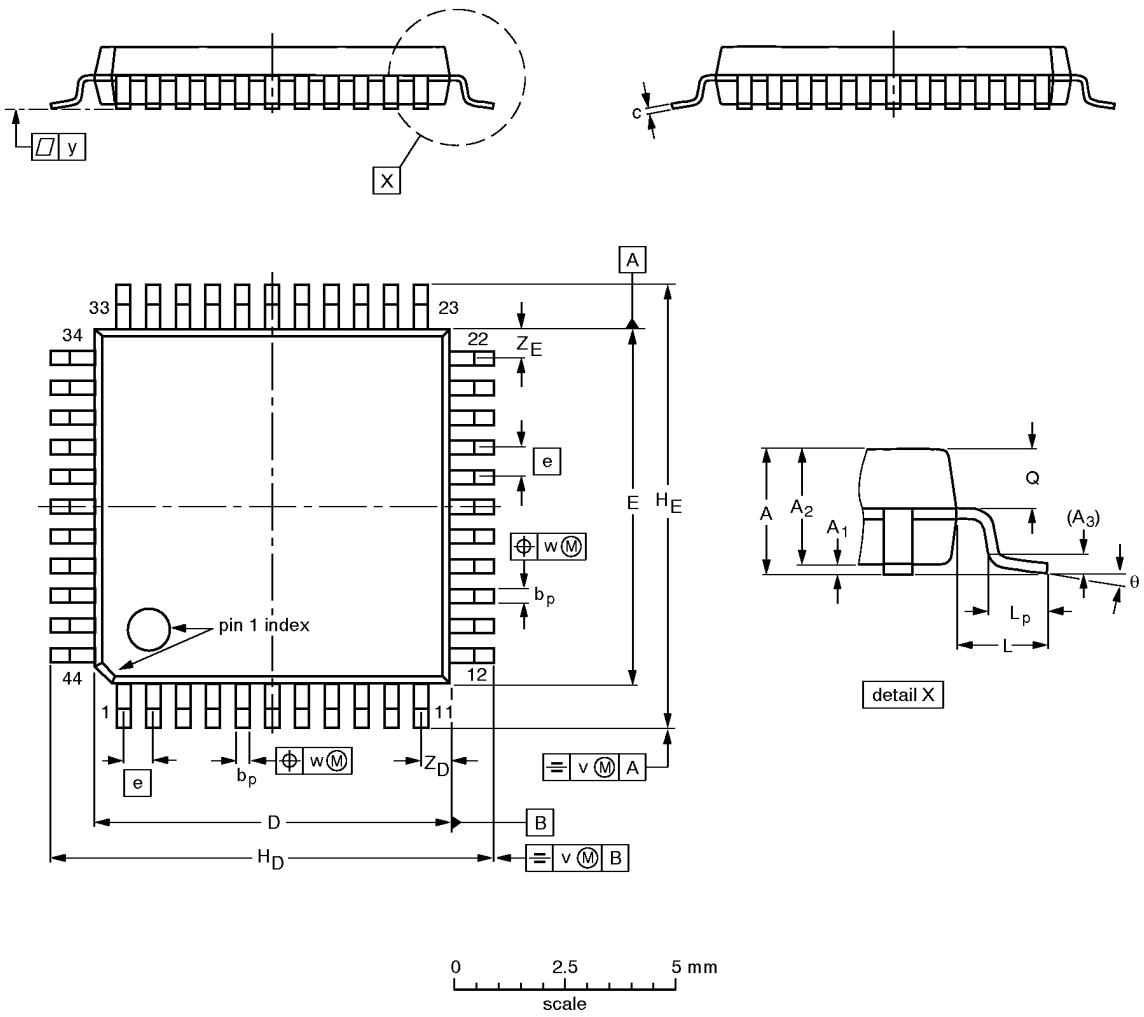
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Note

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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